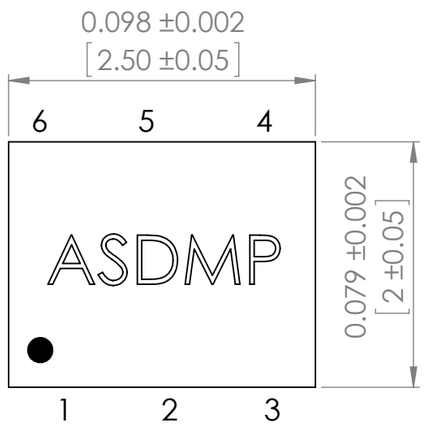
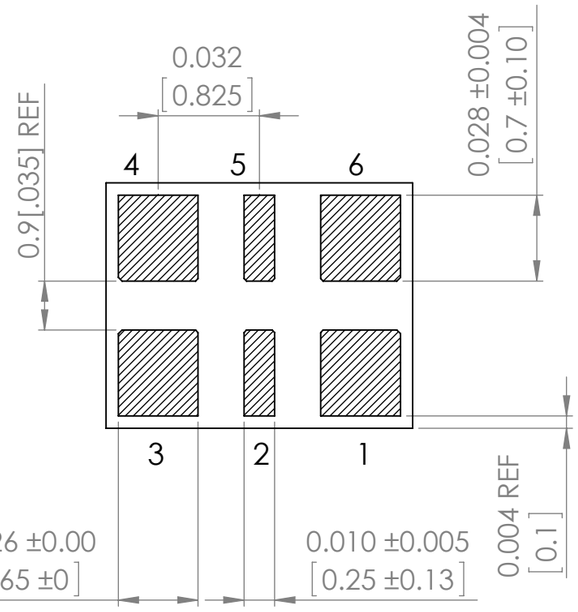
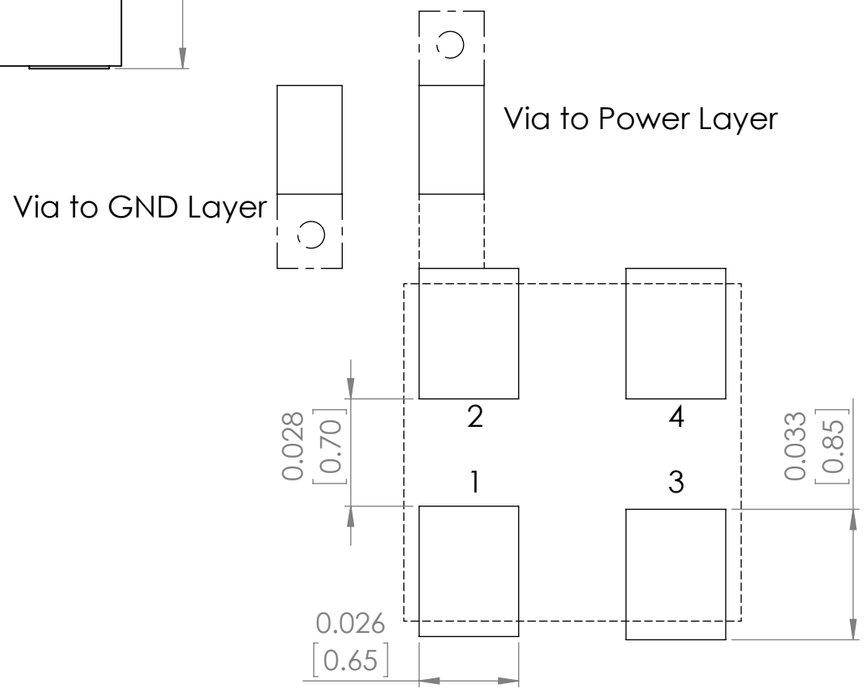
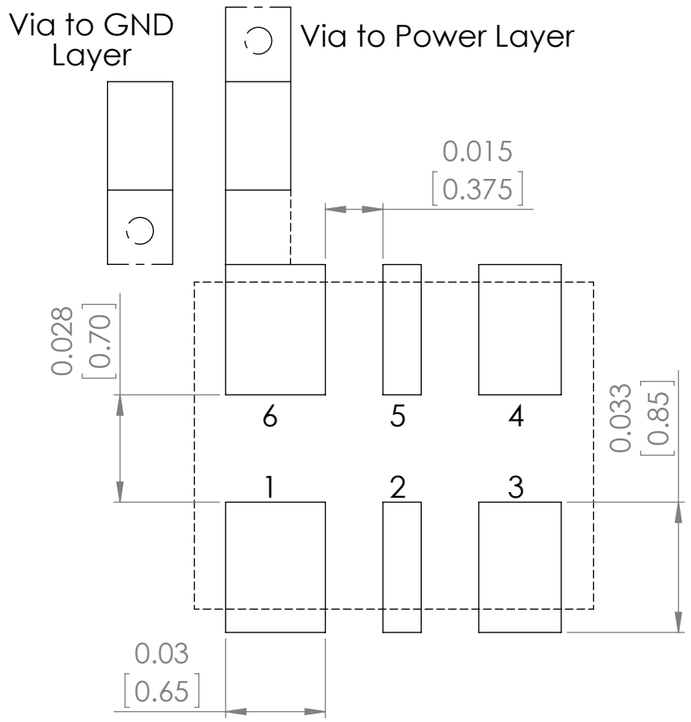




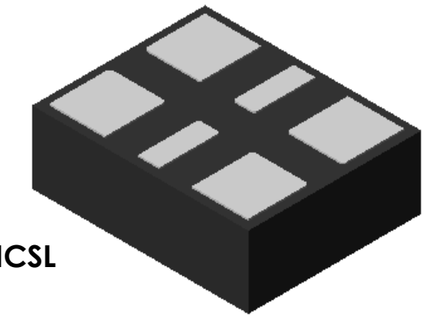


Recommended Land Pattern FOR CMOS

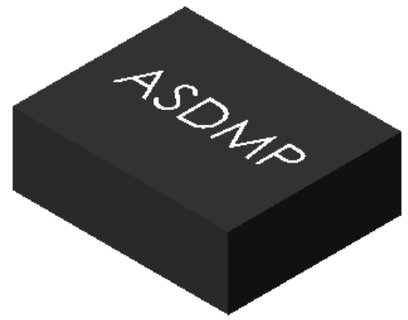
NOTE: Recommended using approximately
0.01uf bypass capacitor between PIN 6 and 3



Recommended Land Pattern FOR LVPECL,LVDS,HCSL



Pin	Function
1	Tri-state
2	NC
3	GND
4	Output
5	NC (CMOS) Output (LVPECL, LVDS, HCSL)
6	Vdd



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCH(MM) SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:		FINISH:		DEBUR AND BREAK SHARP EDGES		
	NAME	SIGNATURE	DATE			
DRAWN	XXXXXX					
CHK'D	XXXXXX					
APPV'D						
MFG						
Q.A				MATERIAL:		
				WEIGHT:		

DO NOT SCALE DRAWING — REVISION -

ABRACON CORPORATION

30332 Esperanza, Rancho Santa margarita, California 92688

TITLE: VOLTAGE CONTROLLED TEMP. COMPENSATED SMD CRYSTAL OSCILLATOR

DWG NO. ASDMP — A3

SCALE:10:1 — SHEET 1 OF 1