STL128DNFP

High voltage fast-switching NPN power transistor

Features

- High voltage capability
- Low spread of dynamic parameters
- Minimum lot-to-lot spread for reliable operation
- Very high switching speed
- Large RBSOA
- Integrated antiparallel collector-emitter diode
- Fully insulated package (U.L. compliant) for easy mounting

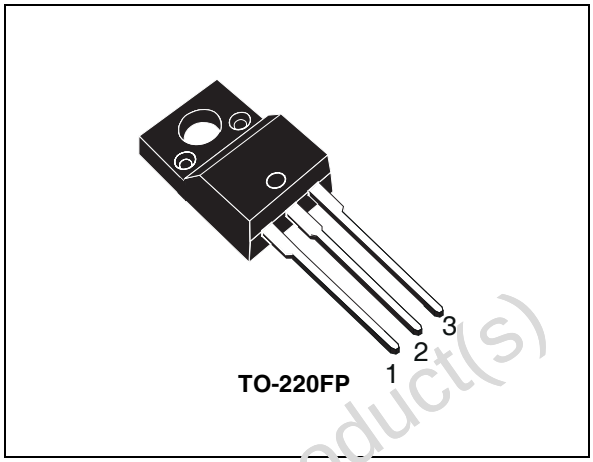
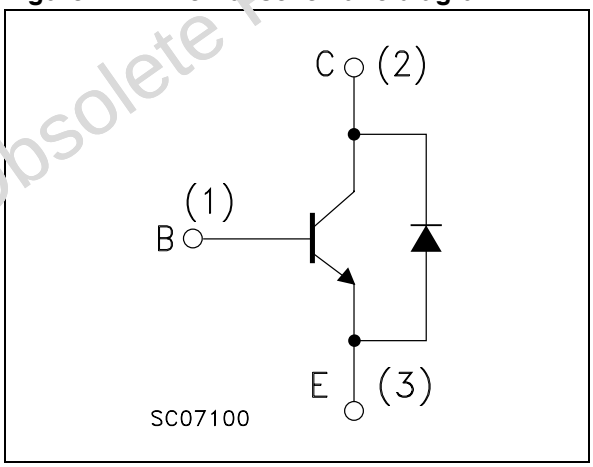


Figure 1. Internal schematic diagram



Applications

- Electronic ballast for fluorescent lighting
- Flyback and forward single transistor low power converters

Description

The device is manufactured using high voltage Multi Epitaxial Planar technology for high switching speeds and medium voltage capability. It uses a cellular emitter structure with planar edge termination to enhance switching speeds while maintaining the wide RBSOA. The device is designed for use in lighting applications and low cost switch-mode power supplies.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL128DNFP	L128DNFP	TO-220FP	Tube

Content

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{BE} = 0)	700	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	400	V
V_{EBO}	Base-emitter voltage (I_C = 0, I_B = 2A, t_P < 10µs)	$V_{(BR)EBO}$	V
I_C	Collector current	3	A
I_{CM}	Collector peak current (t_P < 5ms)	6	A
I_B	Base current	1.5	A
I_{BM}	Base peak current (t_P < 5ms)	3	A
P_{TOT}	Total dissipation at T_c = 25°C	28	W
V_{ins}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t =1s; T_C =25°C)	1500	V
T_{stg}	Storage temperature	-65 to 150	°C
T_J	Max. operating junction temperature	150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	4.46	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cut-off current (V_{BE} = 0)	V_{CE} = 700V V_{CE} = 700V, T_c = 125°C			100 500	µA µA
I_{CEO}	Collector cut-off current (I_B = 0)	V_{CE} = 400V			250	µA
$V_{(BR)EBO}$	Emitter-base breakdown voltage (I_C = 0)	I_E = 10mA	9		18	V
$V_{CEO(sus)}$(1)	Collector-emitter sustaining voltage (I_C = 0)	I_C = 10mA	400			V
$V_{CE(sat)}$(1)	Collector-emitter saturation voltage	I_C = 1A , I_B = 0.2A I_C = 2A , I_B = 0.4A			1 1.5	V V
$V_{BE(sat)}$(1)	Base-emitter saturation voltage	I_C = 1A , I_B = 0.2A I_C = 2A , I_B = 0.4A			1.2 1.3	V V
h_{FE}(1)	DC current gain	I_C = 10mA, V_{CE} = 5V I_C = 2A, V_{CE} = 5V	10 8			
V_f	Diode forward voltage	I_C= 1 A			2.5	V
t_s t_f	Resistive load Storage time Fall time	I_C = 1A, I_{B1}= -I_{B2} = 0.2A V_{CC} = 125V, t_p = 20µs			4.5 0.4	µs µs

1. Pulsed duration = 300 ms, duty cycle ≤1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

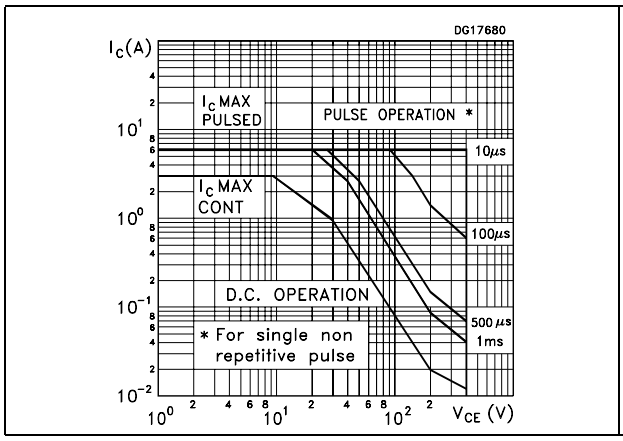


Figure 3. Derating curve

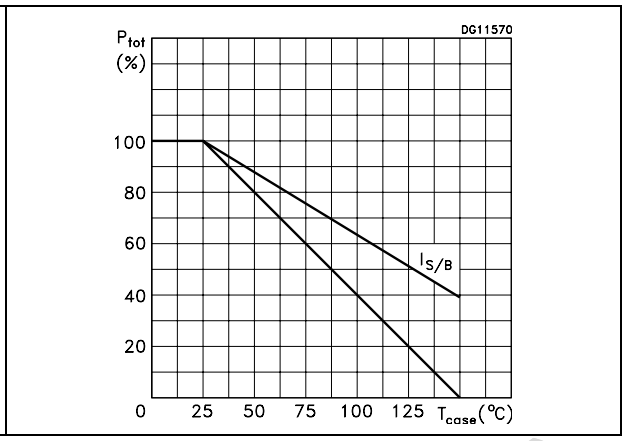


Figure 4. DC current gain

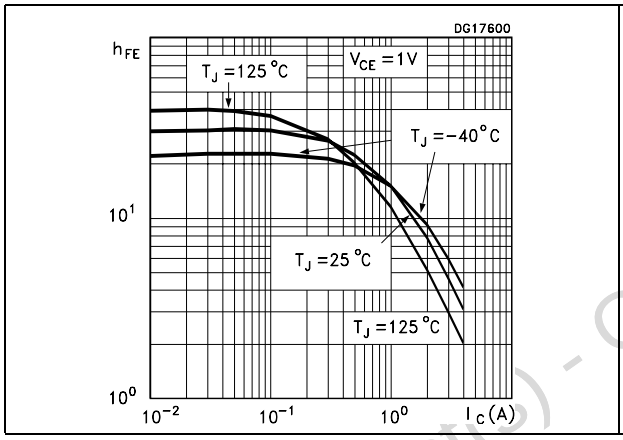


Figure 5. DC current gain

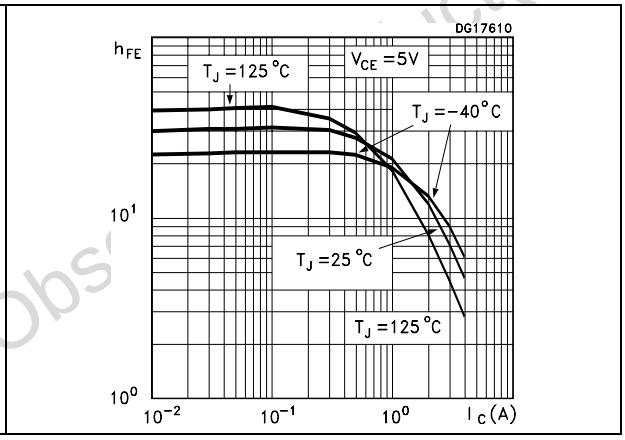


Figure 6. Collector-emitter saturation voltage

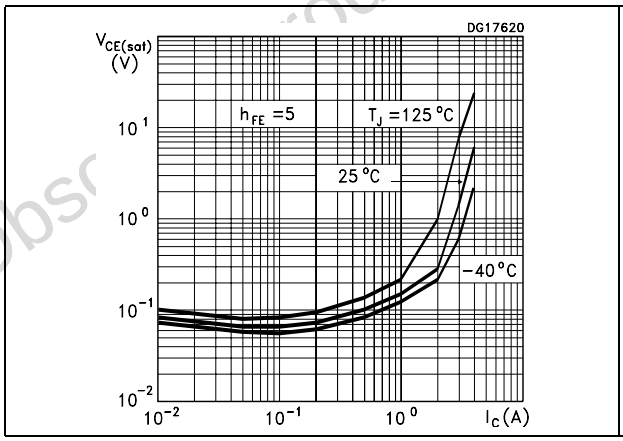


Figure 7. Base-emitter saturation voltage

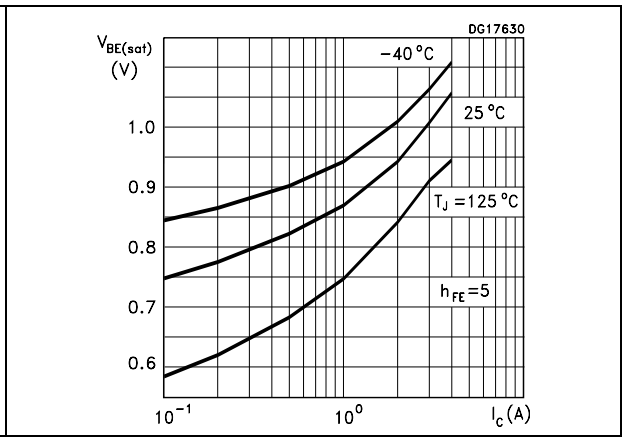


Figure 8. Freewheel diode forward voltage

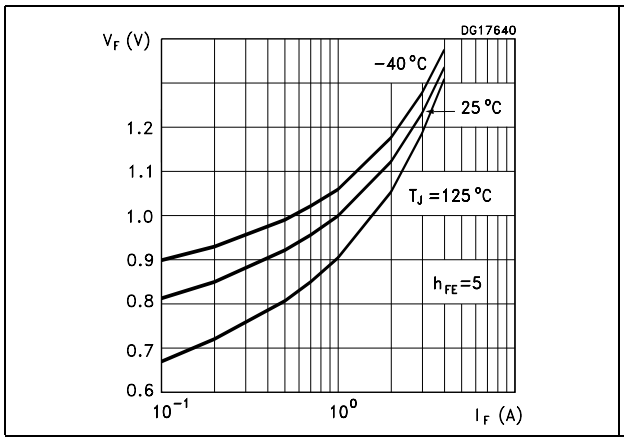


Figure 9. Resistive load switching time

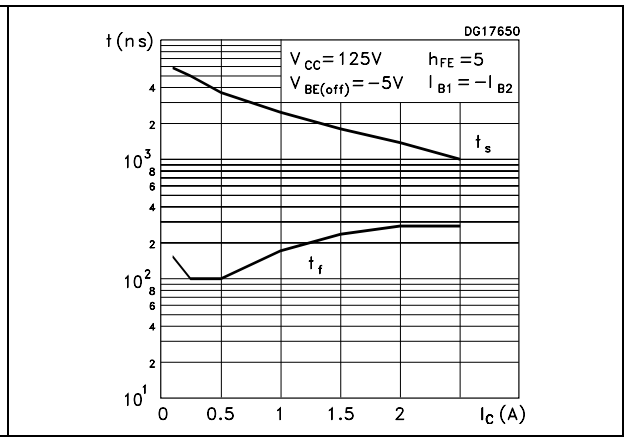
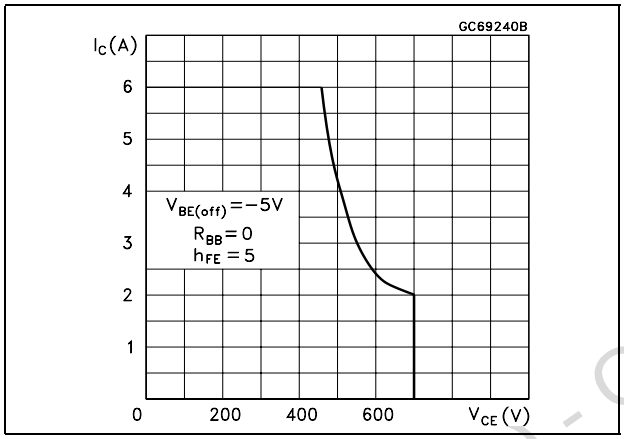
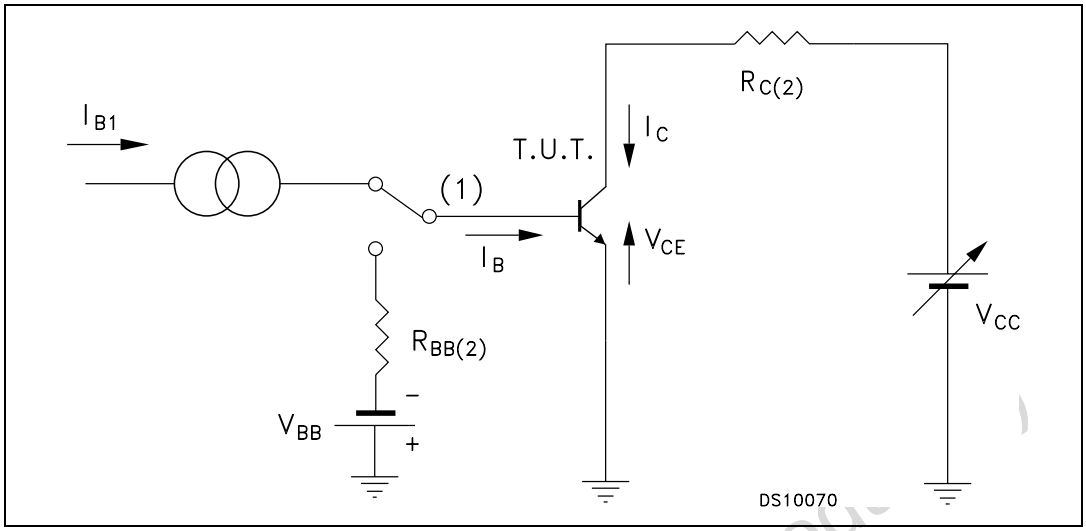


Figure 10. Reverse biased safe operating area



3 Test circuit

Figure 11. Resisive load switching test circuit



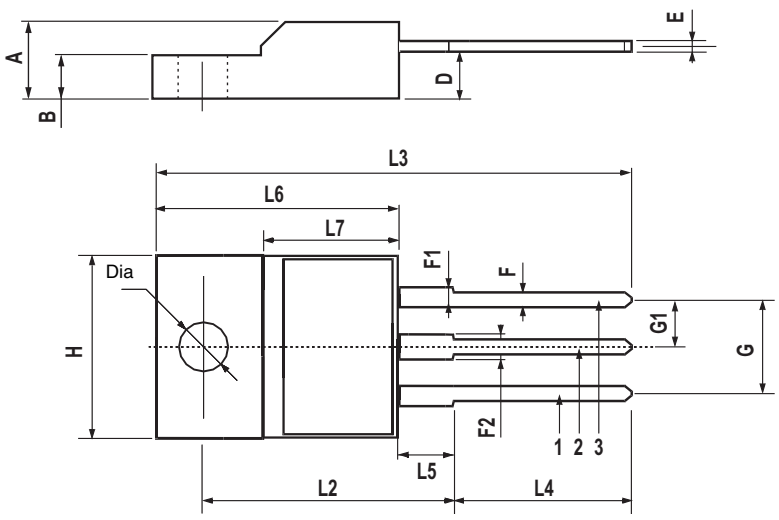
1. Fast electronic switch
2. Non-inductive resistor

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-220FP mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126



5 Revision history

Table 5. Document revision history

Date	Revision	Changes
04-Oct-2007	1	First release

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