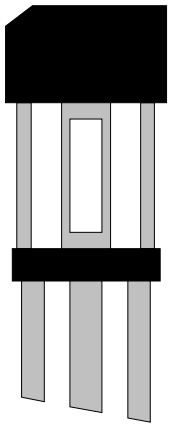
Programmable True Power On Hall Sensor TLE4980C

Features



PSSO3-9

- TPO True Power On functionality
- Mono-cell chopped Hall system
- TIM Twisted Independent Mounting
- Dynamic self-calibrating algorithm
- End-of-line programmable switching points
- TC of back-bias magnet programmable
- High sensitivity and high stability of the magnetic switching points
- High resistance to mechanical stress
- Digital output signal (voltage interface)
- Short-circuit protection
- Module style package with two 4.7 nF integrated capacitors

General information:
The TLE4980C is an active Hall sensor ideally suited for camshaft applications. Its basic function is to map either a tooth or a notch into a unique electrical output state. It has an electrical trimming option for post-fabrication trimming in order to achieve true power on capability even in the case of production spreads such as different magnetic configurations or misalignment. An additional self-calibration module has been implemented to achieve optimum accuracy during normal running operation. It comes in a three-pin package for the supply voltage and an open drain output.

Functional description:
The basic operation of the TLE4980C is to map a „high positive“ magnetic field (tooth) into a “low” electrical output signal and to map a „low positive“ magnetic field (notch) into a “high” electrical output. Optionally the other output polarity can be chosen by programming the PROM. A magnetic field is considered as positive if the North Pole of a magnet shows towards the rear side of the IC housing. Since it seems that also backbias-reduced magnetic configurations still show significant flux densities in one distinct direction the circuit will be optimised for one flux direction in order to provide an optimal signal to noise behaviour.
For understanding the operation of the TLE4980C three different modes have to be considered: Initial operation after power up: This mode will be referred to as „initial mode“. Operation following the initialisation before having full information about the target wheel: This mode will be referred to as “precalibrated mode”. Normal operation with running target wheel: This mode will be referred to as „calibrated mode“.

Initial mode:
The magnetic information is derived from a chopped Hall amplifier. The threshold information comes from a PROM-register that may be programmed at any time, but only once (no EEPROM). The magnetic information is compared against the threshold and the output state is set correspondingly. Some hysteresis is introduced in order to avoid false switching due to noise.
In case that there is no PROM-value available (PROM has not been programmed before) the chip starts an auto-search for the actual magnetic value. The initial threshold value is set to this magnetic value. This feature can be used to find a TPO-value for providing correct programming information to the chip simply by setting the chip in front of a well-defined static target. In this case a moving target wheel is not necessary.
In case there is a PROM value available, the open drain output will be turned on or off by comparing the magnetic field against the pre-programmed value.
During rotation of the target wheel a self-calibration procedure is started in the background. The IC memorises magnetic field values for adjusting the threshold to an optimum value. The exact way of threshold adjustment is described in more detail in the precalibrated mode. Once the IC has sufficient information for improving the accuracy (typically after 2-3 teeth) the device threshold value is adjusted and the device is switched into the precalibrated mode.

Precalibrated mode:
In the precalibrated mode the IC permanently monitors the magnetic signal. To say it in more detail, it searches for minimum (caused by a notch) and maximum (caused by a tooth) values in the signal. Once the IC has found a pair of min / max values it calculates the optimum threshold level and adjusts the system offset in such a way, that the switching occurs on this level. The threshold adjustment is limited to increments of approx. 1,5mT per calibration in order to avoid totally wrong information caused by large signal disturbances (EMC-events or similar). The optimum threshold level may differ depending on the target wheel. For example, for regular gearwheels the magnetic signal

is close to a sinusoid and the optimum threshold value can be considered as 50% value, which is the mean value between minimum and maximum signal. For camshaft wheels an optimum threshold may be at a different percent-value in order to have minimum phase error over airgap variations. See fig.4 for definition of this dynamic switching level.
In case that the initial PROM-value does not lead to a switching of the IC because it is slightly out of the signal range the IC nevertheless does its switch value correction in the background. After having corrected for a sufficient amount the IC will start its output switching. The output switching includes some hysteresis in order to avoid false switching.
If the IC has not been programmed yet, it uses the default 50% value between the minimum and the maximum as switching level.

Calibrated mode:
After a certain number of switching events (64) the accuracy is considered to be quite high. At this time the chip is switched into an averaging mode (= calibrated mode) where only minor threshold corrections are allowed. In this mode a period of 32 switching events is taken to find the absolute minimum and maximum within this period. Threshold calculation is done with these minimum and maximum. A filter algorithm is implemented, which ensures that the threshold will only be updated, if the adjustment value calculated shows in the same direction over the last four consecutive periods. Every new calculated adjustment value that shows in the same direction causes an immediate update of the threshold value. If the direction of the calculated adjustment value changes, there must be again four consecutive adjustment values in the same direction for another update of the threshold value. Additionally there is an activation level implemented, allowing the threshold to be adjusted only if a certain amount (normally bigger than 1LSB) of adjustment is calculated. The threshold correction per cycle is limited to 1 LSB. The purpose of this strategy is to avoid larger offset deviations due to singular events. Also irregularities of the target wheel are cancelled out, since the minimum and maximum values are derived over at least one full revolution of the wheel. The output switching is done at the threshold level without visible hysteresis in order to achieve maximum accuracy. Nevertheless the chip has some internal protection mechanisms in order to avoid multiple switching due to noise.

Changing the mode:
Every time after power up the chip is reset into the initial mode. Subsequent modes (precalibrated, calibrated) are entered consequently as described before. In addition, two plausibility checks are implemented in order to enable some self-recovery strategy in case of unexpected events.
First, there is a watchdog, which checks for switching of the sensor at a certain lower speed limit. If for 12 seconds there is no switching at the output, the chip is reset into the initial mode.
Second, the IC checks if there is signal activity seen by the digital logic and at the same time there is no switching at the output. If the digital circuitry expects that there should have been 4 switching events and actually no switching has occurred at the output, the IC is reset into the initial mode.

Reset:
There are several conditions, which can lead to a reset condition. For the IC behaviour we have to distinguish between a “output hold mode”, a “long reset”, a “short reset” and a “software reset”.

Output hold mode:
This operating mode means that the output is held in the actual state and there is no reset on the digital part performed. This state will be released after the IC reaches his normal operation condition again and goes back into the operating mode he was before.
The following conditions lead to the output hold mode:

- A drop in the supply voltage to a value less than 2.4V but higher than 2.0V for a time not longer than 1µs .. 2µs.

Long reset:
This reset means a total reset of the analogue as well as for the digital part of the IC. The output is forced to its default state (“high”). This condition remains for less than 1ms. After this time the IC is assumed to run in a stable condition and enters the initial mode where the output represents the state of the target wheel (PROM value).
The following conditions lead to a long reset:

- Power-on condition.
- Low supply voltage: drop of the supply voltage to values less than 2.4V for a time longer than 1µs .. 2µs or drop of the supply voltage to values less than 2.0V.

Short reset:
This reset means a reset of the digital circuitry. The output memorizes the state he had before the reset. This condition remains for approx. 1µs. After that time the chip is brought into the initial mode (output stays “high” for approx. 200µs for an untrimmed IC). Then the output is released again and represents the state of the target wheel (PROM value).
The following conditions lead to a short reset:

- Watchdog overflow: If there is no switching at the output for more than 12 seconds.
- If there are four min- or max-events found without a switching event at the output

Software reset:
This reset can be performed in the testmode through the serial-interface. The IC output is then used as data output for the serial interface.
The following condition lead to a software reset:

- There is a reset applied through the serial Interface

Table 1 shows an overview over the behaviour of the output under certain conditions.

	Unprogrammed		Programmed	
	Noninverted	inverted	Noninverted	Inverted
output hold mode	Q_{n-1}	-	Q_{n-1}	Q_{n-1}
long reset	High	-	High	High
short reset	High	-	normal TPO	inverted TPO
initial mode	high (self calibration)	-	normal TPO	inverted TPO
precalibrated mode	Normal	-	Normal	Inverted
calibrated mode	Normal	-	Normal	Inverted

Q_{n-1} … state of output before a reset occurs
normal TPO … “low” if $B>B_{TPO}$; “high” if $B<B_{TPO}$
inverted TPO … “high” if $B>B_{TPO}$; “low” if $B<B_{TPO}$
normal … “low” if $B>B_{Threshold}$; “high” if $B<B_{Threshold}$
inverted … “high” if $B>B_{Threshold}$; “low” if $B<B_{Threshold}$

Table1: Output behaviour under certain conditions

Hysteresis concept:
There are two different hysteresis concepts implemented in the IC.
The first one is called *visible hysteresis*, meaning that the output switching levels are changed between two distinct values (depending on the direction of the magnetic field during a switching event), whenever a certain amount of the magnetic field has been passing through after the last switching event. The *visible hysteresis* is used in the initial mode. See fig.1 for more details.
The second form of hysteresis is called *hidden hysteresis*. This means, that one cannot observe a hysteresis from outside. If the value of the switching level does not change, the output always switches at the same level. But inside the IC there are two distinct levels close above and below the switching level, which are used to arm the output. In other words if the value of the magnetic field crosses the lower of this hysteresis levels, then the output will be able to switch if the field crosses the switching level. After this switching event the output will be disabled until the value of the magnetic field crosses one of the two hysteresis levels. If it crosses the upper hysteresis level, then the output will be armed again and can switch if the magnetic field crosses the switching level. On the other hand, if the magnetic field does not reach the upper hysteresis level, but the lower hysteresis level will be crossed again after a switching event, then the output is allowed to switch, so that no tooth will be lost. But please notice that this causes an additional phase error. The *hidden hysteresis* is used in the precalibrated and calibrated mode. For more details see fig.2

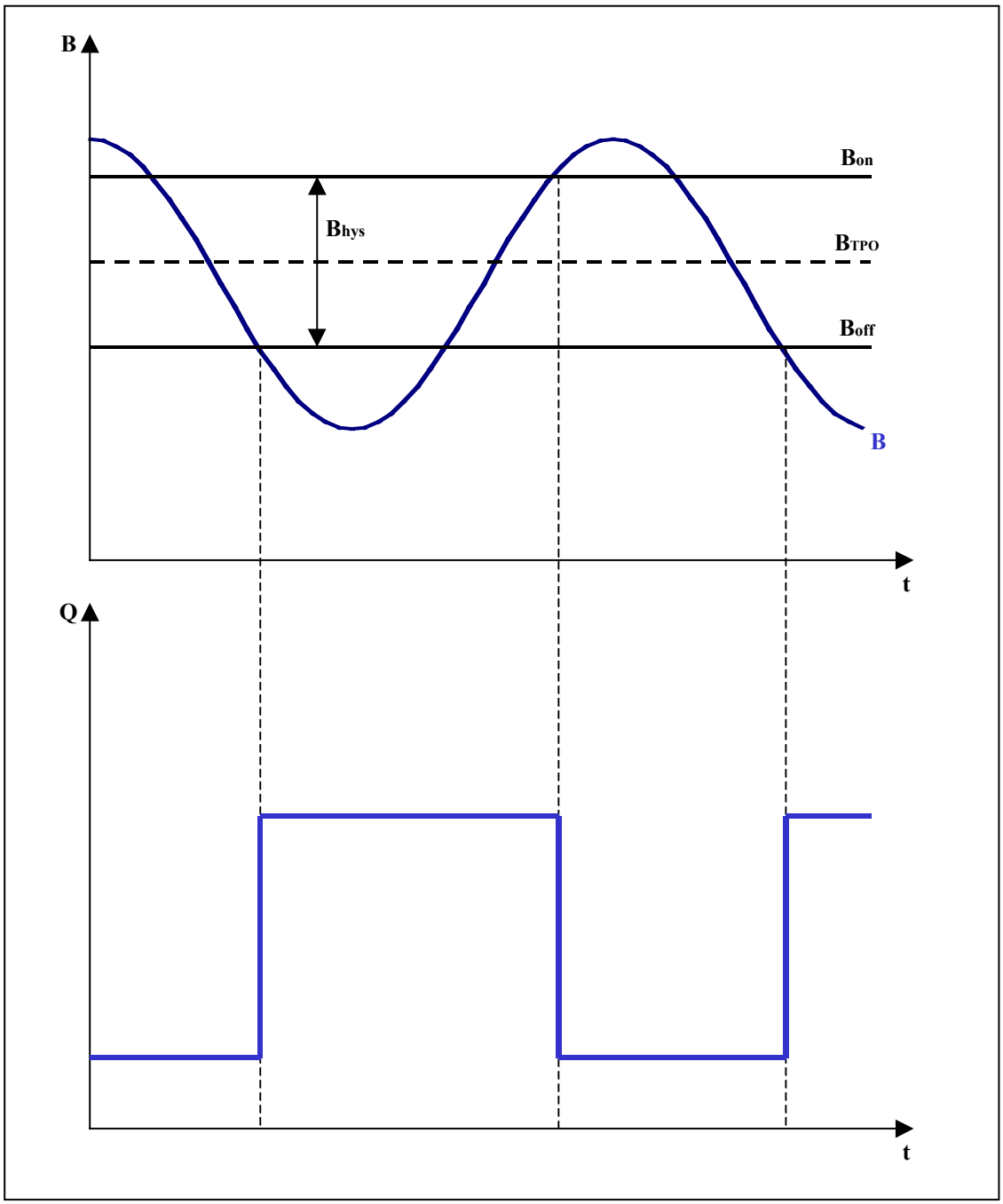


Fig. 1: Visible hysteresis (Initial mode)

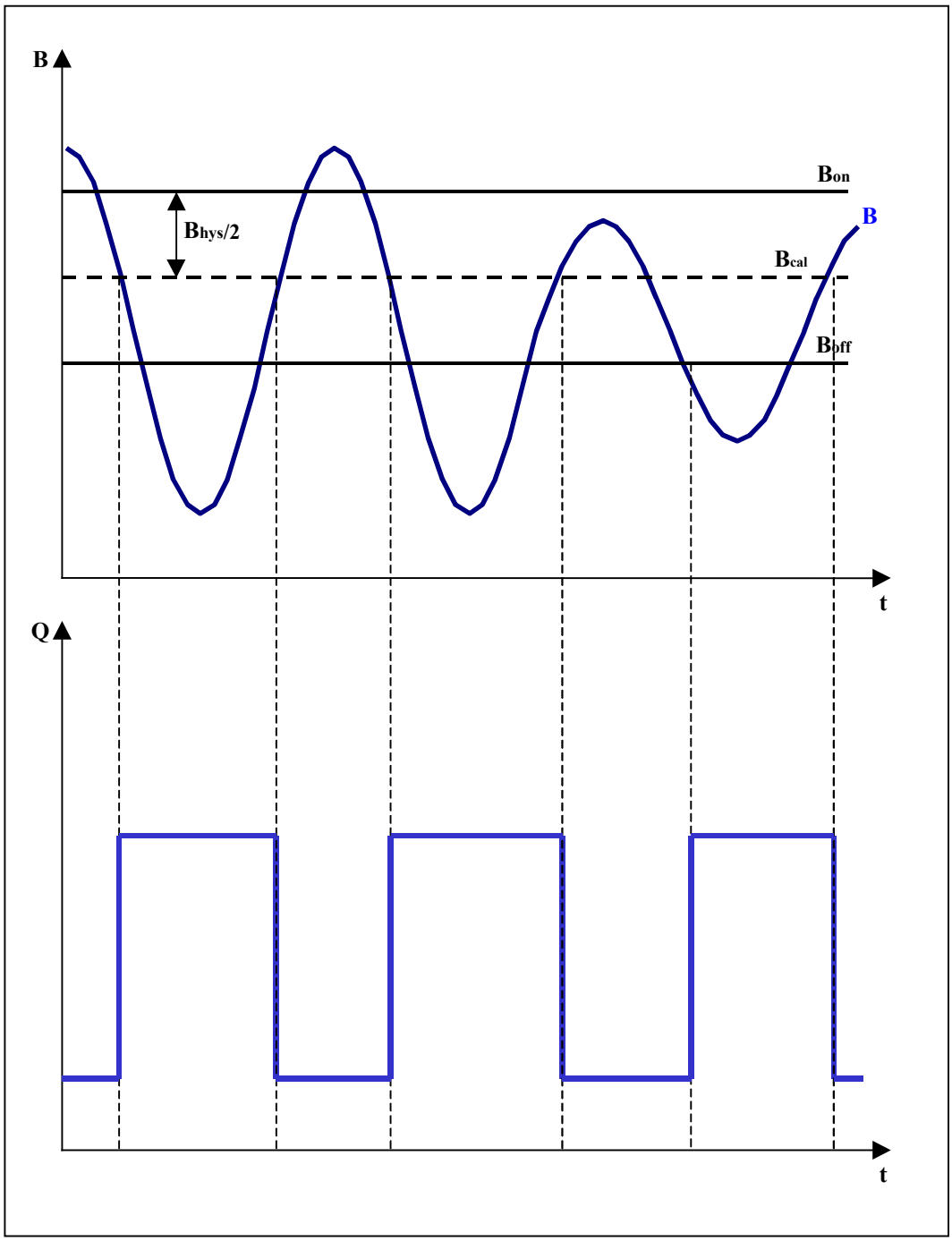


Fig. 2: Hidden hysteresis (precalibrated and calibrated mode)

Block diagram:
The block diagram is shown in fig.3. The IC consists of a spinning Hall probe (monocell in the centre of the chip) with a chopped preamplifier. Next there is a summing node for threshold level adjustment. The threshold switching is actually done in the main comparator at a signal level of „0“. This means, that the whole signal is shifted by this summing node in that way, that the desired switching level occurs at zero. This adjusted signal is fed into an A/D-converter. The converter feeds a digital calibration logic. This logic monitors the digitised signal by looking for minimum and maximum values and also calculates correction values for threshold adjustment. The static switching level is simply done by fetching a digital value out of a PROM. The dynamic switching level is done by calculating a weighted average of min and max value. For 50% weighting factors are equal, for other values weighting factors are different. For example, a factor of approximately 67% can be achieved by doubling the weight of the max value. Generally speaking, a threshold level of $B_{cal} = B_{min} + (B_{max} - B_{min}) * k_0$ can be achieved by multiplying max with the switching level k_0 and min with $(1-k_0)$.

Serial interface:
The serial interface is used to program the chip. At the same time it can be used to provide special settings and to read out several internal registers status bits. The interface description consists of a physical layer and a logical layer. The physical layer describes format, timing and voltage information, whereas the logical layer describes the available commands and the meaning of bits, words and addresses.

Physical interface layer:
The data transmission is done over the VS-pin, which generates input information and clock timing, and the out-pin Q, which delivers the output data. Generally the interface function is disabled; this means, that in normal operation including normal supply distortion the interface is not active and therefore the chip operates in its normal way. A special initialisation sequence must be performed to enter the interface mode that is also referred to as “testmode”. For an untrimmed chip (this is a chip which has not been programmed yet) the initialisation sequence is quite simple: For a short time after power on or reset the chip monitors the output signal. The internal logic brings the output into a high impedance state, which will be a logical “high” caused by the external pull-up resistor. If now the chip sees a logical “low” (for at least 1ms), which is an output voltage lower than 0.3V, the chip enters the testmode. For programmed chips this initialisation procedure is not possible. Instead a second initialisation mechanism has been implemented which is always valid. This means, that using this mechanism the chip will always enter the test mode even in normal operation. The test mode will be disabled after the IC has been programmed. Since you have to be in test mode while programming the IC, you can read out the programmed values as long as you do not leave the test mode.
The initialisation procedure for this second mode is as follows: Whenever the output signal is “low” the external supply has to be set to more than 7V (nom. 7.5V). Whenever the output signal is ”high” the external supply has to be set to less than 5V (nom. 4.5V). This has to be done for at least 5 consecutive periods. The delay between the output signal and the modulated supply signal must not exceed fourty periods of the internal

clock (less than 20µs delay). Any disturbance in this sequence will terminate the initialisation procedure. After having successfully finished the initialisation the chip enters the testmode and data transmission can be started.
Data transmission: Serial transmission is done in words (LSB first). A logical „1“ is represented by a long (2/3 of one period) „high“ voltage level (higher than 5V) on the supply followed by a short (1/3 of one period) „low“ voltage level (lower than 5V), whereas a logical „0“ is represented by a short „high“ level on the supply followed by a long „low“ level. At the same time this high/low voltage combination, which forms in fact a bit, acts as a serial interface clock which clocks out logical high / low values on the output. We recommend a period length of around 100µs per bit. See fig.5 for a more detailed timing diagram. End of word is indicated by a long (we recommend longer than 200µs, first 30µs should be higher than 5V and the rest lower than 5V) „low” supply. Please note, that for communicating 13 bits of data 14 VS-pulses are necessary. If more than 14 input bits are transmitted the output bits are irrelevant (transmission buffer empty) whereas the input bits remain valid and start overwriting the previously transmitted bits. In any case the last 14 transmitted bits are interpreted as transmitted data word (13 bits) + 1 stop bit. End of communication is signalled by a long „high“ voltage level. A new communication has to be set up by a new initialisation sequence.

Programming the PROM:
One possibility for programming the static threshold value is to run the IC on a testbench (or in the car), to wait until the IC has reached the calibrated mode and then simply to issue the copy commands, which transfers the calibrated threshold value into the PROM.
Use the following procedure for this type of programming:
1) Apply an oscillating magnetic field with a suitable offset (Notice that for unfused devices this offset lies in the middle of the maximum and minimum value of the magnetic field).
2) Enter the testmode with the second procedure described in the chapter “Physical interface layer”.
3) Wait until the IC has reached the calibration mode.
4) Choose a k-factor and supply 12V to the output.
5) Write the three following bit-combinations via the serial interface:

$$1010k_6k_5k_4k_3k_2k_1k_0I1$$
$$1011k_6k_5k_4k_3k_2k_1k_0I1$$
$$1011111111111$$

Here k_i indicate the 7bits of the k-factor (k_6 … MSB and k_0 … LSB) in dual-code.
This means: 1100000 is equal to k_0=0.75 and 1010010 is equal to k_0=0.65.
The bit I is the so called Inverting bit, which determines either the output switches inverse to the applied magnetic field (I=”0”) or not (I=”1”).
6) Leave the testmode by writing a long “high” voltage level.

A second form of programming the static threshold value is to bring the IC in front of a target, which delivers a static magnetic field with a suitable strength and perform a

power on by forcing the output to a low state for at least 1ms. This brings the chip in the testmode and he starts immediately a successive approximation and adjusts the value of the offset-DAC to the switching level that corresponds to the field strength.
Use the following procedure for this type of programming:

1) Apply a static magnetic field with a suitable strength.
2) Enter the testmode with the first procedure described in the chapter “Physical interface layer”.
3) Wait until the IC has made the successive approximation and reached the right level for the offset-DAC (at least 10 periods of the internal clock frequency after releasing the output).
4) Choose a k-factor and supply 12V to the output.
5) Write the three following bit-combinations via the serial interface:

$$1010k_6k_5k_4k_3k_2k_1k_0I1$$
$$1011k_6k_5k_4k_3k_2k_1k_0I1$$
$$1011111111111$$

   Here again k_i indicate the 7bits of the k-factor (k_6 … MSB and k_0 … LSB) in dual-code. This means: 1100000 is equal to k_0=0.75 and 1010010 is equal to k_0=0.65. The bit I is the so called Inverting bit, which determines either the output switches inverse to the applied magnetic field (I=”0”) or not (I=”1”).
6) Leave the testmode by writing a long “high” voltage level.

It has to be noted that the chip has increased power dissipation during programming for blowing the fuses. The additional power is taken out of the output.

Overvoltage protection:
The process used for production has a breakthrough voltage of approximately 27.5V. The chip can be brought into breakthrough without damage if the breakthrough power (current) is limited to a certain value. Usually destruction is caused by overheating the device. Therefore for short pulses the breakthrough power can be higher than for long duration stress. For example for load dump conditions an external protection resistor of 200 Ω is recommended in 12V-systems and 50 Ω in 5V-systems.

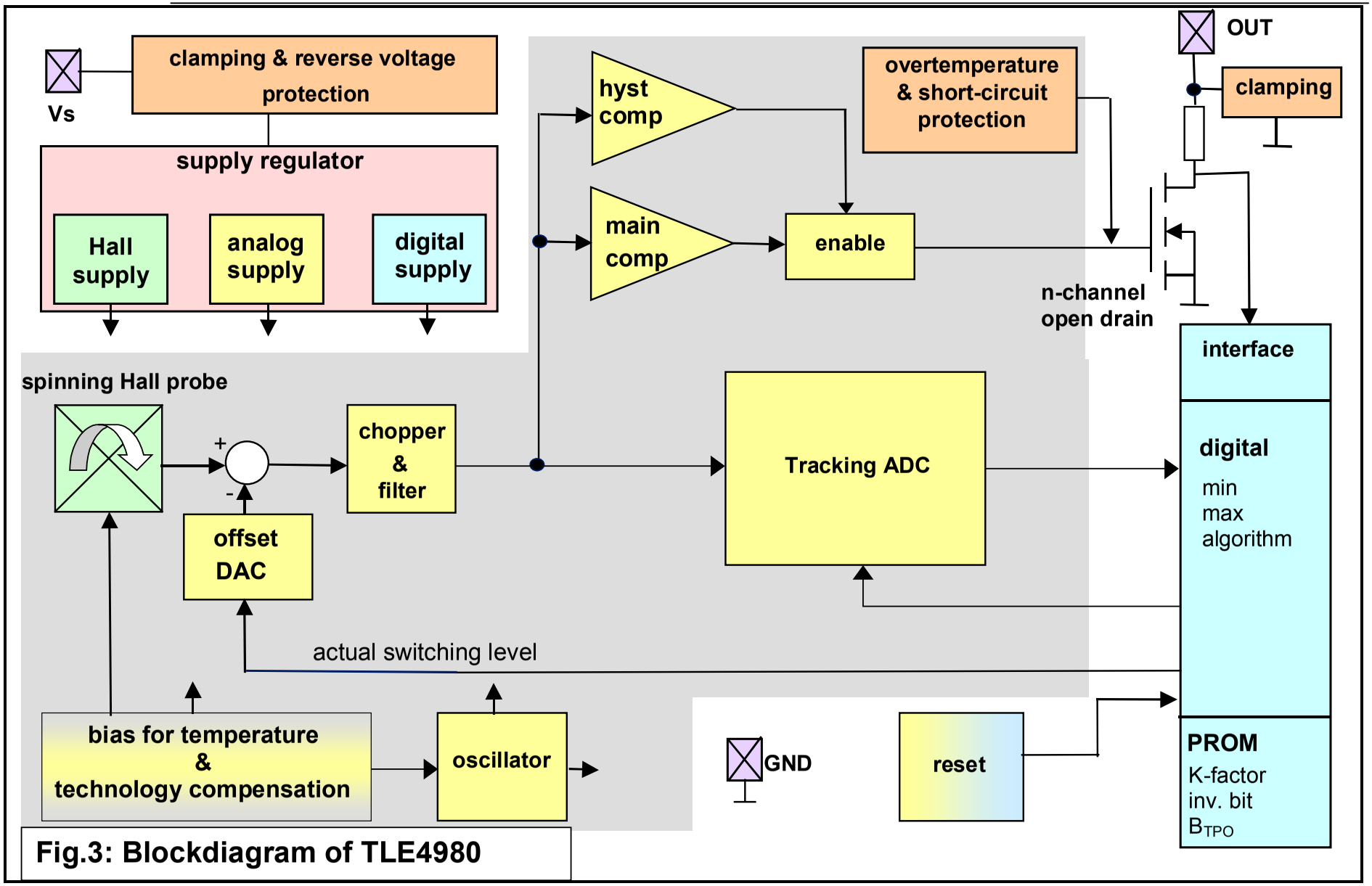


Fig.3: Blockdiagram of TLE4980

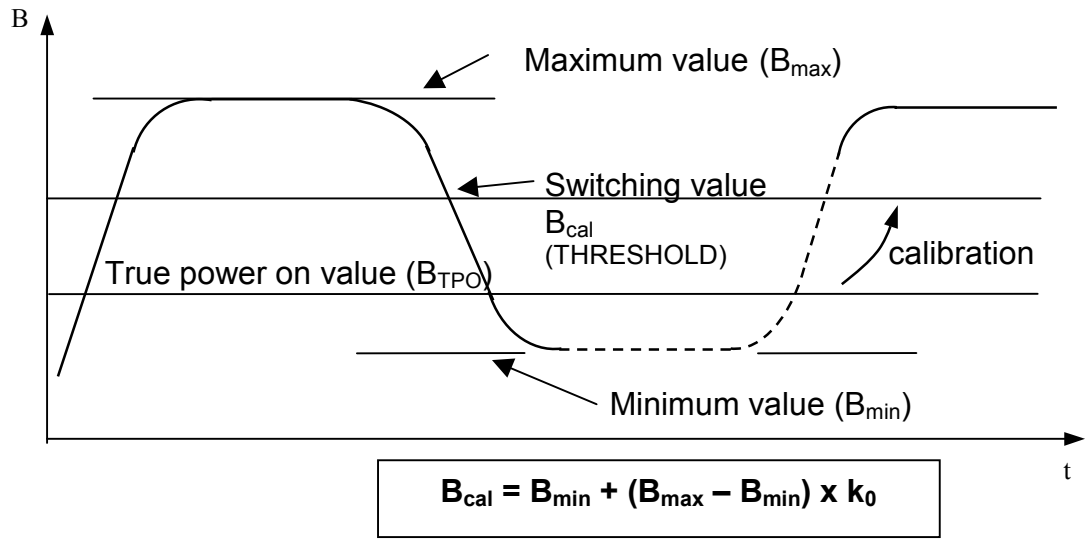


Fig. 4: Dynamic threshold value

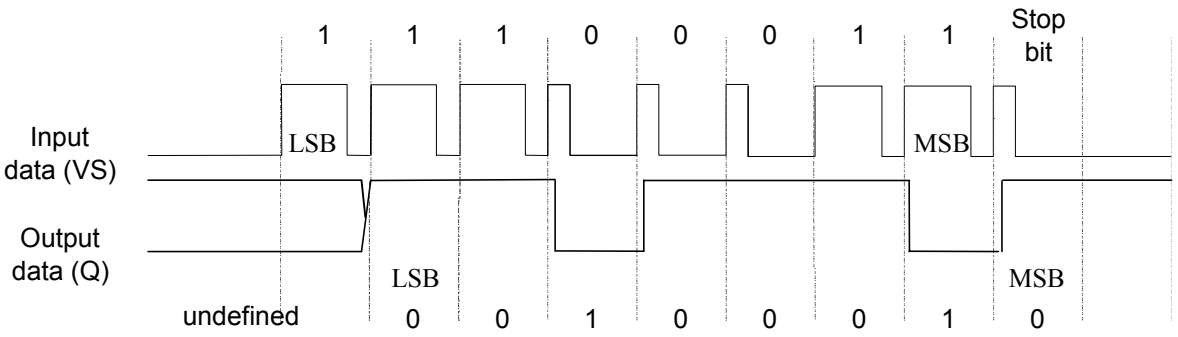


Fig. 5: Serial protocol

Absolute maximum ratings:

Symbol	Name					
		min	typ	max	Unit	Note
V_S	supply voltage	-18		18	V	
		-24		24	V	1h with R_{series}>=200Ω[1]
		-26		26	V	5min with R_{series}>=200Ω[1]
V_Q	output OFF voltage	-0.3		18	V	
		-0.3		24	V	1h with R_{load}>=500Ω
		-0.3		26	V	5min with R_{load}>=500Ω
		-1.0			V	1h
V_Q	output ON voltage			16	V	current internal limited by short circuit protection (72h@T_A<40°C)
				18	V	current internal limited by short circuit protection (1h@T_A<40°C)
				24	V	current internal limited by short circuit protection (1min@T_A<40°C)
I_Q	continuous output current	-50		50	mA	
T_j	junction temperature	-40			°C	
				155	°C	2000h (not additive)
				165	°C	1000h (not additive)
				175	°C	168h (not additive)
				195	°C	3x1h (additive to the other life times)
R_{thJA}	thermal resistance junction-air			190	K/W	
T_S	storage temperature	-50		150	°C	
B	magnetic field induction				mT	no limit
V_{ESD}	ESD - protection			±4	kV	according to standard EIA/Jesd22-A114-B HBM

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] Accumulated life time

Electro Magnetic Compatibility - *(values depend on R_{series})*

Ref. ISO 7637-1; test circuit of Figure 6;

ΔB_{PP} = 2mT (ideal sinusoidal signal); V_S=13.5V ± 0.5V, f_B= 1kHz; T= 25°C; R_{series} ≥ 200Ω;

Parameter	Symbol	Level/typ	Status
testpulse 1	V_{LD}	IV / -100V	C[1]
testpulse 2		IV / 100V	C
testpulse 3a		IV / -150V	A
		IV / -300V	C
testpulse 3b		IV / 100V	A
testpulse 4		-	-[2]
testpulse 5a		II / 55V	C
		III / 70V	E

Ref. ISO 7637-3; test circuit of Figure 6;

ΔB_{PP} = 2mT (ideal sinusoidal signal); V_S=13.5V ± 0.5V, f_B= 1kHz; T= 25°C; R_{series} ≥ 200Ω;

No.	Parameter	Symbol	Level/typ	Status
1.2.2	testpulse 1	V_{LD}	- / -	-
	testpulse 2		- / -	-
	testpulse 3a		IV / -300V	A
	testpulse 3b		IV / 300V	A

Note: Test criteria for status C: No missing pulse no additional pulse on the IC output signal.
Test criteria for status A: Same plus duty cycle and jitter in the specification limits.
Test criteria for status E: destroyed

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] According to 7637-1 the supply switched „OFF“ for t=200ms. For battery „ON“ is valid status „A“
[2] According to 7637-1 the test voltage for test pulse 4 is 12V ± 0.2V

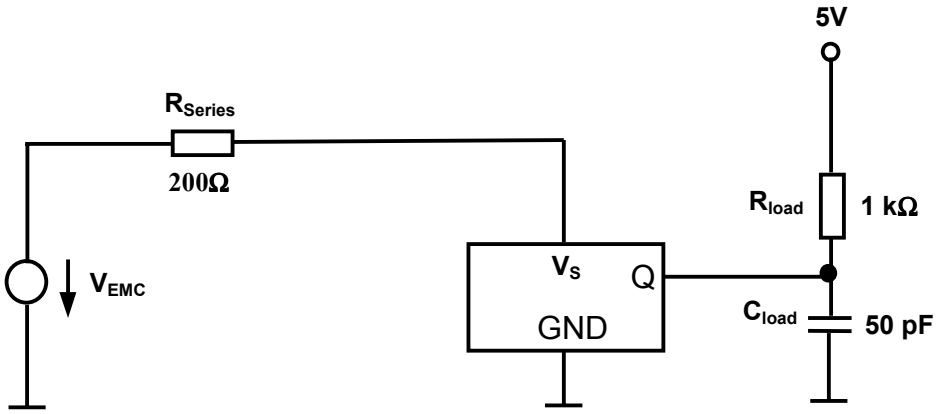


Figure 6: Testcircuit for EMC-tests

Operating range:

Symbol	Name				
		min	max	Unit	Note
V_S	operating supply voltage	3.3	18	V	Continuous
			24	V	1h with R_{series}>=200Ω; extended limits for parameters in characteristics
T_j	operating junction temperature	-40		°C	
			155	°C	2000h (not additive)
			165	°C	1000h (not additive)
			175	°C	168h (not additive)
T_{cal}	trimming temperature	15	35	°C	V_S=5/12V
I_Q	continuous output ON current	0	20	mA	V_{Qmax}=0.5V
V_Q	continuous output OFF voltage	-0.3	18	V	Continuous
		-18	24	V	1h with R_{load}>=500Ω
f_B	magnetic signal switching frequency	0	5	kHz	Measured between two rising edges of the magnetic signal
t_{edge}	rise time of magnetic edge	85		µs	The edge of the magnetic signal is not allowed to rise faster than this value (otherwise the tracking ADC of the chip is not able to follow)
B	linear magnetic range	0	120	mT	
B_{BB}	magnetic preinduction	20	70	mT	
B_{TPO}	true power on range	20	75	mT	hysteresis not included (typ. B_{Hys}=1.0mT)
$B_{AC\ TPO}$	magnetic signal swing for TPO-function	5.8	50.0	mT_{pp}	B_{TPO}=44mT; B_{HYS} = 0.75mT[1]
B_{AC_cal}	magnetic signal swing for calibrated mode	3	50	mT_{pp}	
B_{over}	magnetic overshoot		10	% of B_{AC_cal}	
k_0	adjustment range of switching level	10	90	% of B_{AC_cal}	The switching point in calibrated mode is determined by: $B_{cal} = B_{min} + (B_{max} – B_{min}) * k_0$
TC_{magnet}	magnet temperature coefficient	-1200	-500	ppm/K	

[1] Encapsulated devices with B_{TPO}=44mT and B_{HYS}=0.5mT show minimum value of $5mT_{pp}$

AC/DC characteristics:

Symbol	Name					
		min	typ	max	Unit	Note
V_{Qsat}	output saturation voltage		0.25	0.5	V	I_Q = 20mA
I_{Qleak}	output leakage current		0.1	10	µA	V_Q = 18V
I_{Qshort}	current limit for short circuit protection	30	50	80	mA	
T_{prot}	junction temperature limit for output protection	195	210	230	°C	
t_{rise} [1]	output rise time	4	11	17	µs	V_{LOAD} = 4,5..24V R_{LOAD} = 1kΩ C_{LOAD} = 4,7nF included in package
t_{fall} [2]	output fall time		0.4	0.8	µs	V_{LOAD} = 4,5..24V R_{LOAD} = 1kΩ C_{LOAD} = 4,7nF included in package
I_{SVmin}	supply current @ 3.5V		5.5	6.5	mA	V_S = 3.5V
I_S	supply current		5.6	7.5	mA	
I_{smax}	supply current @ 24V			8.0	mA	R_{series}>=200Ω
V_{Sclamp}	Clamping voltage V_S-Pin		27.5		V	1mA through clamping device
V_{Qclamp}	Clamping voltage Q-Pin		27.5		V	1mA through clamping device
t_{on}	power on time		0.56 [3]	1	ms	Time to achieve specified accuracy. During this time the output is locked [4]
			0.75 [5]		ms	
t_d [6]	delay time of output to magnetic edge	6	10	14	µs	Higher magnetic slopes and overshoots reduce t_d, because the signal is filtered internal. [7]
Δt_d	temperature drift of delay time of output to magnetic edge	-3		3	µs	not additional to t_d
t_{watch}	watchdog time		12		s	If there is no change at the output during this time a reset is performed.
n_{watch}	watchdog edges		4		-	If n_{watch} min or max-events have been found and there was no change at the output a reset is performed.

1 value of capacitor: 4.7nF±10% (excluded drift due to temperature); ceramic: X7R; maximum voltage: 100V
2 see footnote 1
3 trimmed IC
4 output is in high-state
5 untrimmed IC
6 measured at T_j = 25°C; represents the influence of the production spread (corresponds to the 3σ-value)
7 measured with a sinusoidal-field magnetic-field with an amplitude of 10mT and a frequency of 1kHz

Symbol	Name					
		min	typ	max	Unit	Note
f_{clk}	clock frequency for digital part		1.76		MHz	
$f_{chopper}$	clock frequency used by the chopper preamplifier		220		kHz	output jitter is not affected by the chopper frequency
Δk_0	resolution of switching level adjustment		0.8		%	
FSR_{ODAC}	full scale range of the offset-DAC	90	120	150	mT	
$FSR_{ODACtyp}$	full scale range of the offset-DAC	104	120	141	mT	T_j=25°C
B_{TPO_res}	resolution of threshold in TPO mode		0.12		mT	
ΔB_{TPO}	drift of B_{TPO}-point	-1.8		+3.2	mT	B_{TPO}=44mT[1]
ΔB_{AC_cal}	accuracy of threshold in calibration mode	-2		2	%	percentage of B_{cal}; B_{AC}=10mT_{pp} sinusoidal signal[2]; systematic deviation due to hysteresis in the filter algorithm of 1.5% at B_{AC}=10mT_{pp} not included;
B_{neff}	effective noise value of the magnetic switching points		33		µT	T_j = 25°C; The magnetic noise is normal distributed, nearly independent to frequency and without sampling noise or digital noise effects. The effective value corresponds to 1σ probability of normal distribution. Consequently a 3σ value corresponds to 0.3% probability of appearance.
			55	120	µT	Typical value corresponds to 1σ. Max value corresponds to 1σ values in the full temperature range and include technological spreads.

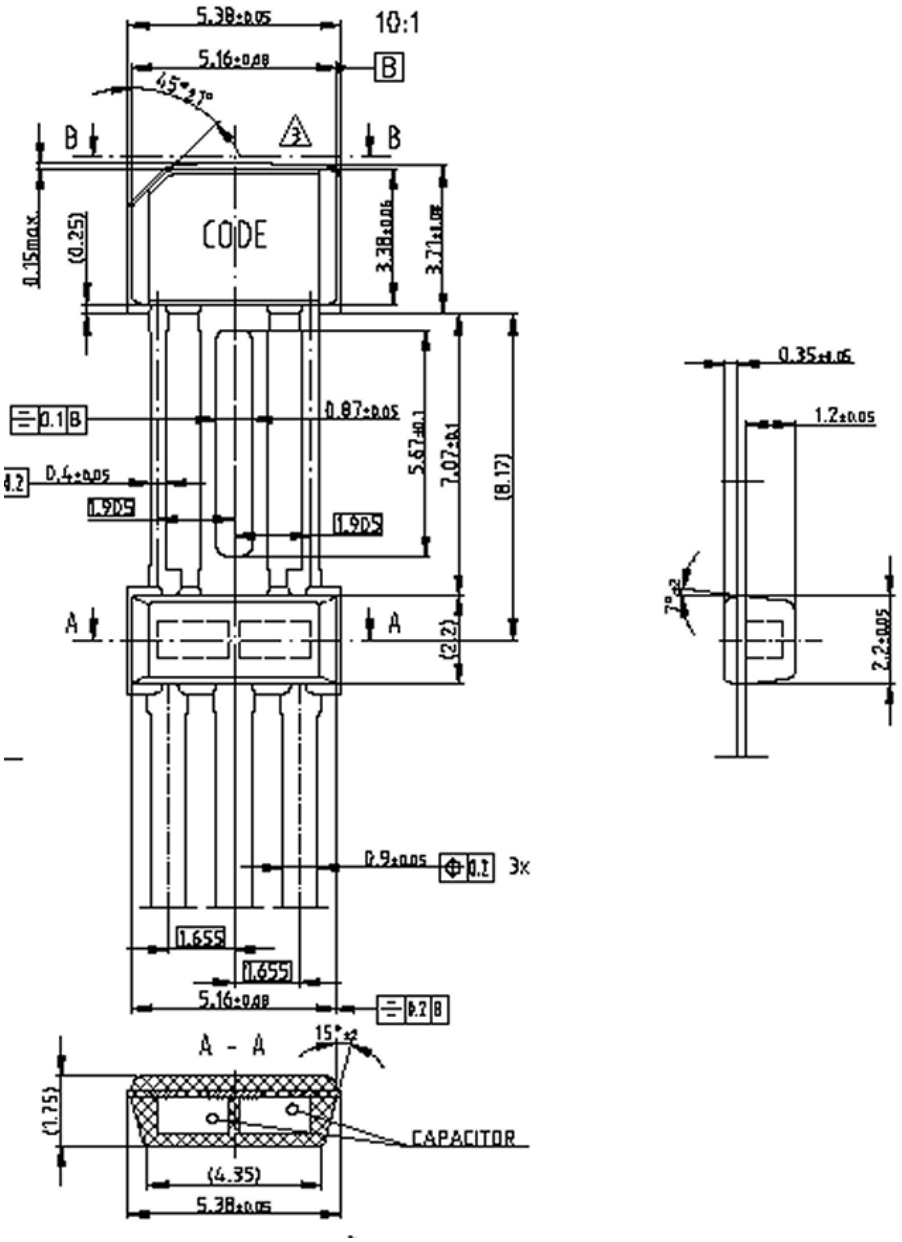
Note: The listed AC/DC and magnetic characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not other specified, typical characteristics apply at T_j = 25 °C and V_S = 12 V.

[1] This value shows the deviation from the programmed B_{TPO} value and its temperature coefficient. Included are the package-effect, the deviation from the adjusted temperature coefficient of the B_{TPO} point (resolution of the temperature coefficient and spread of the technologie) and the drift of the offset (over temperature and lifetime). Not included is the hysteresis in the initial mode.

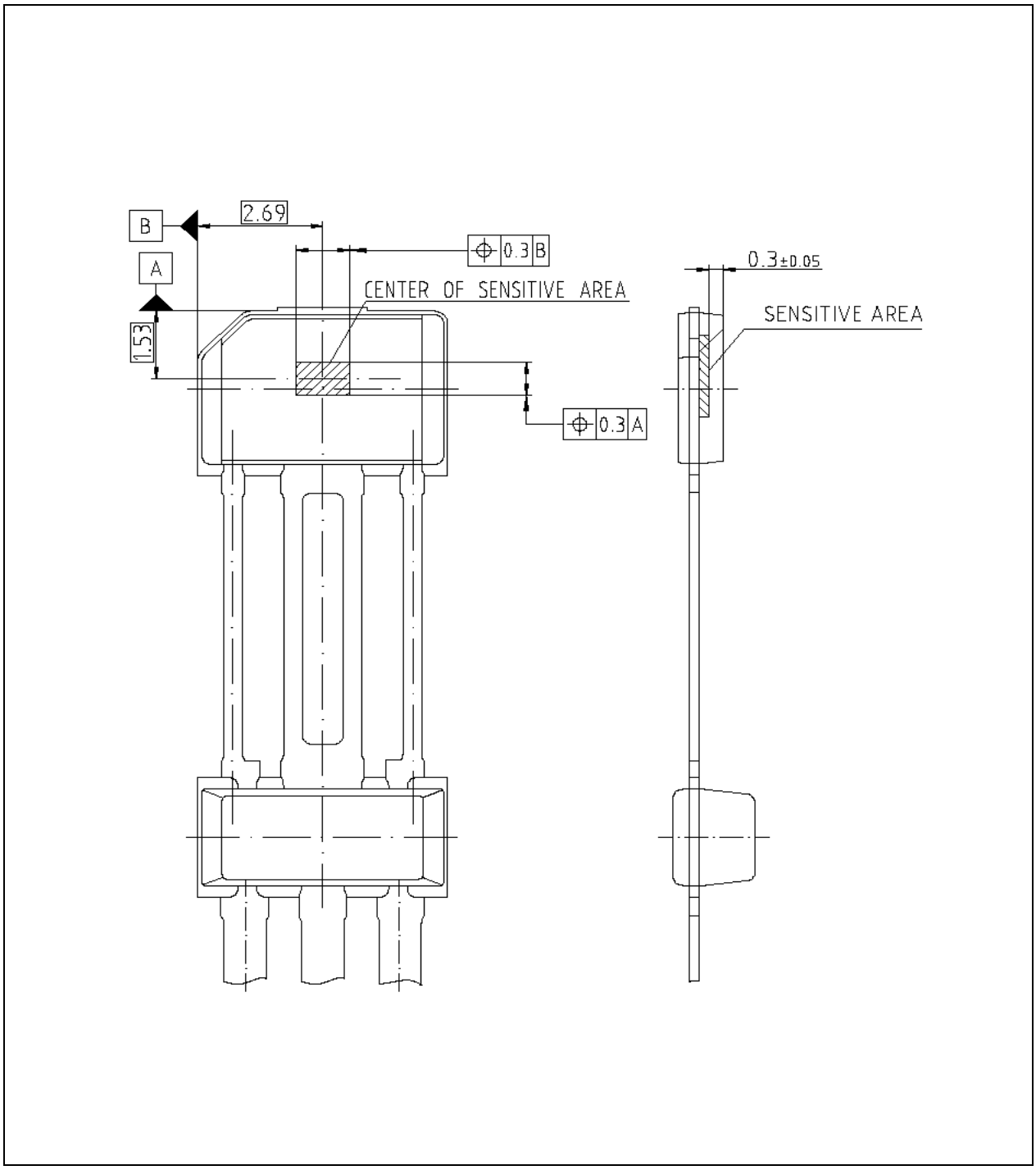
[2] bigger amplitudes of signal lead to smaller values of ΔB_{AC_cal}

Package Dimensions

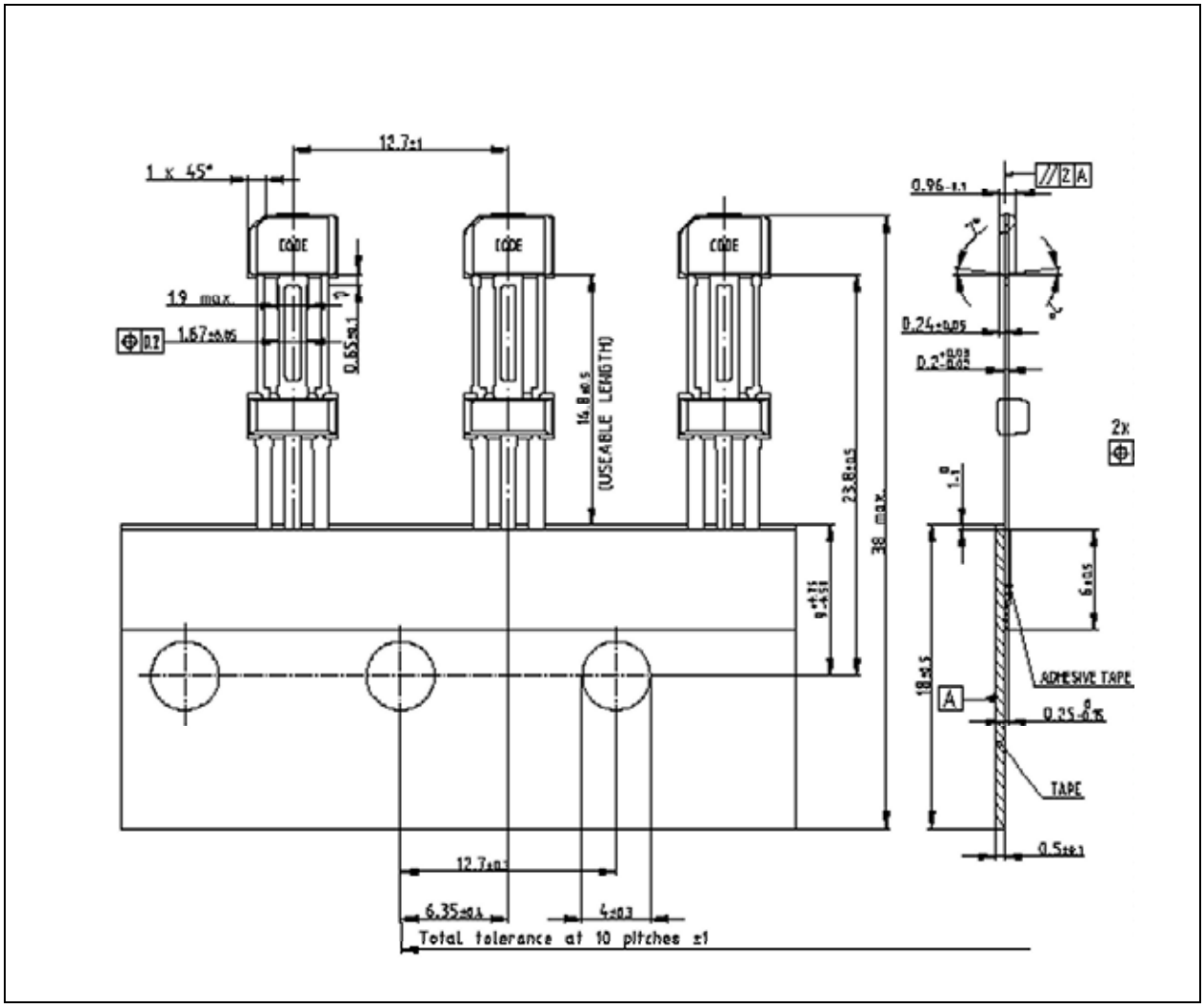
P-SSO 3-9
(**P**lastic **S**ingle **S**mall **O**utline)



Position of the Hall Element



Tape Loading Orientation



Pin Definitions and Function PSSO3-9

Pin	Symbol	Function
1	V_S	Supply Voltage
2	GND	Ground
3	Q	Open Drain Input

Appendix:

Calculation of mechanical errors:

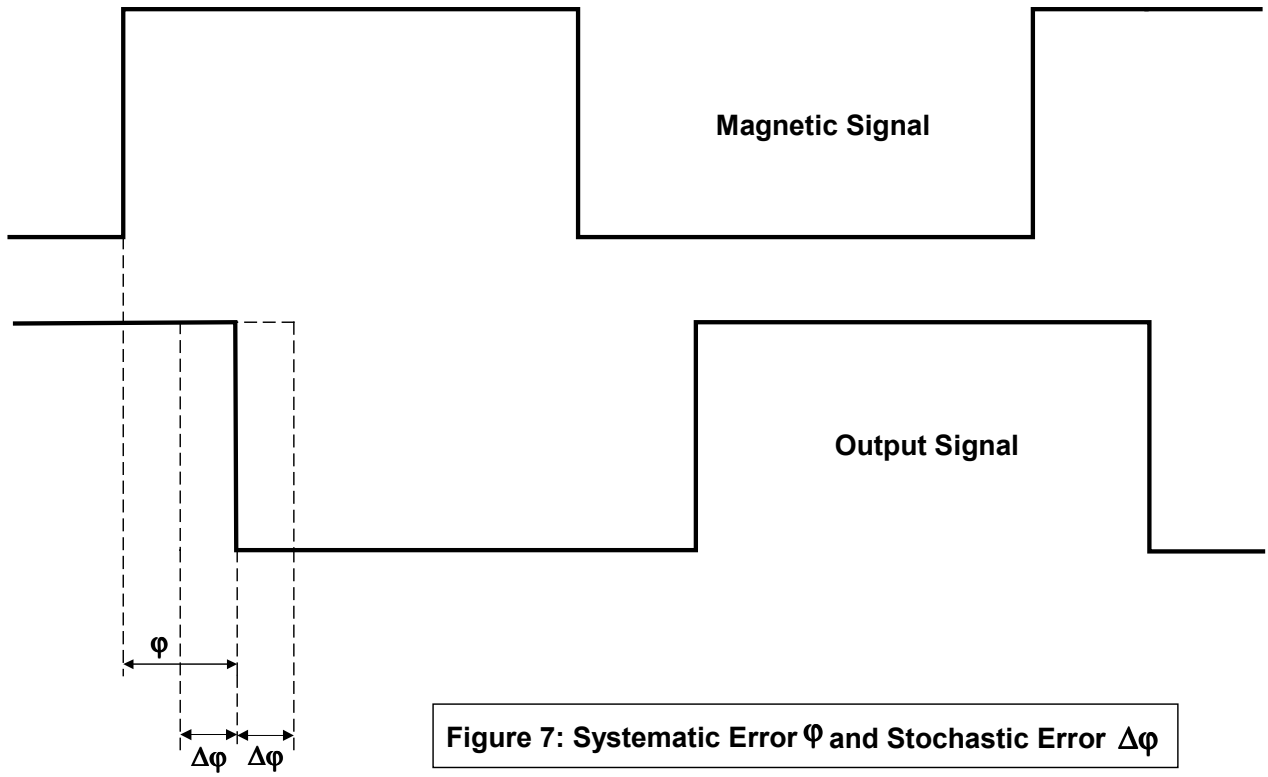


Figure 7: Systematic Error φ and Stochastic Error Δφ

Systematic Phase Error φ

The systematic error comes in because of the delay-time between the threshold point and the time when the output is switching. It can be calculated as follows:

$$\varphi = \frac{360° \bullet n}{60} \bullet t_d$$

φ ... systematic phase error in °
n ... speed of the camshaft-wheel in min^{-1}
t_d ... delay time (see specification) in *sec*

Stochastic Phase Error Δφ

The stochastic phase error includes the error due to the variation of the delay time with temperature and the error caused by the resolution of the threshold. It can be calculated in the following way:

$$\Delta\varphi_d = \frac{360° \bullet n}{60} \bullet \Delta t_d$$

$$\Delta\varphi_{cal} = \frac{\partial\varphi}{\partial B} \bullet \Delta B_{AC\_cal}$$

$\Delta\varphi_d$	...	stochastic phase error due to the variation of the delay time over temperature in °
$\Delta\varphi_{cal}$	...	stochastic phase error due to the resolution of the threshold value in °
n	...	speed of the camshaft wheel in *min*$^{-1}$
$\frac{\partial\varphi}{\partial B}$	...	inverse of the magnetic slope of the edge in °/*T*
Δt_d	...	variation of delay time over temperature in *sec*
ΔB_{AC_cal}	...	accuracy of the threshold in *T*

Jitter (Repeatability)

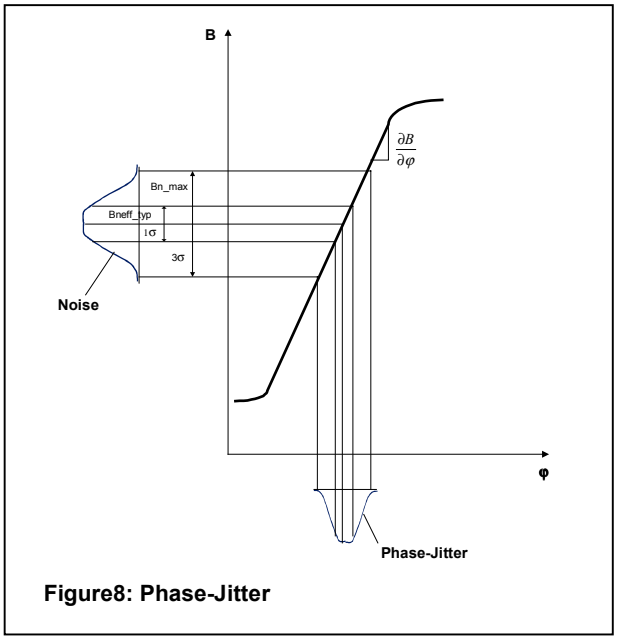


Figure8: Phase-Jitter

The phase jitter is normally caused by the analogue system noise. If there is an update of 1bit of the offset-DAC due to the algorithm, what could happen after a period of 16 teeth, then an additional step in the phase occurs (see description of the algorithm). This is not included in the following calculations. The noise is transformed through the slope of the magnetic edge into a phase error. The phase jitter is determined by the two formulas:

$$\varphi_{Jitter\_typ} = \frac{\partial\varphi}{\partial B} \bullet \left(B_{neff\_typ}\right)$$

$$\varphi_{Jitter\_\max} = \frac{\partial\varphi}{\partial B} \bullet \left(B_{n\_\max}\right)$$

φ_{Jitter_typ}	...	typical phase jitter at T=25°C in ° (1Sigma)
φ_{Jitter_max}	...	maximum phase jitter at T=170°C in ° (3Sigma)
$\frac{\partial\varphi}{\partial B}$	...	inverse of the magnetic slope of the edge in °/*T*
B_{neff_typ}	...	typical value of B_{neff} in *T* (1σ-value at T=25°C)
B_{n_max}	...	maximum value of B_n in *T* (3σ-value at T=170°C)

Example:

Assumption:
n = 3000 min^{-1}
t_d = 14 µs
Δt_d = ±3 µs
$\frac{\partial B}{\partial \varphi}$ = 1 mT/°
ΔB_{AC_cal} = ±0.2 mT (=2% of 10mT swing)
B_{neff_typ} = ±33 µT (1σ-value at T=25°C)
B_{n_max} = ±360 µT (3σ-value at T=170°C)

Calculation:

φ = 0.252°	...	systematic phase error
$\Delta\varphi_d$ = ±0.054°	...	stochastic phase error due to delay time variation
$\Delta\varphi_{cal}$ = ±0.2°	...	stochastic phase error due to accuracy of the threshold
φ_{Jitter_typ} = ±0.033°	...	typical phase jitter (1σ-value at T=25°C)
φ_{Jitter_max} = ±0.36°	...	maximum phase jitter (3σ-value at T=170°C)