STN1NK60ZL

N-channel 600 V, 10.4 Ω typ., 0.44 A SuperMESH™ Power MOSFET in a SOT-223 package

Datasheet - production data

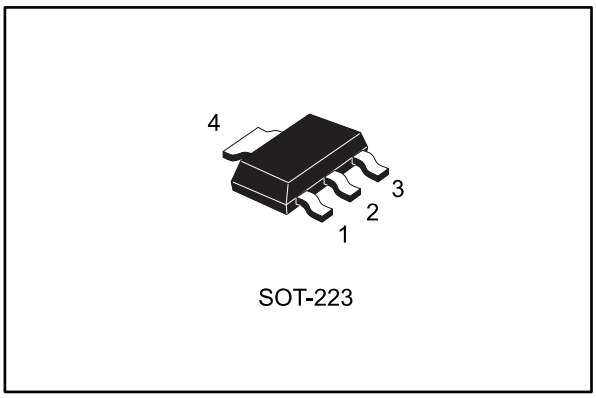
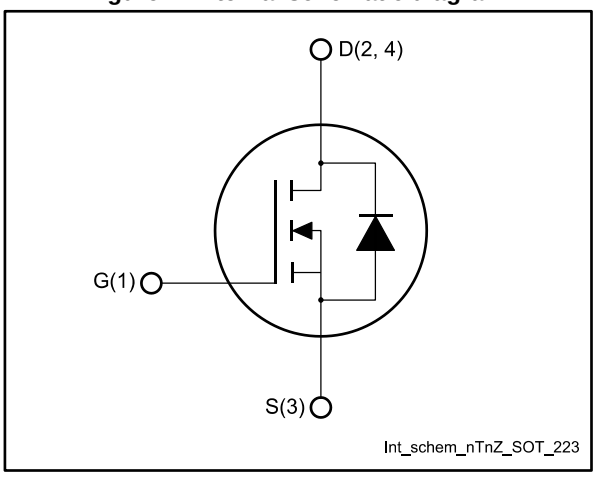


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STN1NK60ZL	600 V	15 Ω	0.44 A	3.3 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- ESD improved capability

Applications

- Switching applications

Description

This high voltage device is an N-channel Power MOSFET developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1: Device summary

Order code	Marking	Package	Packing
STN1NK60ZL	1NK60ZL	SOT-223	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_{amb} = 25 °C	0.44	A
I_D	Drain current (continuous) at T_{amb} = 100 °C	0.3	A
I_{DM}(1)	Drain current (pulsed)	1.8	A
P_{TOT}	Total dissipation at T_{amb} = 25 °C	3.3	W
dv/dt (2)	Peak diode recovery voltage slope	3	V/ns
T_j	Operating junction temperature range	- 55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)Pulse width limited by safe operating area.

(2)$I_{SD} \leq 0.3$ A, di/dt ≤ 200 A/µs, $V_{DD} = 80\%V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$(1)	Thermal resistance junction- ambient max	38	°C/W

Notes:

(1) When mounted on 1 inch² FR-4 board, 2 Oz Cu, t < 3 s

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	0.3	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	150	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	0.9	1.7	2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.25 A		10.4	15	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	-	125	-	pF
C_{oss}	Output capacitance		-	13	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 0.8 A V_{GS}= 10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	9.4	-	nC
Q_{gs}	Gate-source charge		-	0.8	-	nC
Q_{gd}	Gate-drain charge		-	4.5	-	nC

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 300 V, I_D = 0.4 A, R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*)	-	4.4	-	ns
t_r	Rise time		-	4	-	ns
$t_{d(off)}$	Turn-off delay time		-	18.4	-	ns
t_f	Fall time		-	41	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		0.44	A
I_{SDM}(1)	Source-drain current (pulsed)		-		1.8	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 0.44 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 0.8 A, di/dt = 100 A/µs,V_{DD} = 60 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	155		ns
Q_{rr}	Reverse recovery charge		-	232		nC
I_{RRM}	Reverse recovery current		-	3		A
t_{rr}	Reverse recovery time	I_{SD} = 0.8 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	186		ns
Q_{rr}	Reverse recovery charge		-	297		nC
I_{RRM}	Reverse recovery current		-	3.2		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

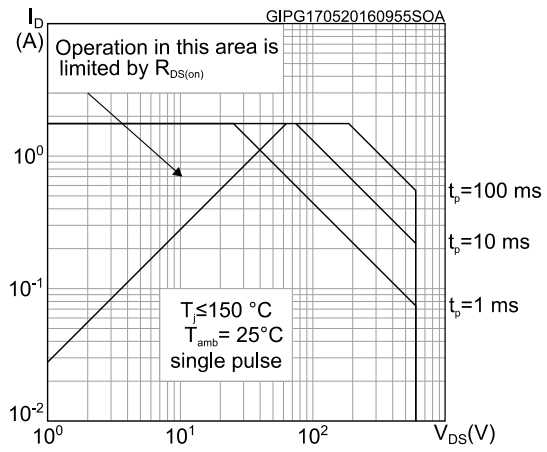


Figure 3: Thermal impedance

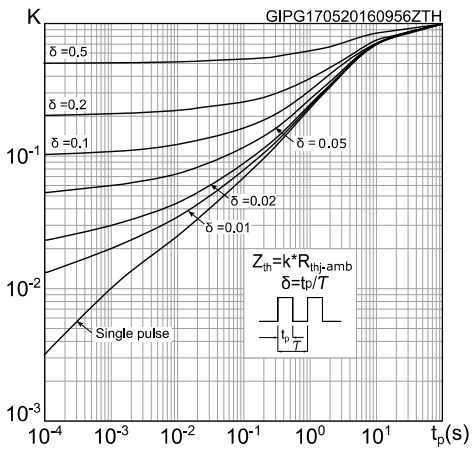


Figure 4: Output characteristics

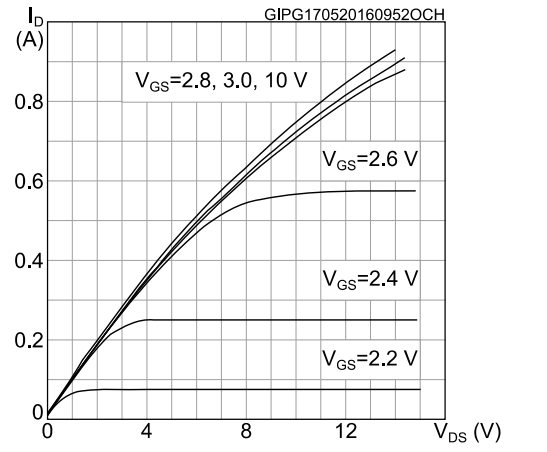


Figure 5: Transfer characteristics

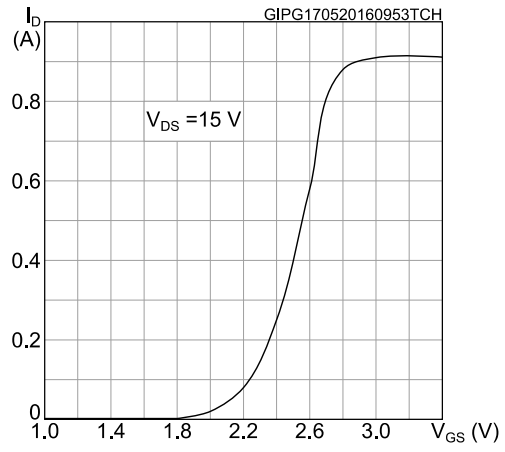


Figure 6: Gate charge vs gate-source voltage

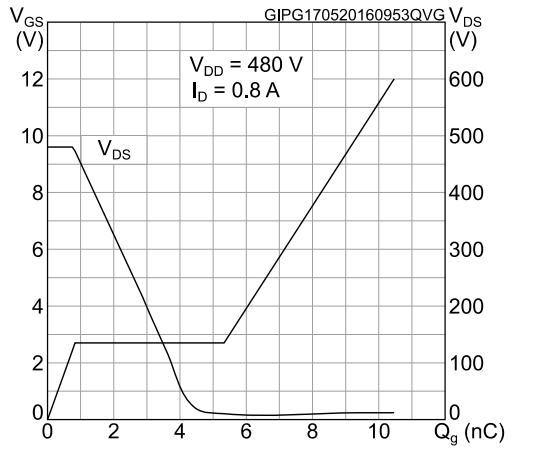


Figure 7: Static drain-source on-resistance

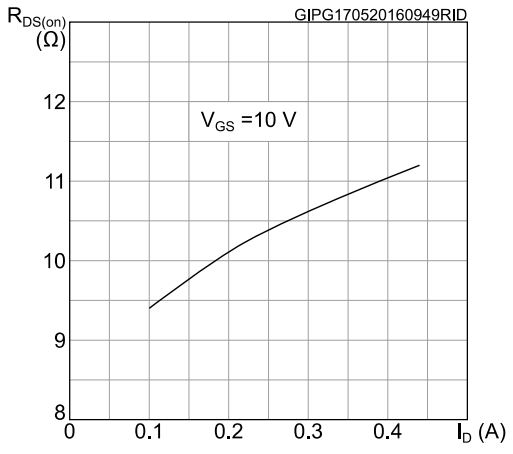


Figure 8: Capacitance variations

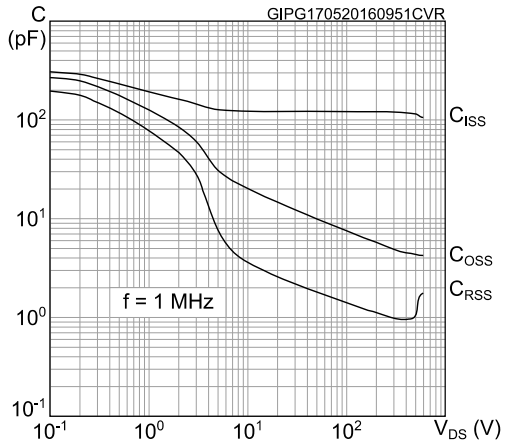


Figure 9: Normalized gate threshold voltage vs temperature

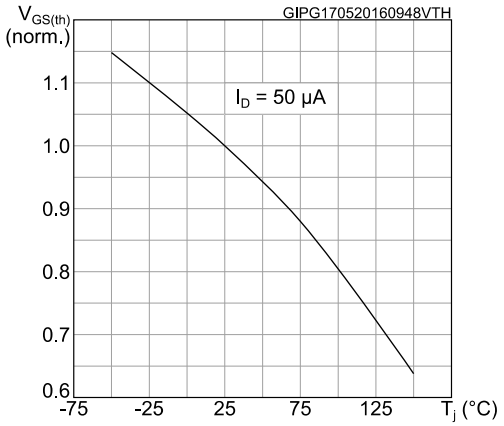


Figure 10: Normalized on-resistance vs temperature

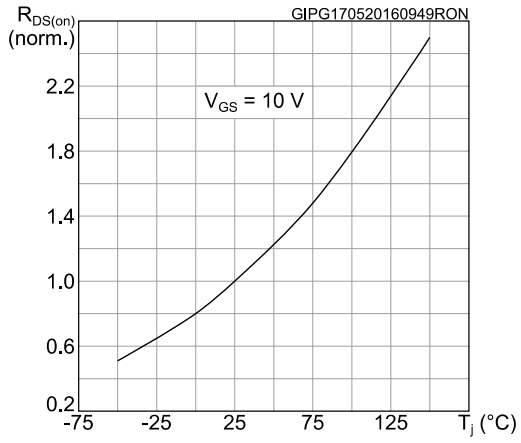


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

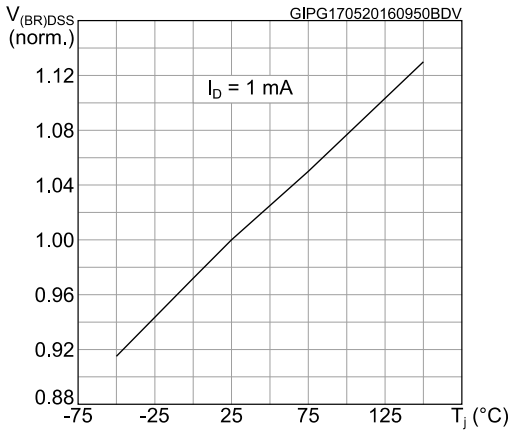


Figure 12: Maximum avalanche energy vs starting T_J

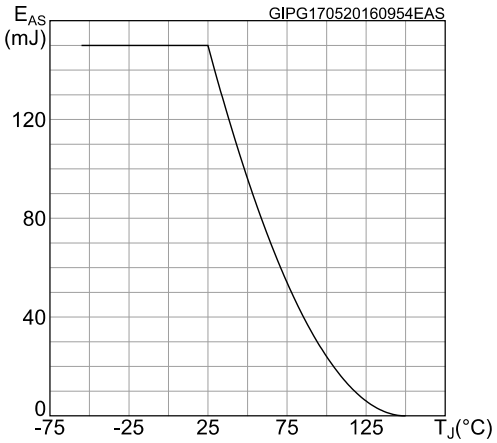
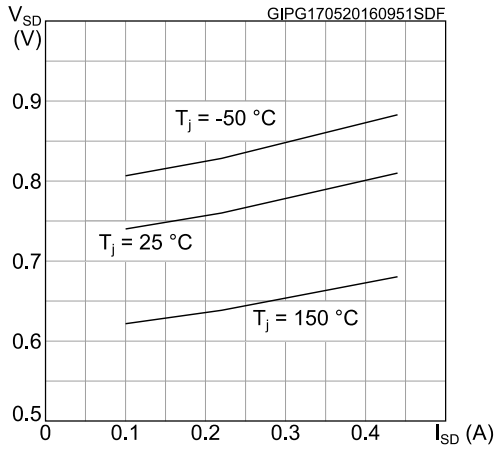


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Test circuit for resistive load switching times

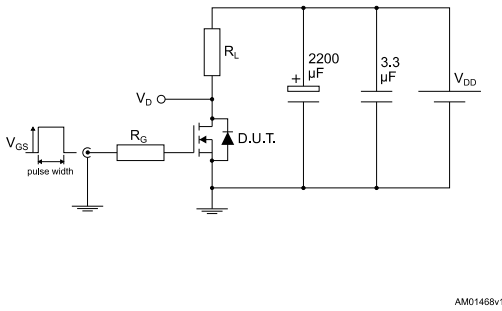


Figure 15: Test circuit for gate charge behavior

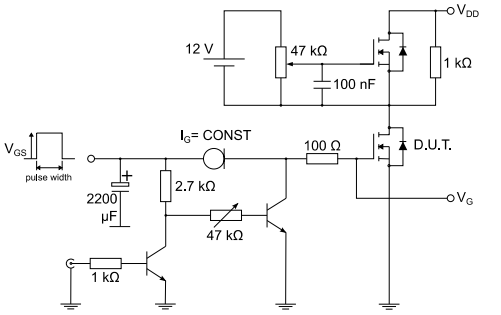


Figure 16: Test circuit for inductive load switching and diode recovery times

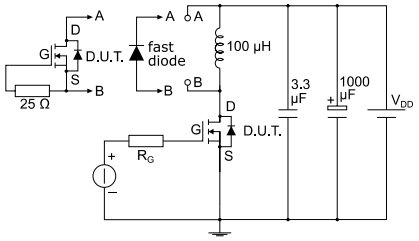


Figure 17: Unclamped inductive load test circuit

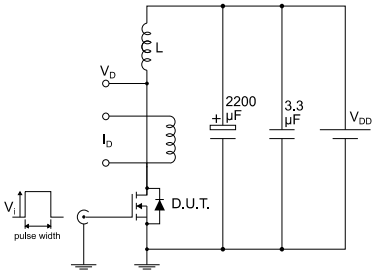


Figure 18: Unclamped inductive waveform

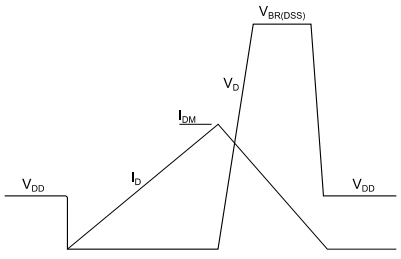
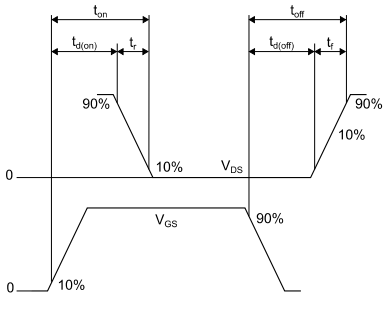


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 SOT-223 package information

Figure 20: SOT-223 package outline

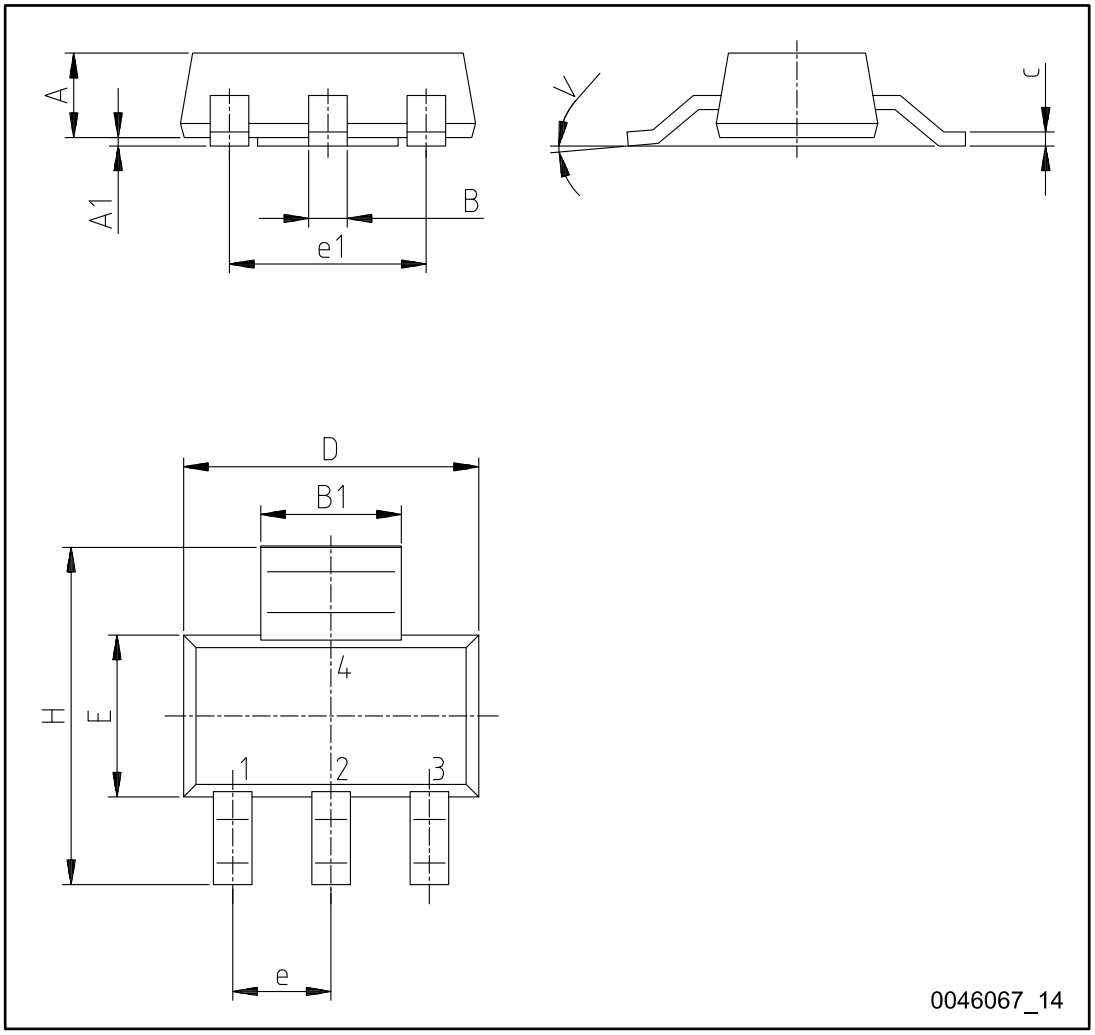
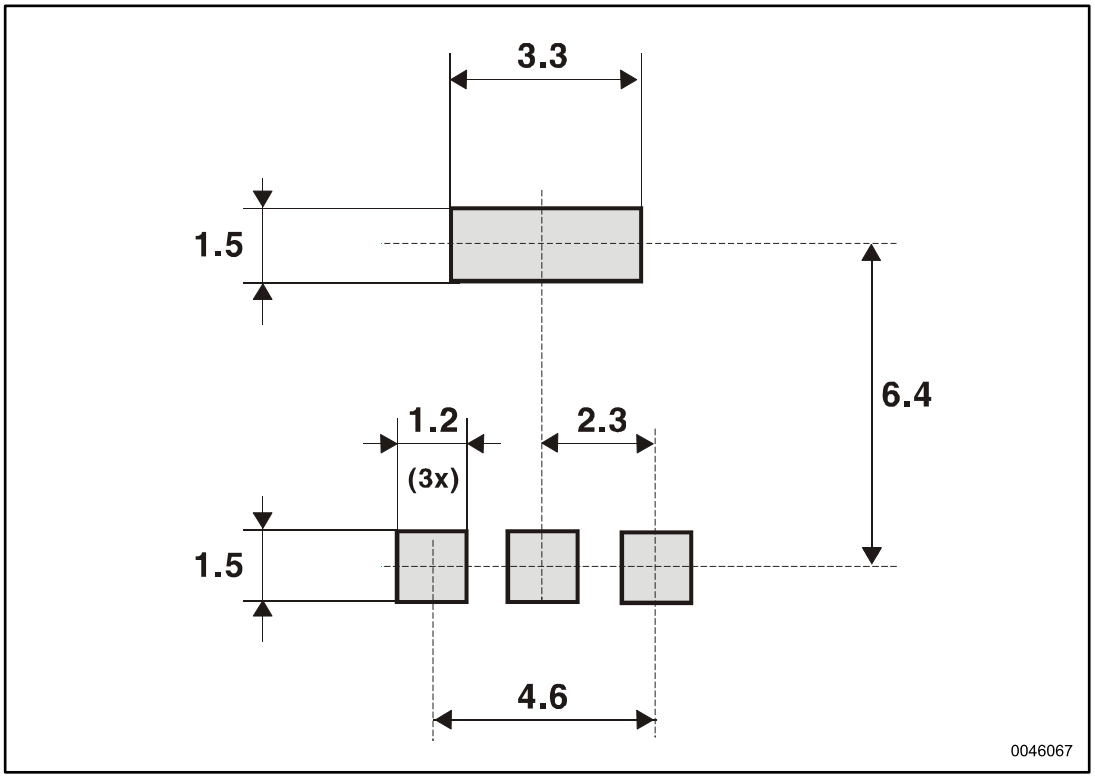


Table 9: SOT-223 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.8
A1	0.02		0.1
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7.0	7.3
V			10º

Figure 21: SOT-223 recommended footprint (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
12-Nov-2015	1	First release.
05-Dec-2016	2	Modified: features in cover page Modified *Table 2: "Absolute maximum ratings"*, *Table 3: "Thermal data"*, *Table 4: "Avalanche characteristics"*, *Table 5: "On/off-state"*, *Table 6: "Dynamic"*, *Table 7: "Switching times"* and *Table 8: "Source-drain diode"* Datasheet promoted from preliminary data to production data Modified *Section 3.1: "Electrical characteristics (curves)"* Minor text changes

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