

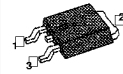
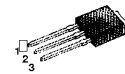
FEATURES

- ◆ Avalanche Rugged Technology
- ◆ Rugged Gate Oxide Technology
- ◆ Lower Input Capacitance
- ◆ Improved Gate Charge
- ◆ Extended Safe Operating Area
- ◆ Lower Leakage Current: 10 μ A (Max.) @ $V_{DS} = 400V$
- ◆ Low $R_{DS(ON)}$: 2.815 Ω (Typ.)

$$BV_{DSS} = 400 V$$

$$R_{DS(on)} = 3.6\Omega$$

$$I_D = 1.7 A$$

D-PAK**I-PAK**

1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	400	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	1.7	A
	Continuous Drain Current ($T_C=100^\circ C$)	1.1	
I_{DM}	Drain Current-Pulsed (1)	6	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (2)	116	mJ
I_{AR}	Avalanche Current (1)	1.7	A
E_{AR}	Repetitive Avalanche Energy (1)	2.6	mJ
dv/dt	Peak Diode Recovery dv/dt (3)	4.0	V/ns
P_D	Total Power Dissipation ($T_A=25^\circ C$) *	2.5	W
	Total Power Dissipation ($T_C=25^\circ C$)	26	W
	Linear Derating Factor	0.21	W/ $^\circ C$
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8. from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	4.76	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount).

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Rev. B

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV _{DSS}	Drain-Source Breakdown Voltage	400	--	--	V	V _{GS} =0V, I _D =250μA
ΔBV/ΔT _J	Breakdown Voltage Temp. Coeff.	--	0.53	--	V/°C	I _D =250μA See Fig 7
V _{GS(th)}	Gate Threshold Voltage	2.0	--	4.0	V	V _{DS} =5V, I _D =250μA
I _{GSS}	Gate-Source Leakage, Forward	--	--	100	nA	V _{GS} =30V
	Gate-Source Leakage, Reverse	--	--	-100		V _{GS} =-30V
I _{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	V _{DS} =400V
		--	--	100		V _{DS} =320V, T _C =125°C
R _{DS(on)}	Static Drain-Source On-State Resistance	--	--	3.6	Ω	V _{GS} =10V, I _D =0.85A (4)
g _{fs}	Forward Transconductance	--	1.10	--	Ŝ	V _{DS} =50V, I _D =0.85A (4)
C _{iss}	Input Capacitance	--	215	280	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz See Fig 5
C _{oss}	Output Capacitance	--	35	42		
C _{rss}	Reverse Transfer Capacitance	--	13	17		
t _{d(on)}	Turn-On Delay Time	--	11	30	ns	V _{DD} =200V, I _D =2A, R _G =24Ω See Fig 13 (4) (5)
t _r	Rise Time	--	15	40		
t _{d(off)}	Turn-Off Delay Time	--	38	90		
t _f	Fall Time	--	13	35		
Q _g	Total Gate Charge	--	10	14	nC	V _{DS} =320V, V _{GS} =10V, I _D =2A See Fig 6 & Fig 12 (4) (5)
Q _{gs}	Gate-Source Charge	--	1.8	--		
Q _{gd}	Gate-Drain (. Miller.) Charge	--	5.4	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I _S	Continuous Source Current	--	--	1.7	A	Integral reverse pn-diode in the MOSFET
I _{SM}	Pulsed-Source Current (1)	--	--	6		
V _{SD}	Diode Forward Voltage (4)	--	--	1.5	V	T _J =25°C, I _S =1.7A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	224	--	ns	T _J =25 °C, I _F =2A
Q _{rr}	Reverse Recovery Charge	--	0.87	--	μC	di _F /dt=100A/μs (4)

Notes;

- (1) Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- (2) L=70mH, I_{AS}=1.7A, V_{DD}=50V, R_G=27Ω, Starting T_J=25°C
- (3) I_{SD} ≤ 2A, di/dt ≤ 80A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J=25°C
- (4) Pulse Test: Pulse Width = 250μs, Duty Cycle ≤ 2%
- (5) Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

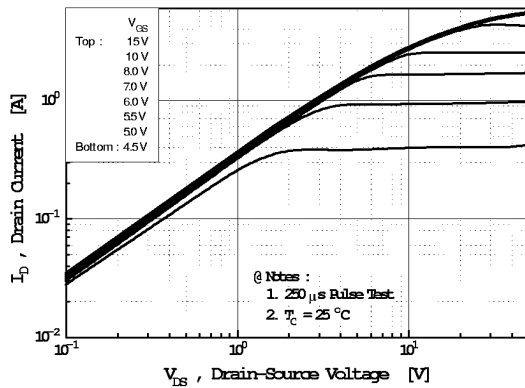


Fig 2. Transfer Characteristics

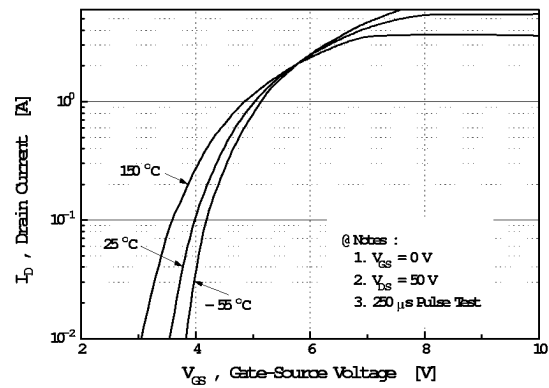


Fig 3. On-Resistance vs. Drain Current

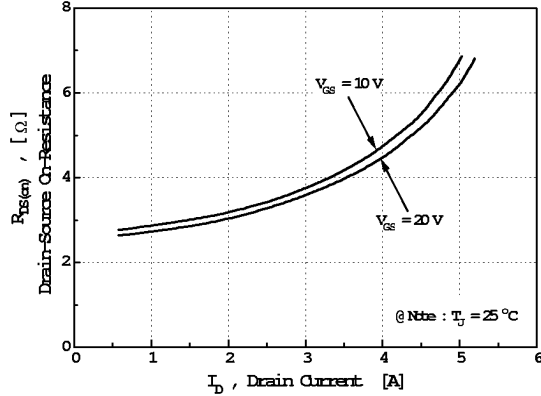


Fig 4. Source-Drain Diode Forward Voltage

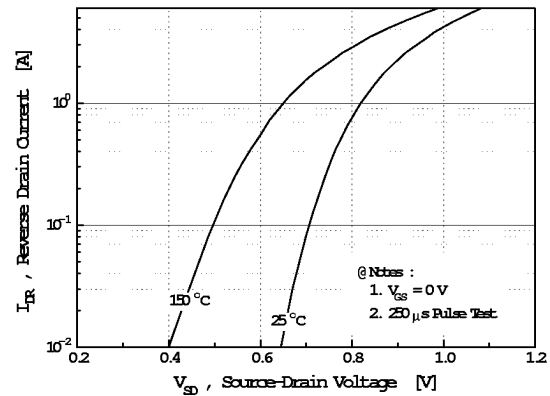


Fig 5. Capacitance vs. Drain-Source Voltage

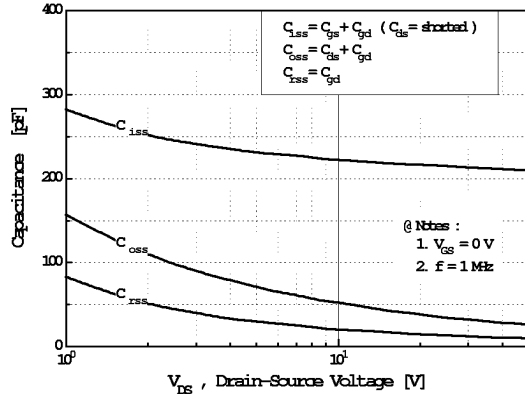


Fig 6. Gate Charge vs. Gate-Source Voltage

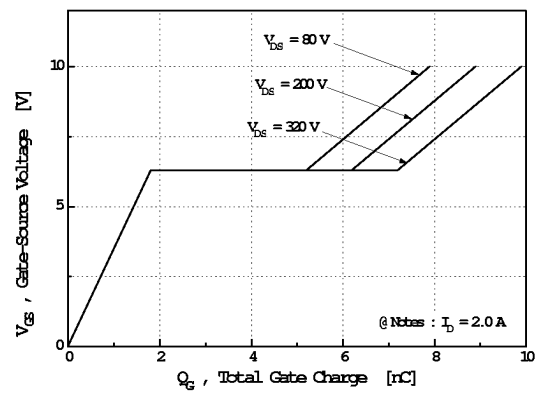


Fig 7. Breakdown Voltage vs. Temperature

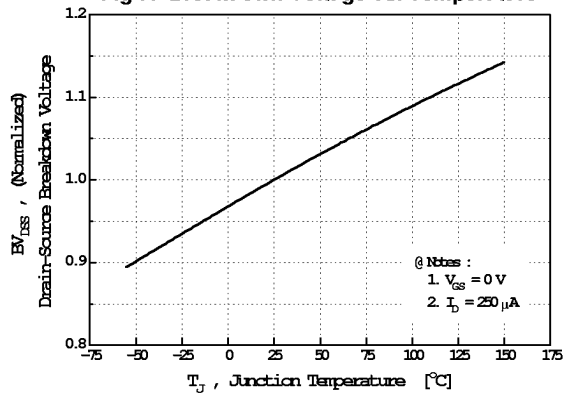


Fig 8. On-Resistance vs. Temperature

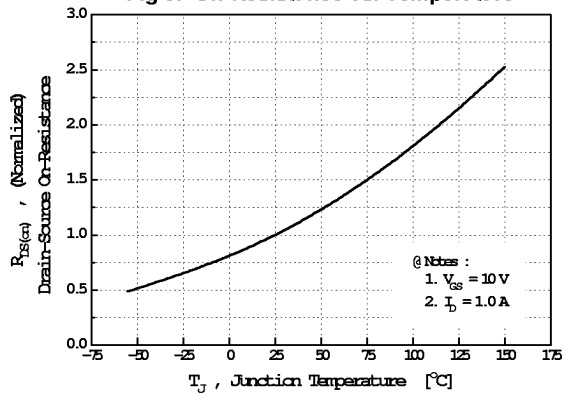


Fig 9. Max. Safe Operating Area

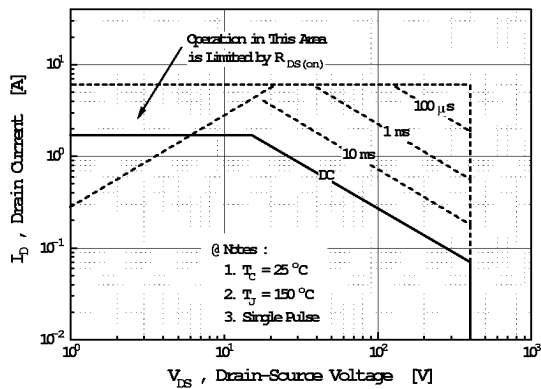


Fig 10. Max. Drain Current vs. Case Temperature

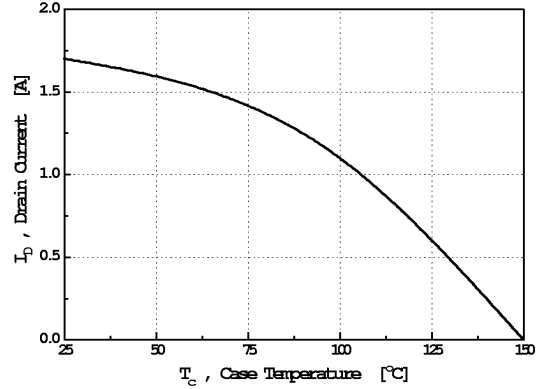


Fig 11. Thermal Response

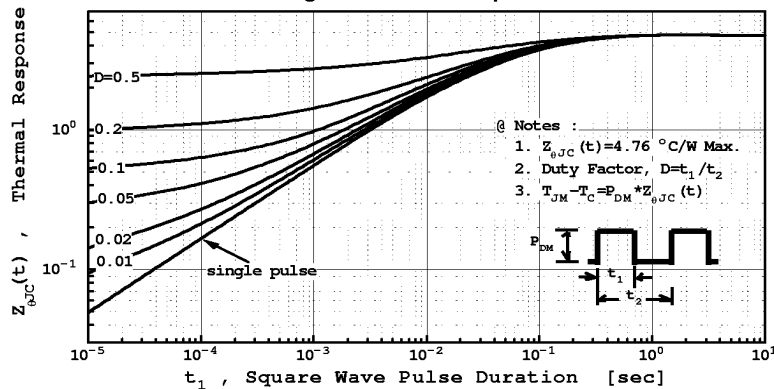


Fig 12. Gate Charge Test Circuit & Waveform

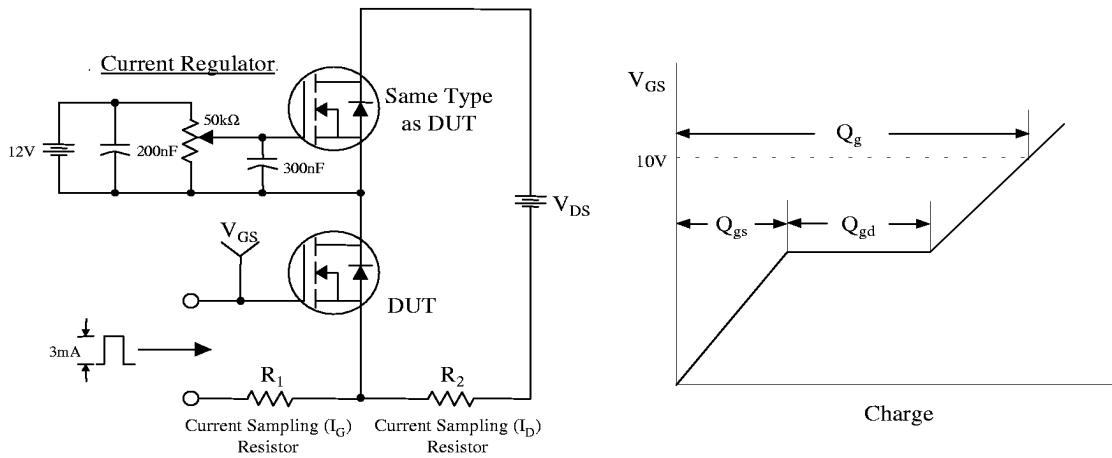


Fig 13. Resistive Switching Test Circuit & Waveforms

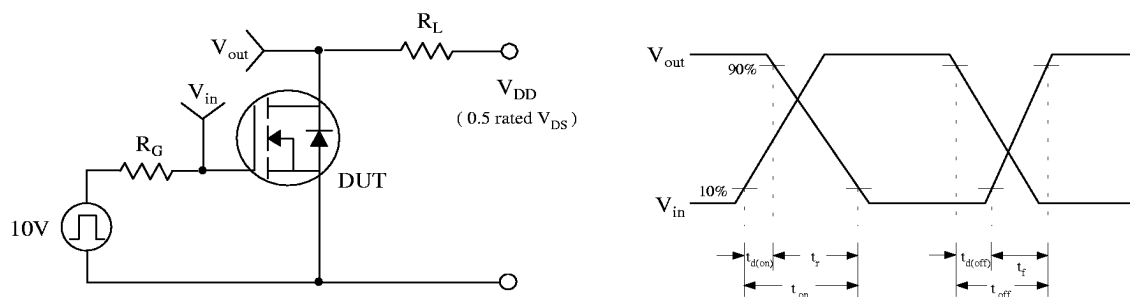


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

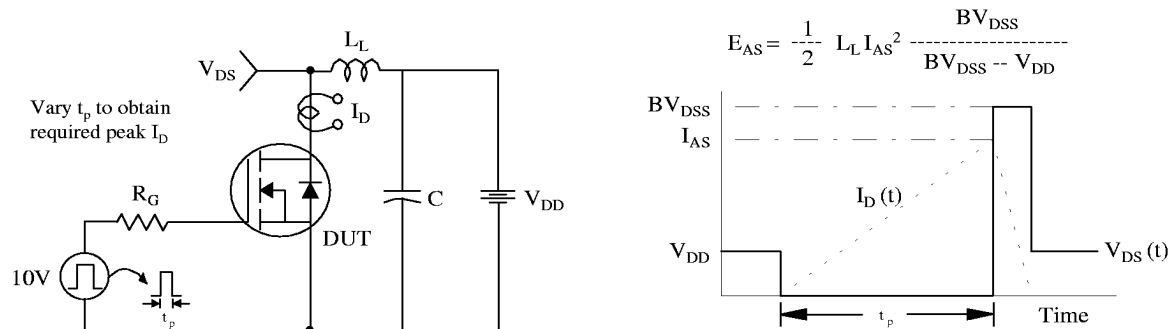


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

