

Vishay Siliconix

Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	40			
$R_{DS(on)}$ (Ω) at $V_{GS} = 10 \text{ V}$	0.020			
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5 \text{ V}$	0.028			
I _D (A) per leg	8			
Configuration	Dual			

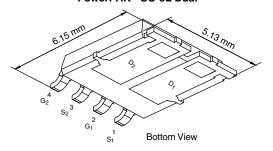
FEATURES

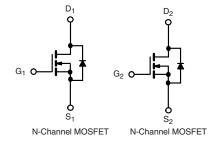
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC











ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ970EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	40	V	
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ^a	T _C = 25 °C	- I _D	8		
	T _C = 125 °C		8		
Continuous Source Current (Diode Conduction) ^a		I _S	8	А	
Pulsed Drain Current ^b		I _{DM}	32		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	28		
Single Pulse Avalanche Energy	L = 0.1 IIIIA	E _{AS}	39	mJ	
Maximum Power Dissipation ^b	T _C = 25 °C	P _D	48	W	
	T _C = 125 °C	T _D	16		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature) ^{e, f}			260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	85	°C/W	
Junction-to-Case (Drain)		R _{thJC}	3.1	C/VV	

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.
- e. See solder profile (www.vishav.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TES	TEST CONDITIONS		TYP.	MAX.	UNIT	
Static							,	
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		40		=.	V	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		2.0	2.5	ľ	
Gate-Source Leakage	I _{GSS}	V _{DS} =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
Zero Gate Voltage Drain Current		$V_{GS} = 0 V$	V _{DS} = 40 V	-	-	1		
	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 40 V, T _J = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	V _{DS} = 40 V, T _J = 175 °C	-	-	150		
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥5 V	30			Α	
Drain-Source On-State Resistance ^a		V _{GS} = 10 V	I _D = 10.2 A	-	0.016	0.020	Ω	
	Б	V _{GS} = 4.5 V	I _D = 8.7 A	=.	0.022	0.028		
	R _{DS(on)}	V _{GS} = 10 V	I _D = 10.2 A, T _J = 125 °C	-	0.025	0.031		
		V _{GS} = 10 V	I _D = 10.2 A, T _J = 175 °C	-	0.029	0.036		
Forward Transconductanceb	9 _{fs}	V _{DS} =	= 15 V, I _D = 10.2 A	-	28	-	S	
Dynamic ^b								
Input Capacitance	C _{iss}		V _{GS} = 0 V V _{DS} = 20 V, f = 1 MHz	=.	1730	2165	pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$		=.	260	325		
Reverse Transfer Capacitance	C _{rss}	1		=.	130	165		
Total Gate Charge ^c	Qg		= 10 V V _{DS} = 20 V, I _D = 10.2 A	-	34	55	nC	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V		-	5.2	-		
Gate-Drain Charge ^c	Q _{gd}	1		-	6.5	-		
Gate Resistance	R _g	f = 1 MHz		0.71	3.92	7.12	Ω	
Turn-On Delay Time ^c	t _{d(on)}			-	10	15		
Rise Time ^c	t _r	V_{DD} = 20 V, R_L = 20 Ω $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω		-	8	12	ns	
Turn-Off Delay Time ^c	t _{d(off)}			-	50	75		
Fall Time ^c	t _f			-	10	15		
Source-Drain Diode Ratings and Chara	icteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	32	Α	
Forward Voltage	V _{SD}	$I_F = 2.9 \text{ A}, V_{GS} = 0$		_	0.8	1.1	V	

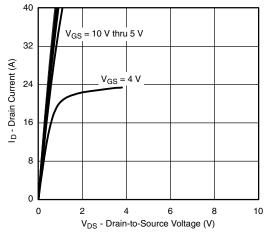
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,\,duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

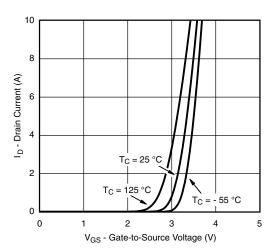
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



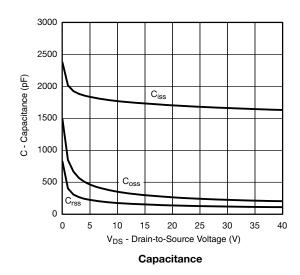
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

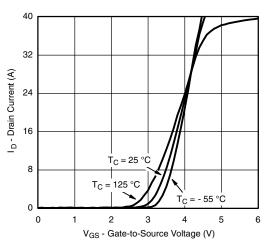


Output Characteristics

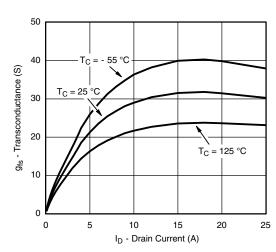


Transfer Characteristics

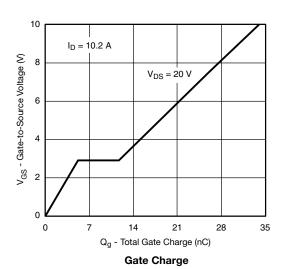




Transfer Characteristics

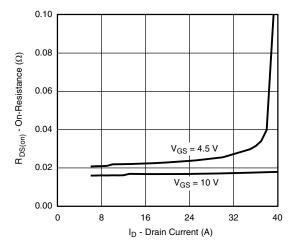


Transconductance

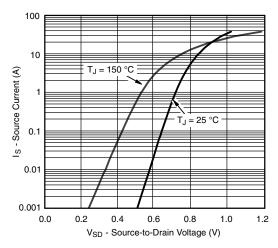




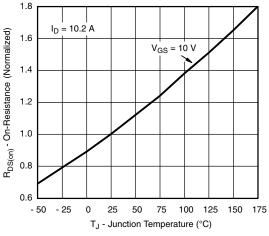
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



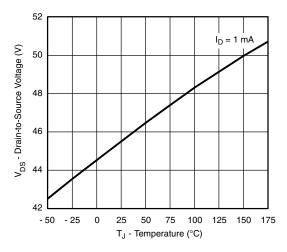
On-Resistance vs. Drain Current



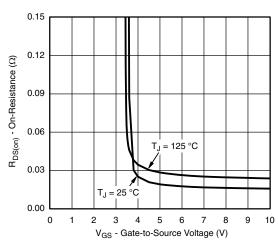
Source Drain Diode Forward Voltage



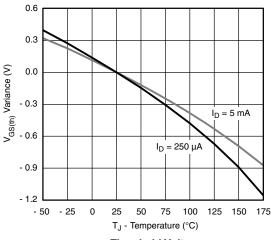
On-Resistance vs. Junction Temperature



Drain-Source Breakdown vs. Junction Temperature



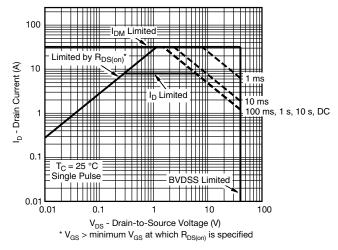
On-Resistance vs. Gate-to-Source Voltage



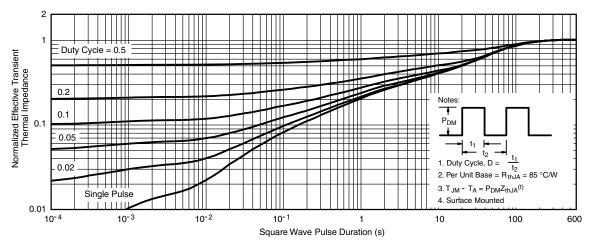
Threshold Voltage



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



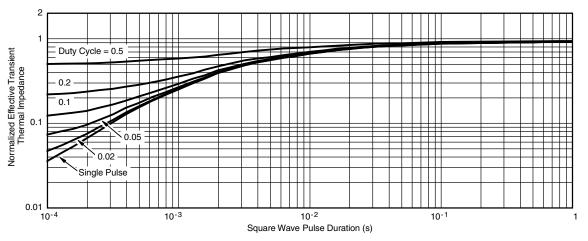
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65282.



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