Infrared remote control transmitter RC-5 PCA8521

FEATURES

- RC5 protocol
- Maximum of:
  - 56 keys (20-pin version)
  - 30 keys (16-pin version)
- Option of multi-system or single system transmitter
  - Multi-system: maximum 8 systems, selection by key
  - Single system: maximum 8 different systems per IC, selection by jumper wire or switch
- Power-down and key wake-up
- High output current (≤ 45 mA)
- Oscillator frequency of 432 kHz or 4 MHz
- Multiple key protection
- Option of 25% or 33% duty factor
- Contained in DIP16, SO16, DIP20 or SO20 packages.

GENERAL DESCRIPTION

The PCA8521 can be used in infrared remote control transmitters. It generates output pulses, in accordance with the RC5 protocol, when a key is pressed. The IC does not contain a software programmable processor. However, it does contain a ROM in which the codes that have to be transmitted are stored. An example of an application diagram using a 20-pin IC is illustrated in Fig.7. The oscillator frequency may be optionally chosen as 432 kHz or 4 MHz. For 432 kHz additional external capacitors must be connected. The capacitors for a 4 MHz oscillator is integrated. When a key in the key-matrix is pressed a drive line will be connected to a sense line. This causes the oscillator to start and a corresponding code will be generated conforming to the RC5 protocol.

Seven drive lines ($\overline{DR0}$ to $\overline{DR6}$) and eight sense lines (SN0 to SN7) may be connected via the key matrix to scan the keys (see Fig.1).

When two or more keys are activated simultaneously no transmission will take place.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8521FP	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-4
PCA8521FT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA8521BP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCA8521BT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

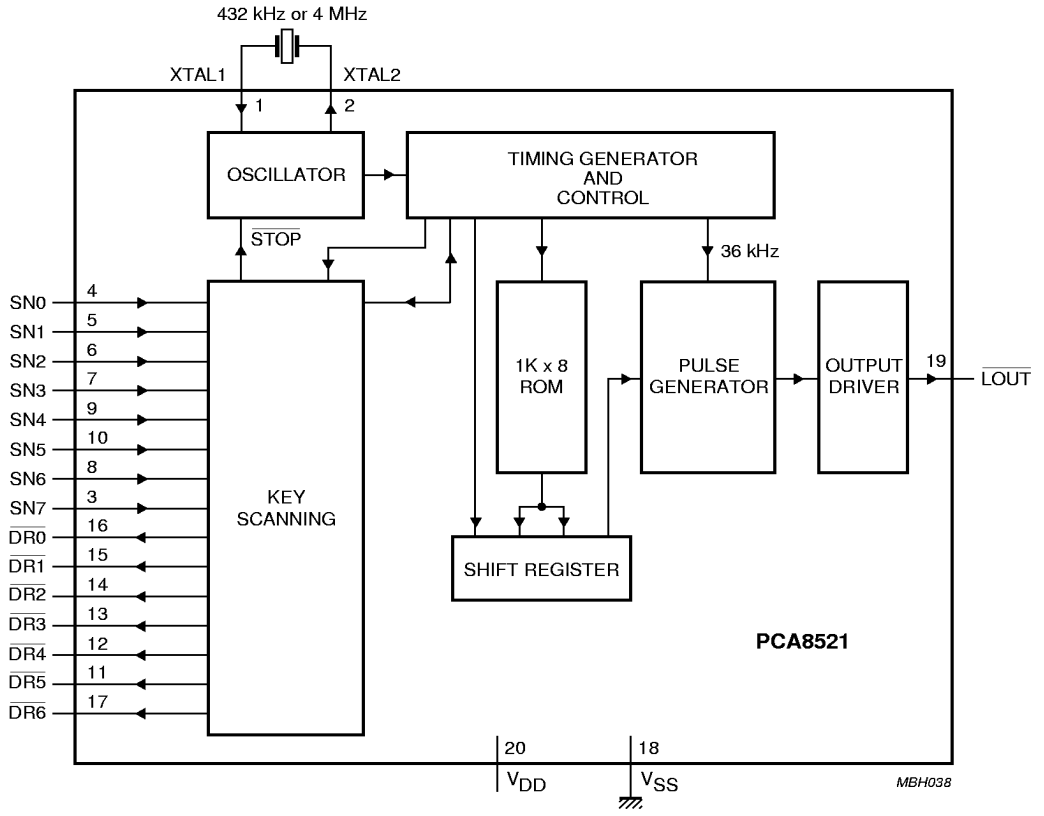


Fig.1 Block diagram (for DIP20 and SO20 packages).

PINNING

16-pin dual in-line and small outline package

SYMBOL	PIN	DESCRIPTION
XTAL1	1	oscillator input
XTAL2	2	oscillator output
SN0	3	sense line 0 for key matrix
SN1	4	sense line 1 for key matrix
SN2	5	sense line 2 for key matrix
SN3	6	sense line 3 for key matrix
SN4	7	sense line 4 for key matrix
SN5	8	sense line 5 for key matrix
$\overline{DR4}$	9	drive line 4 for key matrix (active LOW)
$\overline{DR3}$	10	drive line 3 for key matrix (active LOW)
$\overline{DR2}$	11	drive line 2 for key matrix (active LOW)
$\overline{DR1}$	12	drive line 1 for key matrix (active LOW)
$\overline{DR0}$	13	drive line 0 for key matrix (active LOW)
V_{SS}	14	ground
$\overline{LOUT}$	15	output signal (active LOW)
V_{DD}	16	power supply

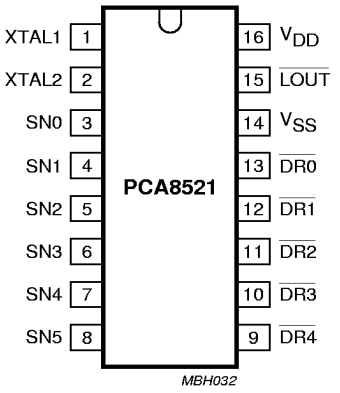


Fig.2 Pin configuration (DIP/SO16).

20-pin dual in-line and small outline package

SYMBOL	PIN	DESCRIPTION
XTAL1	1	oscillator input
XTAL2	2	oscillator output
SN7	3	sense line 7 for key matrix
SN0	4	sense line 0 for key matrix
SN1	5	sense line 1 for key matrix
SN2	6	sense line 2 for key matrix
SN3	7	sense line 3 for key matrix
SN6	8	sense line 6 for key matrix
SN4	9	sense line 4 for key matrix
SN5	10	sense line 5 for key matrix
$\overline{DR5}$	11	drive line 5 for key matrix (active LOW)
$\overline{DR4}$	12	drive line 4 for key matrix (active LOW)
$\overline{DR3}$	13	drive line 3 for key matrix (active LOW)
$\overline{DR2}$	14	drive line 2 for key matrix (active LOW)
$\overline{DR1}$	15	drive line 1 for key matrix (active LOW)
$\overline{DR0}$	16	drive line 0 for key matrix (active LOW)
$\overline{DR6}$	17	drive line 6 for key matrix (active LOW)
V_{SS}	18	ground
$\overline{LOUT}$	19	output signal (active LOW)
V_{DD}	20	power supply

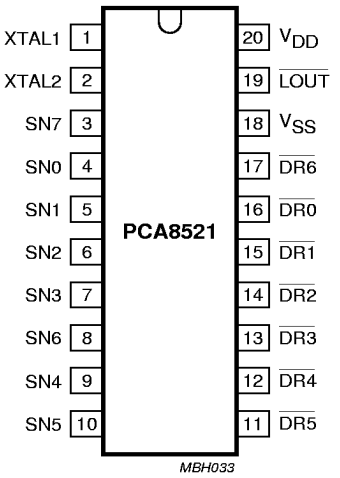


Fig.3 Pin configuration (DIP/SO20).

FUNCTIONAL DESCRIPTION

Key numbering for the matrix is given in Tables 1 and 2.

Table 1 Key numbering for 16-pin package

DRIVER LINES	SENSE LINES					
	SN0	SN1	SN2	SN3	SN4	SN5
$\overline{DR0}$	0	1	2	3	4	5
$\overline{DR1}$	8	9	10	11	12	13
$\overline{DR2}$	16	17	18	19	20	21
$\overline{DR3}$	24	25	26	27	28	29
$\overline{DR4}$	32	33	34	35	36	37

Table 2 Key numbering for 20-pin package

DRIVER LINES	SENSE LINES							
	SN0	SN1	SN2	SN3	SN4	SN5	SN6	SN7
$\overline{DR0}$	0	1	2	3	4	5	6	7
$\overline{DR1}$	8	9	10	11	12	13	14	15
$\overline{DR2}$	16	17	18	19	20	21	22	23
$\overline{DR3}$	24	25	26	27	28	29	30	31
$\overline{DR4}$	32	33	34	35	36	37	38	39
$\overline{DR5}$	40	41	42	43	44	45	46	47
$\overline{DR6}$	48	49	50	51	52	53	54	55

When the keys have been scanned the key-number of the activated key serves as the address of the ROM to obtain the required code-word. When a 16-pin IC is used the following sense lines and driver lines will not be connected; SN6, SN7, $\overline{DR5}$ and $\overline{DR6}$. Consequently, key numbers 6, 7, 14, 15, 22, 23, 30, 31, 38, 39 and 40 to 55 will not be addressed.

The ROM contains 8 banks of 64 code-words. Thus for each key a maximum of 8 different code-words may be generated. With multi-system use, 8 different systems (e.g. TV, VCR, tuner, CD etc.) may be selected. Apart from the system bits the command bits may also be different in different banks (true multi-function keys). Selection can be performed using the keys. For each key three bank select bits are present that determine which bank will be selected for the next key.

For each key an 'inhibit' bit is also present. When this bit is at logic 1 at an address in a given bank, and when the corresponding key is pressed (when this bank has been selected) no transmission will take place.

A single system option is available however, whereby instead of keys a jumper wire and/or a switch may be used for bank selection. Using this option it is possible to program different transmitter models in one IC and select the required bank by means of a jumper wire. Instead of a jumper wire a side-switch may also be used to change the generated code temporarily (select different bank) to obtain multi-function keys. With this option the jumper wires or switch must be connected between sense line SN0 and one of the drive lines $\overline{DR0}$ to $\overline{DR6}$ or ground. This means that SN0 cannot be used to connect keys and the maximum number of keys will be 25 keys for a 16-pin package and 49 keys for a 20-pin package.

It is not possible to use a combination of jumper wires and selection keys for bank selection in one unit.

The output of the ROM is loaded into a shift register that provides the input bits for the pulse generator. This pulse generator drives the output pin.

Timing generator

A schematic diagram of the timing generator is illustrated in Fig.4. The oscillator frequency is 432 kHz or 4 MHz. The timing generator is stopped when no key is activated and started again when a key is pressed.

The output of the oscillator (CLK1) is divided by 111 for 4 MHz or by 12 for 432 kHz. Selection is achieved using a mask option. The output of the divider is CLK2 which is used for clocking of the control timer. The frequency of CLK2 is 36 kHz and the inverse is used to generate the output pulses in the subcarrier frequency. By mask option the duty factor can be chosen to be 25% or 33%.

The control timer has a length of 4096 subcarrier (pulse) periods. This is equal to the transmission repetition time. A bit time is equal to 64 pulses and the repetition time is 64 bit times. The control timer provides the timing of the key scanning, the ROM access and the code transmission. When the control timer has arrived at a certain state, and no key has been pressed for at least 28 ms, a stop signal will be generated which will stop the oscillator. All drive lines will then be set to logic 0. As soon as a key is pressed one of the sense lines will become logic 0. This will generate a start signal which will restart the oscillator.

Key scanning

Six bits of the control timer are used to control the key scanning, subsequently 64 time slots are available. Each time slot corresponds to a key number. The 3 most significant bits (MSBs) control the drive lines and the 3 least significant bits (LSBs) control the sense lines. The scan timing is illustrated in Fig.5. In the first 8 time slots drive line $\overline{DR0}$ is LOW. During this time the 8 sense lines SN0 to SN7 are sequentially tested. The same occurs for the next 8 time slots when $\overline{DR1}$ is at logic 0 and so on until $\overline{DR6}$ is at logic 0. After testing there are 8 time slots when no drive line is at logic 0 (all drive lines HIGH).

When, during time slots 0 to 63, one of the sense lines is at logic 0 the contents of the 6 bits is stored in the key register. This register is used to address the ROM.

No transmission will take place when two or more keys are activated. This situation is considered to be the same as 'no key' and the control bit in the command word for the next transmission will be toggled.

When no key is pressed the oscillator will stop at the end of the control timer (see Section "Timing generator"). In this situation all drive lines will be set to logic 0. When one of the keys is pressed again a wake-up will occur by starting the oscillator.

An option is available to select 'single' or 'multi' system.

Single system

SN0 should be connected to one of the drive lines or ground.

The bank that will be selected is equal to drive line number to which SN0 is connected. When connected to ground the number will be 7. This is achieved by loading the bank select flip-flops BS0 to BS2 with the contents of C5 to C7 of the control timer (see Fig.4) when sense line SN0 is at logic 0. In this way it is possible to use two different systems in one transmitter by using a side switch. With this option SN0 cannot be used to connect keys, so the maximum number of keys will be lower. (49 keys with 20-pin IC and 25 keys with 16-pin IC).

Multi system

The bank is selected by key for maximum 8 different systems (e.g. TV, VCR, CD, etc.), any key is flexible for bank selection. When a user inserts a new battery, the default bank is always in bank 7. If only bank 7 is used, then maximum number of keys can be:

- 56 keys for a 20-pin IC
- 30 keys for 16-pin IC.

ROM

A schematic diagram of the ROM is illustrated in Fig.6. The ROM is divided into 8 banks of 2×64 bytes. Bank selection is performed using flip-flops BS0 to BS2 that are the 3 highest bits of the address. With the 'single system' these bits are loaded from the 3 MSBs of the scan control when SN0 = 0. At power-on the bank select flip-flops will be in an arbitrary state.

When a key was activated, the key number is stored in the 6-bit key register. This register forms the lower bits of the ROM address. For each command the ROM will be accessed twice. This gives 16 bits in total (M0L to M7L and M0H to M7H). The bits are described in Table 3.

Table 3 ROM bit description

BITS	FUNCTION
M0L to M5L	Command bits 0 to 5.
M6L	Field bit. This bit indicates whether command codes 0 to 63 are used (field bit is at logic 1) or command codes 64 to 127 are used (field bit is at logic 0).
M7L	Inhibit bit. When this bit is at logic 1 no transmission will take place. When this bit is at logic 0 the appropriate code-word will be transmitted.
M0H to M4H	System bits 0 to 4.
M5H to M7H	Bank select. Will be stored in BS0 to BS2 when the 'multi-system' option is selected. With single system bits M5H to M7H are don't care.

Pulse output

The bits of the remote control word, as indicated by the addressed ROM locations, are loaded into a shift register every bit-time this register is shifted. The output is used to generate a logic 0 or a logic 1 in the biphase (Manchester) coding, modulated with a frequency of 36 kHz. The duty factor of the modulation pulses may be selected (optionally) to be 25% or 33.3%. The output of the pulse generator controls the output driver that can provide a maximum current of 45 mA.

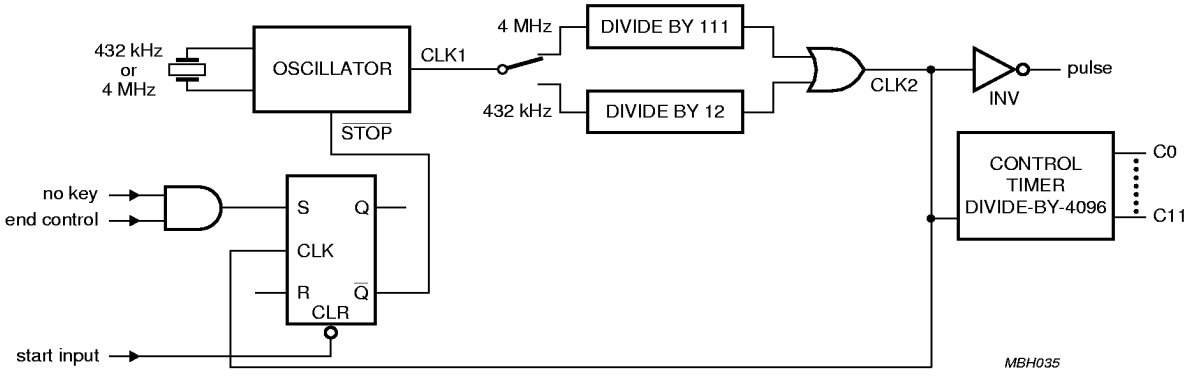


Fig.4 Timer schematic diagram.

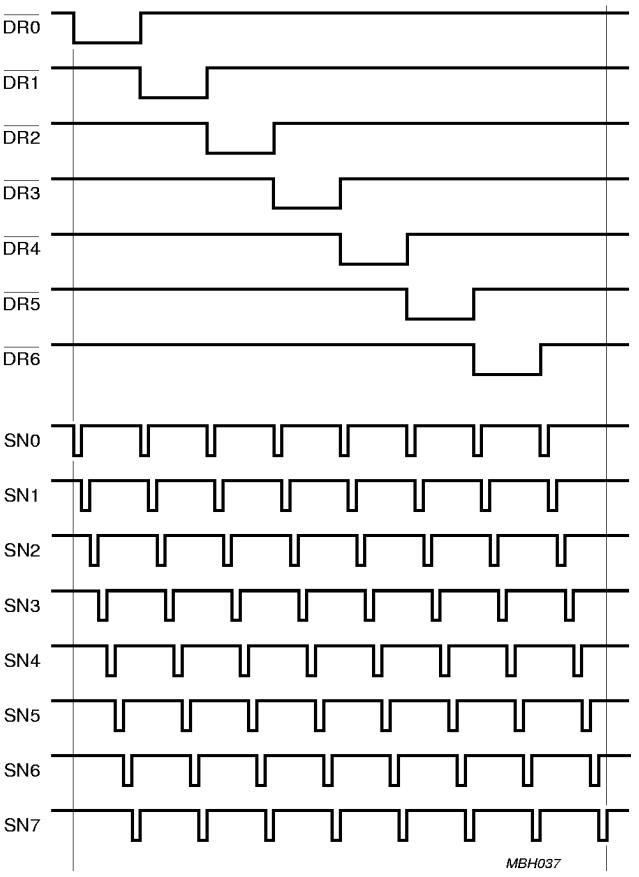


Fig.5 Scan timing.

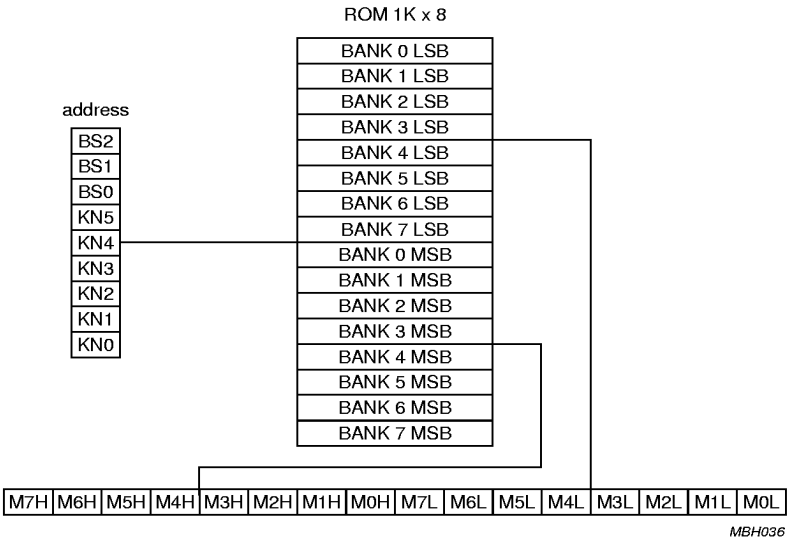


Fig.6 ROM schematic diagram.

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		2.0	–	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; T_{amb} = 25 °C	–	–	2	mA
$I_{DD(q)}$	quiescent current	V_{DD} = 3 V; T_{amb} = 25 °C	–	–	1	µA
T_{amb}	operating ambient temperature		0	–	50	°C
Sense lines (input only and will have a weak internal pull-up resistance)						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
R_{pu}	pull-up resistance	V_{DD} = 2 V	50	–	100	kΩ
Driver lines (output only; open drain; maximum on-resistance when LOW)						
R_{on}	maximum on-resistance	V_{DD} = 2 V	–	–	2	kΩ
Output driver (has a weak pull-up resistance)						
I_{sink}	sink current	V_{DD} = 2 V; V_o = 1 V	–	–	45	mA
R_{pu}	pull-up resistance	V_{DD} = 2 V	–	–	5	kΩ

SYSTEM DEVELOPMENT

Software (RC8521)

A PC program is provided that enables the user to fill in system and command codes for each key number in each bank. This program converts the input data into a ROM code-file needed to produce the metal mask and to program an EPROM to be used in the hardware emulator.

Hardware (OM4839)

An emulator is available that functionally emulates the IC. An EPROM with the ROM code information is inserted into the emulator to produce the required remote control codes corresponding to the keys in the prototype device.

APPLICATION INFORMATION

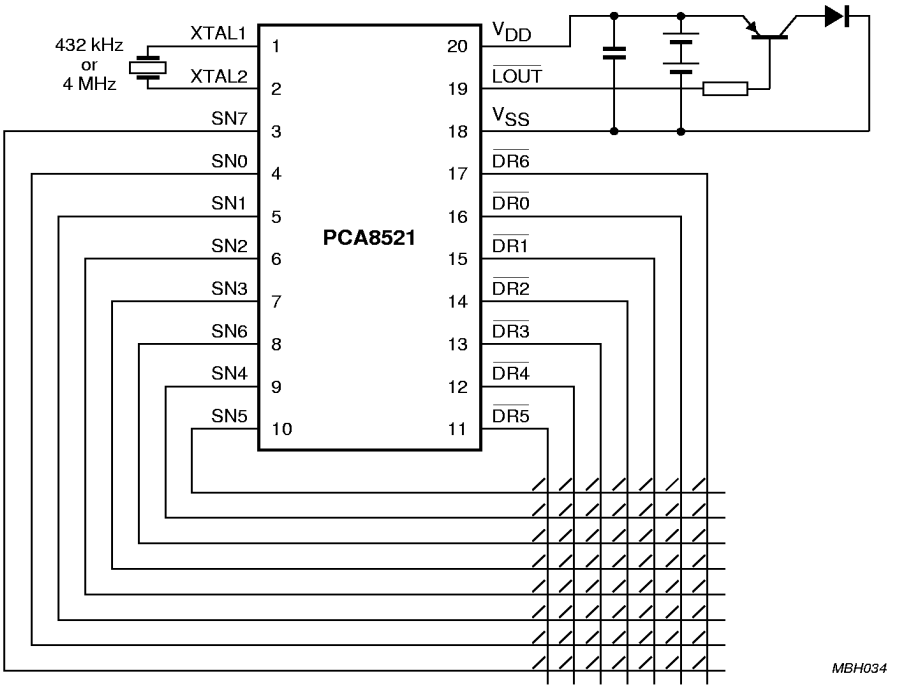


Fig.7 Application diagram (for DIP20 and SO20 packages).

INTERNAL PIN CONFIGURATION

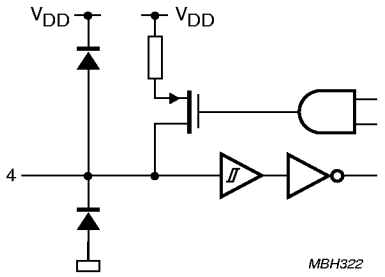


Fig.8 Pin configuration for pin SN0.

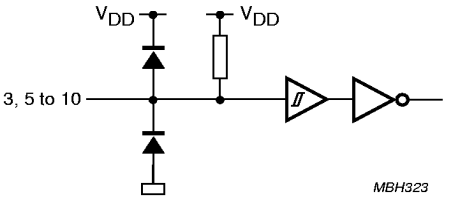


Fig.9 Pin configuration for pins SN1 to SN7.

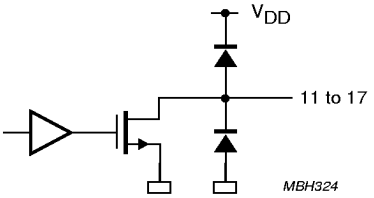


Fig.10 Pin configuration for pins $\overline{DR0}$ to $\overline{DR6}$.

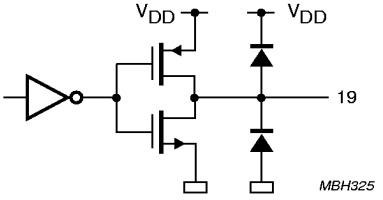
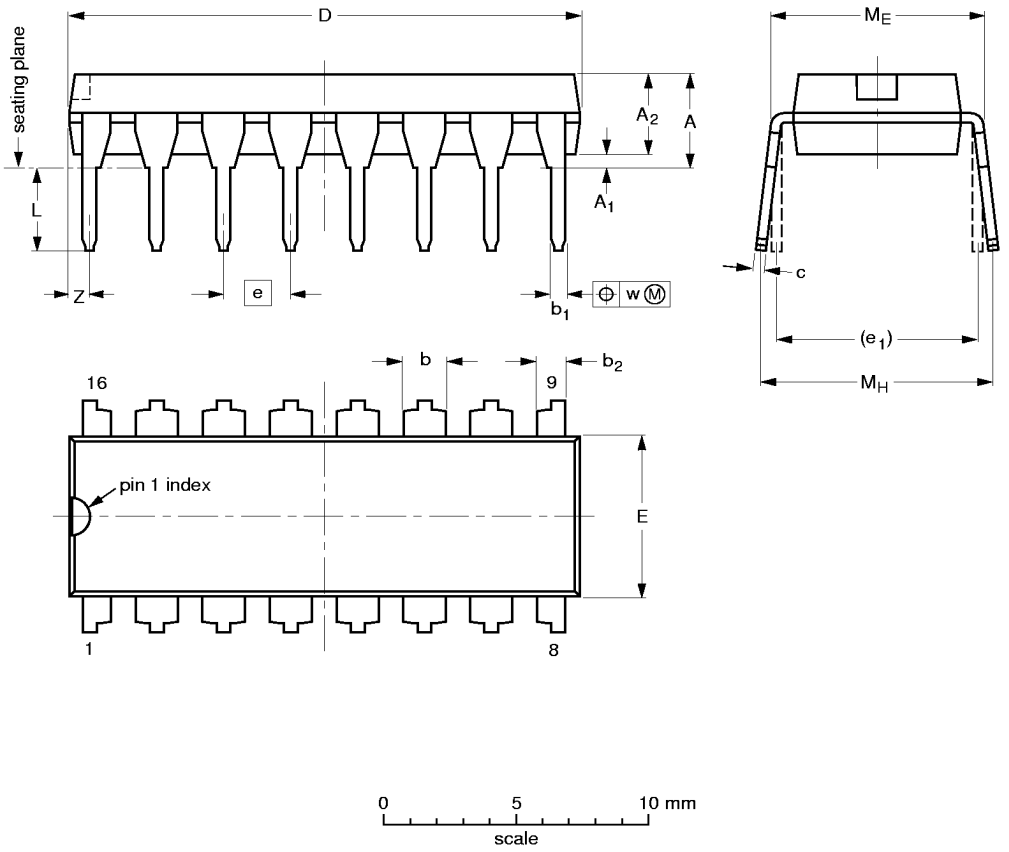


Fig.11 Pin configuration for pin $\overline{LOUT}$.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

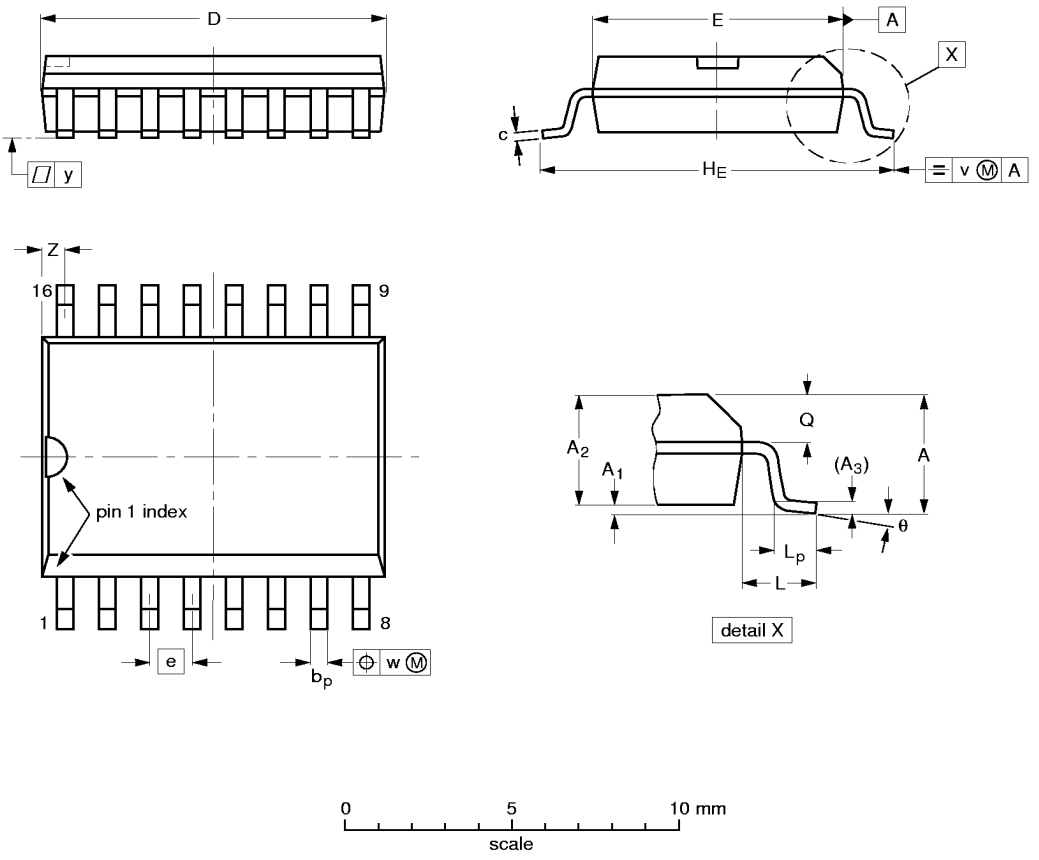
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

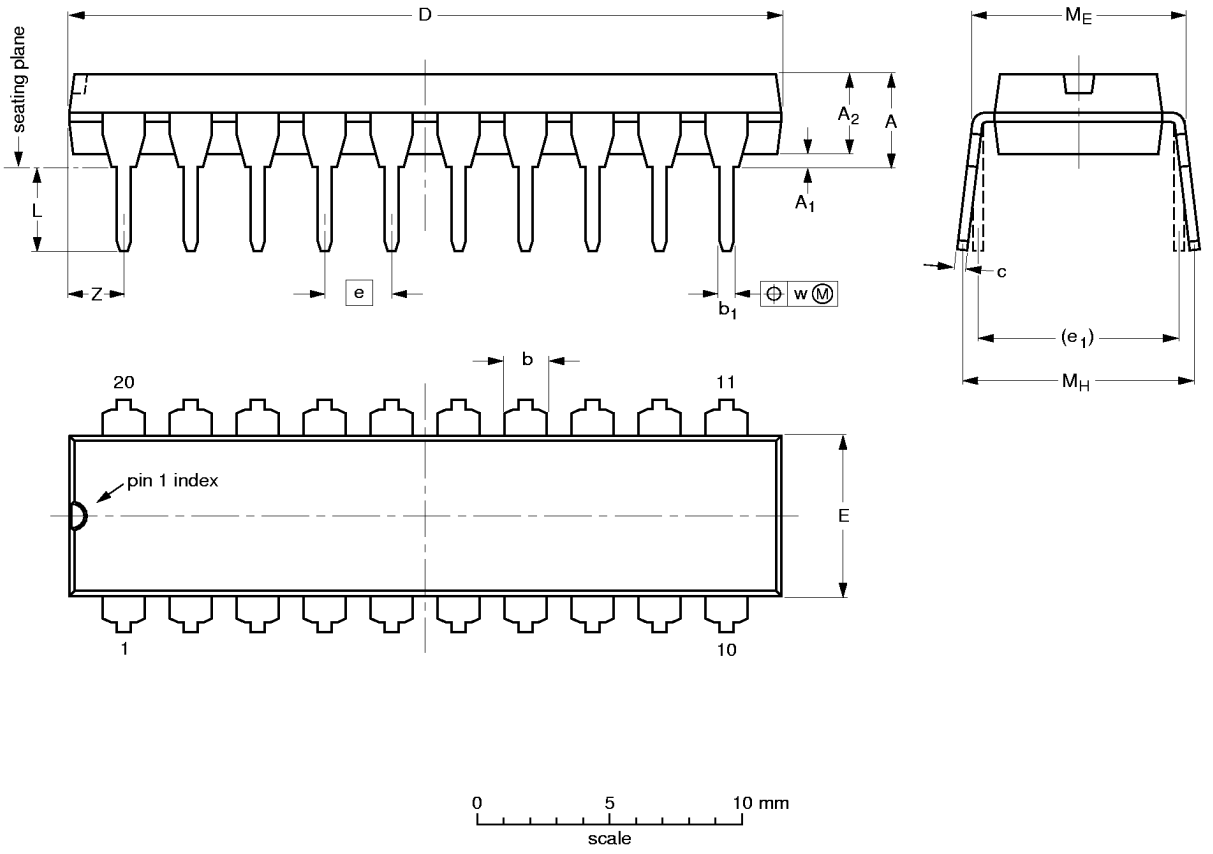
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

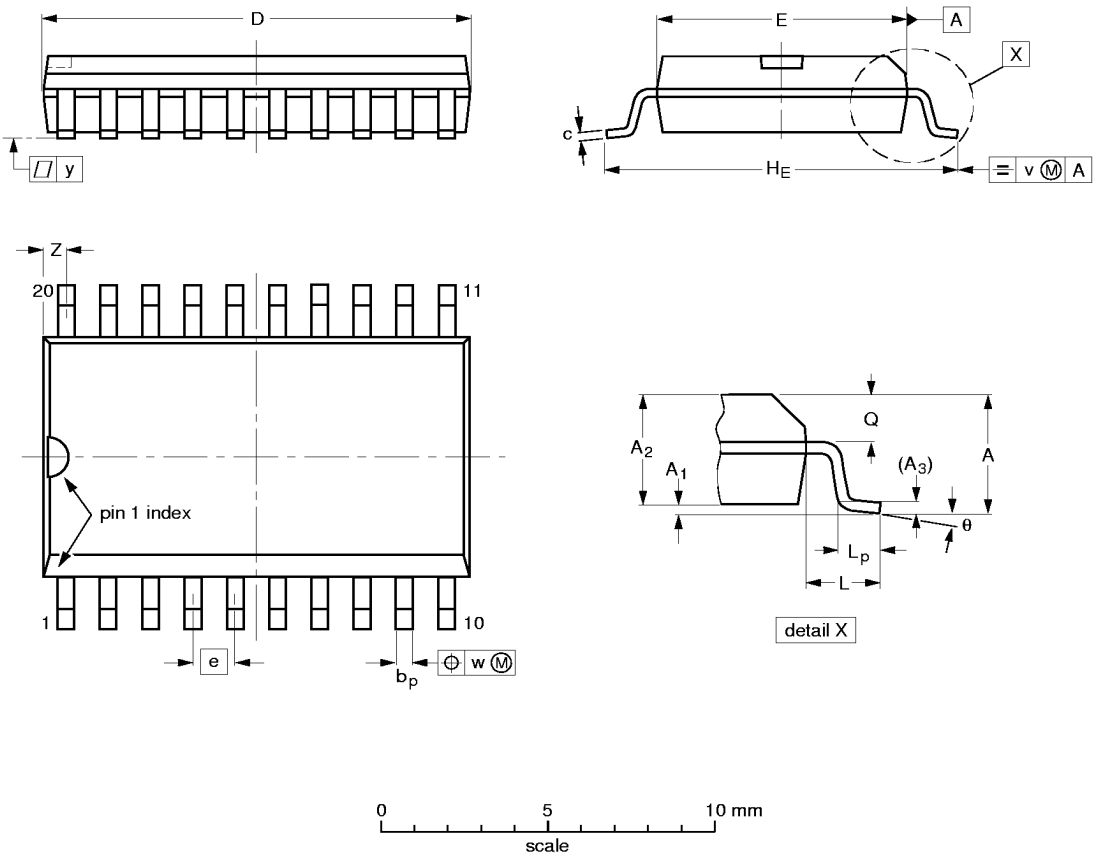
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.