

Document Title

512K x 16 bit 1.8V and Ultra Low Power CMOS Static RAM

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	November 2,2001	Preliminary
0B	1.Remove the 55ns products 2.Change for I _{CC} 1: 15mA to 20mA for 70ns Industrial product 10mA to 12mA for 100ns commercial product 10mA to 15mA for 100ns Industrial product 3.Change for I _{CC} 2: 2mA to 2.5mA 4.Change for I _{SB} 2: 20μA to 25μA for Industrial product 5.Change for V _{DR} Min:1.0V to 1.2V 6.Cgange for I _{DR} : 10μA to 20μA for commerical /L product 6μA to 13μA for commerical/LL product 15μA to 30μA for industrial/L product 8μA to 23μA for Industrial/LL product	September 2,2002	

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512K x 16 1.8V ULTRA LOW POWER CMOS STATIC RAM

FEATURES

- High-speed access times: 70, 100 ns
- CMOS low power operation
 - 20 mW (typical) operating
 - 5 μ W (typical) CMOS standby
- TTL compatible interface levels
- Single 1.65V-2.2V Vcc power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Available in the know good die form 44-pin TSOP-2 and 48-pin 8*10mm TF-BGA

DESCRIPTION

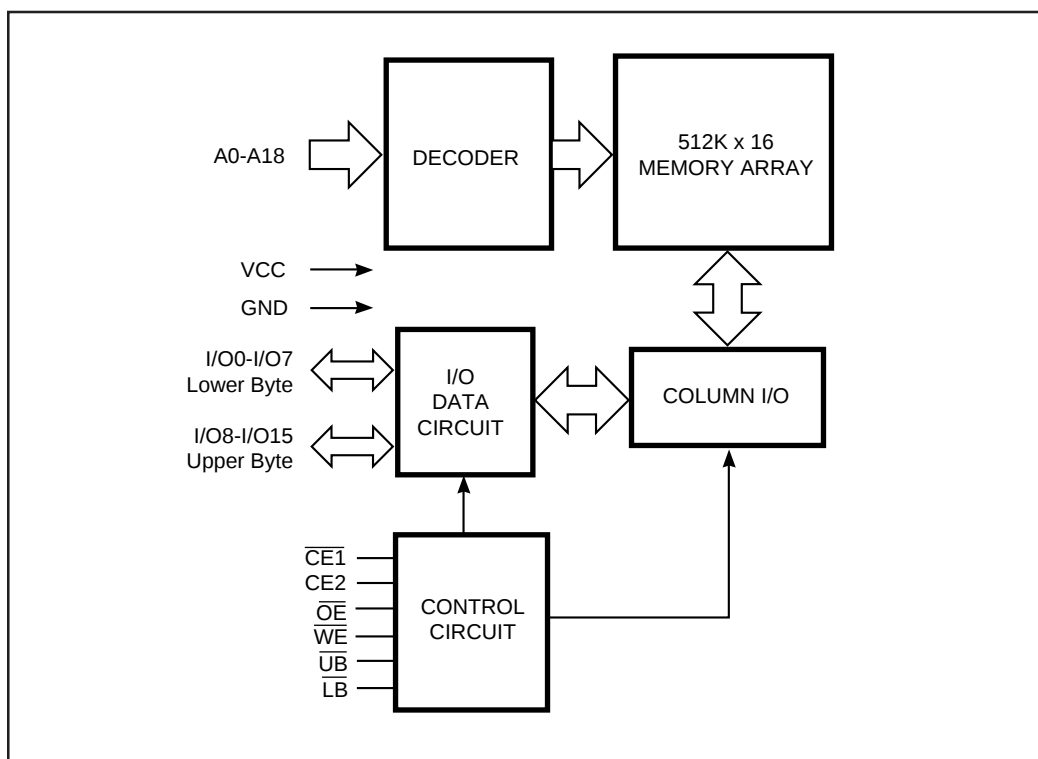
The *ICSI* IC62VV51216L and IC62VV51216LL are low-power, 8,388,608 bit static RAMs organized as 524,288 words by 16 bits. They are fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or CE2 is Low (deselected) or both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using Chip Enable Output and Enable inputs, $\overline{CE1}$, CE2 and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IC62VV51216L and IC62VV51216LL are packaged in the JEDEC standard 44-pin TSOP-2 and 48-pin 8*10mm TF-BGA.

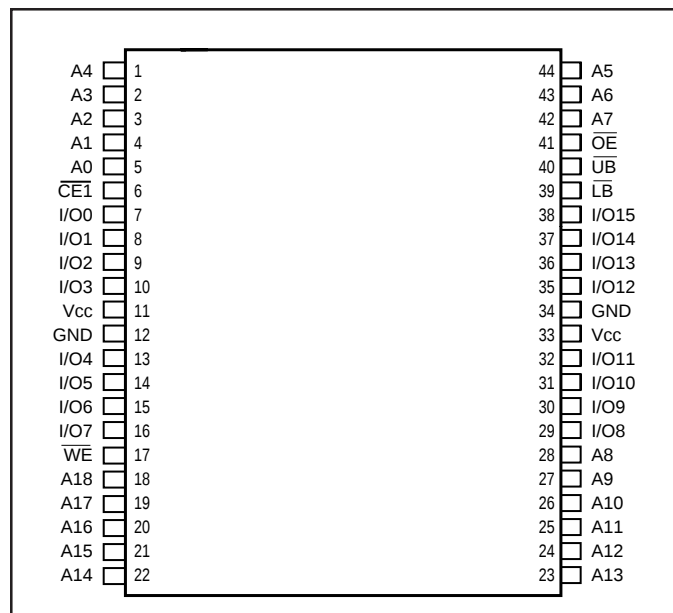
FUNCTIONAL BLOCK DIAGRAM



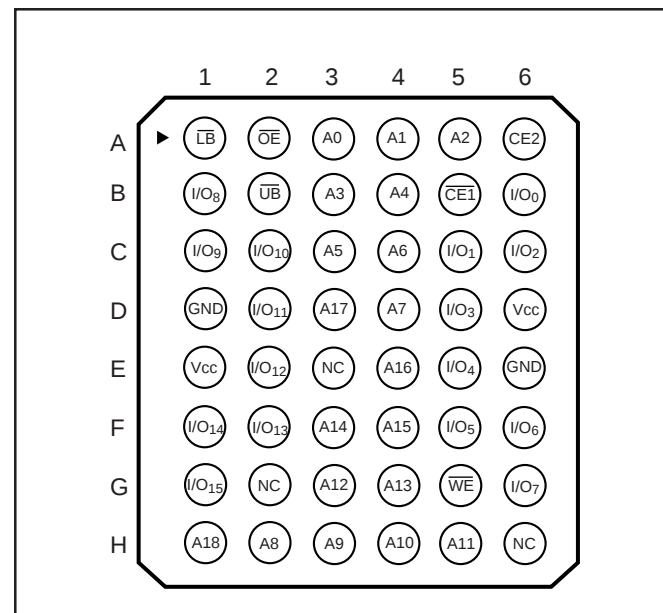
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PIN CONFIGURATIONS

44-Pin TSOP-2



48-Pin TF-BGA (TOP View)



PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O15	Data Input/Output
CE1	Chip Enable1 Input
CE2	Chip Enable2 Input, BGA only
OE	Output Enable Input
WE	Write Enable Input

LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

Mode							I/O PIN		Power
	WE	CE1	CE2	OE	LB	UB	I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	X	High-Z	High-Z	Standby
	X	X	L	X	X	X	High-Z	High-Z	Standby
	X	X	X	X	H	H	High-Z	High-Z	Standby
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	Active
	H	L	H	H	X	L	High-Z	High-Z	Active
Read	H	L	H	L	L	H	DOUT	High-Z	Active
	H	L	H	L	H	L	High-Z	DOUT	Active
	H	L	H	L	L	L	DOUT	DOUT	Active
Write	L	L	H	X	L	H	DIN	High-Z	Active
	L	L	H	X	H	L	High-Z	DIN	Active
	L	L	H	X	L	L	DIN	DIN	Active

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	1.65V- 2.2V
Industrial	−40°C to +85°C	1.65V - 2.2V

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to V _{CC} + 0.4	V
T _{BIAS}	Temperature Under Bias	−40 to +85	°C
V _{CC}	V _{CC} related to GND	−0.3 to +2.4	V
T _{STG}	Storage Temperature	−65 to +150	°C
P _T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = −0.1 mA	1.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	—	0.2	V
V _{IH} ⁽¹⁾	Input HIGH Voltage		1.4	V _{CC} + 0.2	V
V _{IL} ⁽²⁾	Input LOW Voltage ⁽¹⁾		−0.2	0.4	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	−1	1	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC} , OUTPUTS DISABLED	−1	1	μA

Notes:

1. V_{IH}(max.) = V_{CC} + 0.2V for pulse width less than 10ns.
2. V_{IL}(min.) = −2.0V for pulse width less than 10 ns.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 1.4V
Input Rise and Fall Times	5 ns
Input Reference Level	0.9V
Output Reference Level	0.9V
Output Load	See Figures 1 and 2

AC TEST LOADS

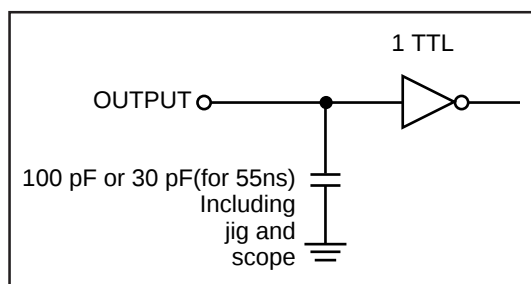


Figure 1

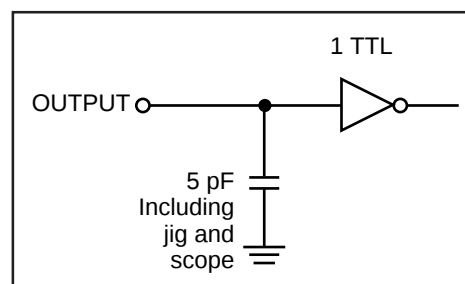


Figure 2

IC62VV51216L POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-70		-100		Unit
				Min.	Max.	Min.	Max.	
I _{CC1}	V _{CC} Dynamic Operating Supply Current	V _{CC} = 1.8V I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	15	—	12	mA
			Ind.	—	20	—	15	
I _{CC2}	V _{CC} Dynamic Operating Supply Current	V _{CC} = 1.8V I _{OUT} = 0 mA, f = 1 MHz	Com.	—	2.5	—	2.5	mA
			Ind.	—	2.5	—	2.5	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., other input=0-V _{CC} 1) $\overline{CE1} \geq V_{CC} - 0.2V$, (CE1 controlled) or 2) $0V \leq CE2 \leq 0.2V$ (CE2 controlled) or 3) $\overline{LB} / \overline{UB} \geq V_{CC} - 0.2$ ($\overline{LB} / \overline{UB}$ controlled)	Com.	—	35	—	35	μA
			Ind.	—	50	—	50	

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

IC62VV51216LL POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-70		-100		Unit
				Min.	Max.	Min.	Max.	
I _{CC1}	V _{CC} Dynamic Operating Supply Current	V _{CC} = 1.8V, I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	15	—	12	mA
			Ind.	—	20	—	15	
I _{CC2}	V _{CC} Dynamic Operating Supply Current	V _{CC} = 1.8V I _{OUT} = 0 mA, f = 1 MHz	Com.	—	2.5	—	2.5	mA
			Ind.	—	2.5	—	2.5	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., other input=0-V _{CC} 1) $\overline{CE1} \geq V_{CC} - 0.2V$, ($\overline{CE1}$ controlled) or 2) $0V \leq CE2 \leq 0.2V$ (CE2 controlled) or 3) $\overline{LB} / \overline{UB} \geq V_{CC} - 0.2$ ($\overline{LB} / \overline{UB}$ controlled)	Com.	—	15	—	15	μA
			Ind.	—	25	—	25	

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

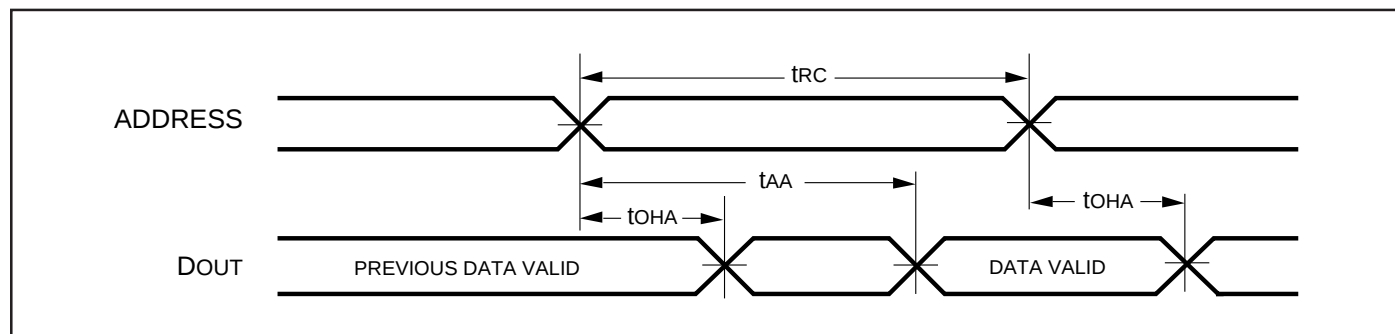
Symbol	Parameter	-70		-100		Unit
		Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	70	—	100	—	ns
t _{AA}	Address Access Time	—	70	—	100	ns
t _{OH}	Output Hold Time	10	—	15	—	ns
t _{ACE}	$\overline{CE1}$ Low and CE2 HIGH Access Time	—	70	—	100	ns
t _{DOE}	$\overline{OE}$ Access Time	—	35	—	50	ns
t _{HZOE} ⁽²⁾	$\overline{OE}$ to High-Z Output	—	25	—	30	ns
t _{LZOE} ⁽²⁾	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t _{HZCE} ⁽²⁾	$\overline{CE1}$ HIGH or CE2 LOW to High-Z Output	0	25	0	30	ns
t _{LZCE} ⁽²⁾	$\overline{CE1}$ Low and CE2 HIGH to Low-Z Output	10	—	10	—	ns
t _{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	70	—	100	ns
t _{HZB}	$\overline{LB}$, $\overline{UB}$ o High-Z Output	0	25	0	30	ns
t _{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
- Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

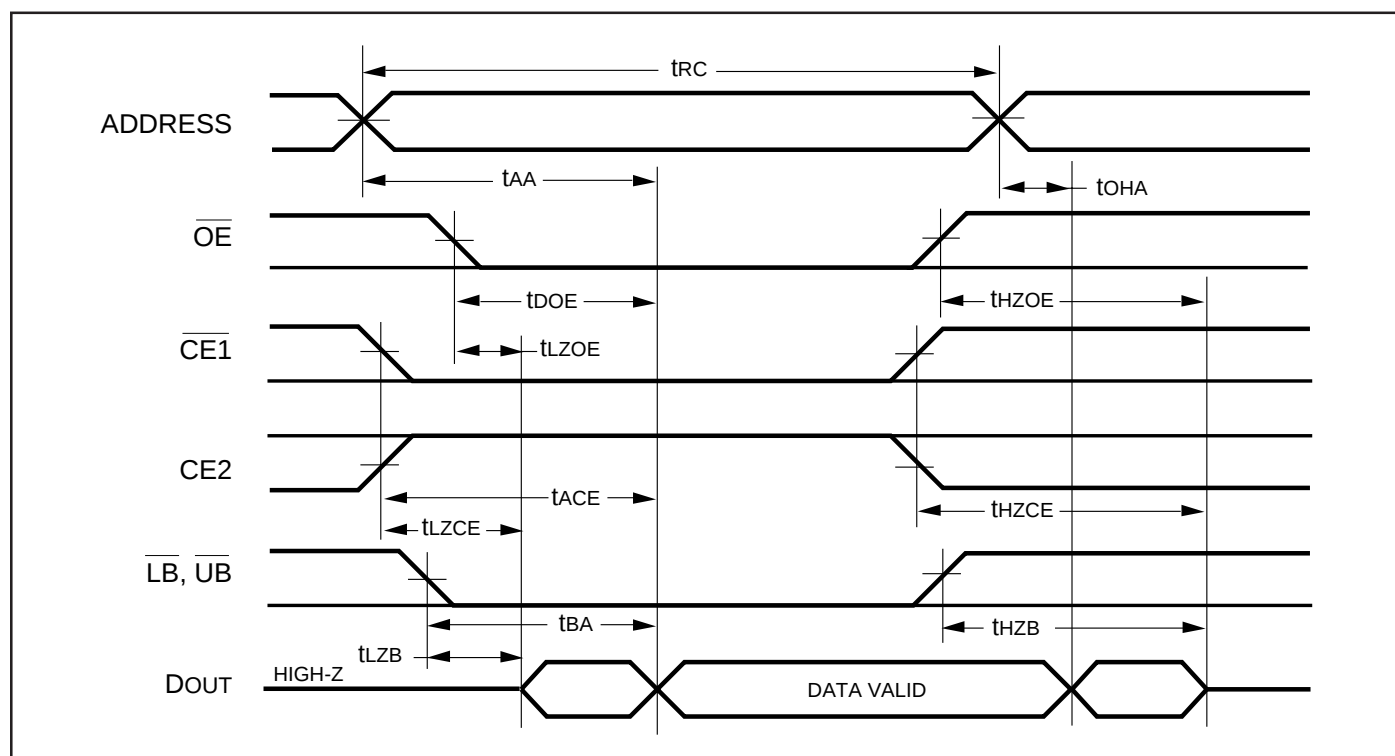
AC TEST LOADS

READ CYCLE NO.1^(1,2) (Address Controlled) ($\overline{CE1} = \overline{OE} = V_{IL}$, $\overline{CE2} = V_{IH}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$)



AC WAVEFORMS

READ CYCLE NO. 2^(1,3) ($\overline{OE}$, Controlled)



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$, $\overline{UB}$, or $\overline{LB} = V_{IL}$, $\overline{CE2} = V_{IH}$
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and $\overline{CE2}$ HIGH transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

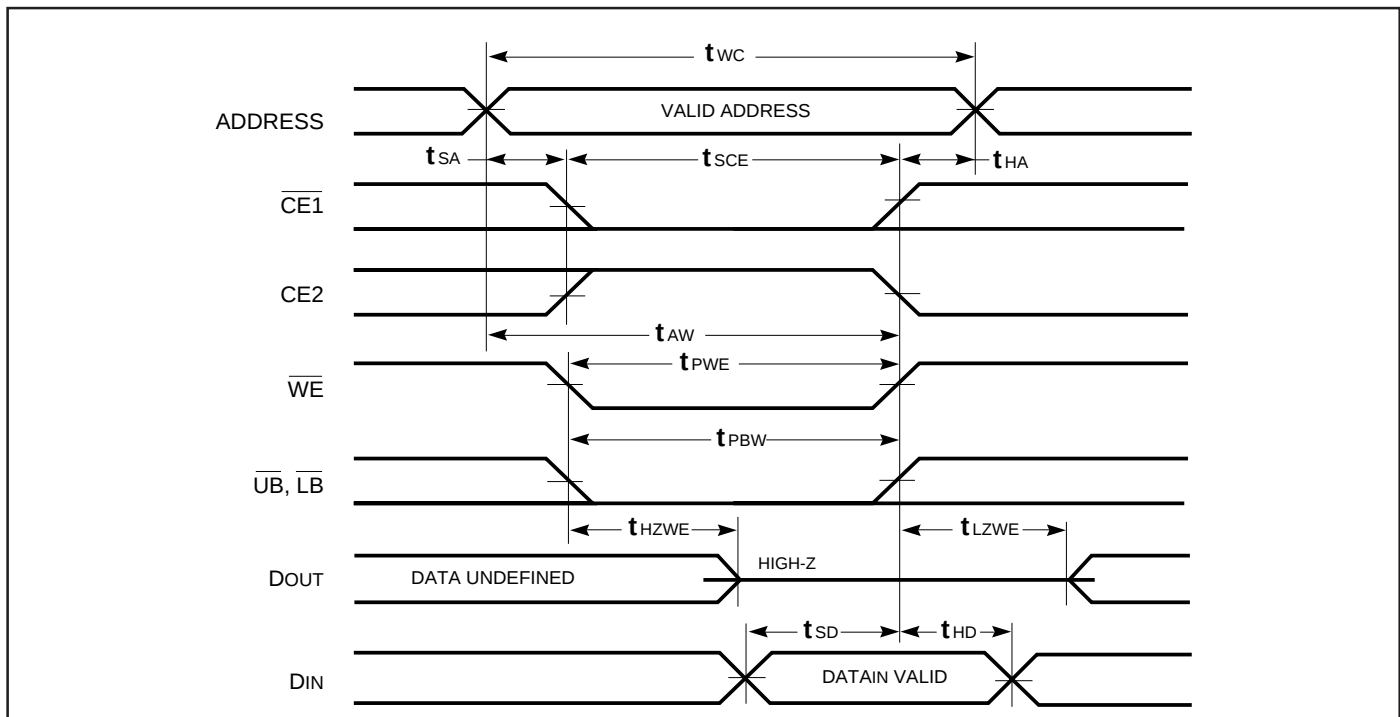
Symbol	Parameter	-70		-100		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	70	—	100	—	ns
t_{SCE}	$\overline{CE1}$ Low and CE2 HIGH to Write End	65	—	80	—	ns
t_{AW}	Address Setup Time to Write End	65	—	80	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	60	—	80	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	55	—	80	—	ns
t_{SD}	Data Setup to Write End	30	—	40	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
$t_{HZWE}^{(3)}$	$\overline{WE}$ LOW to High-Z Output	—	30	—	40	ns
$t_{LZWE}^{(3)}$	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
- The internal write time is defined by the overlap of $\overline{CE1}$ LOW, and $\overline{UB}$ or $\overline{LB}$, $\overline{WE}$ LOW, and CE2 HIGH. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
- Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

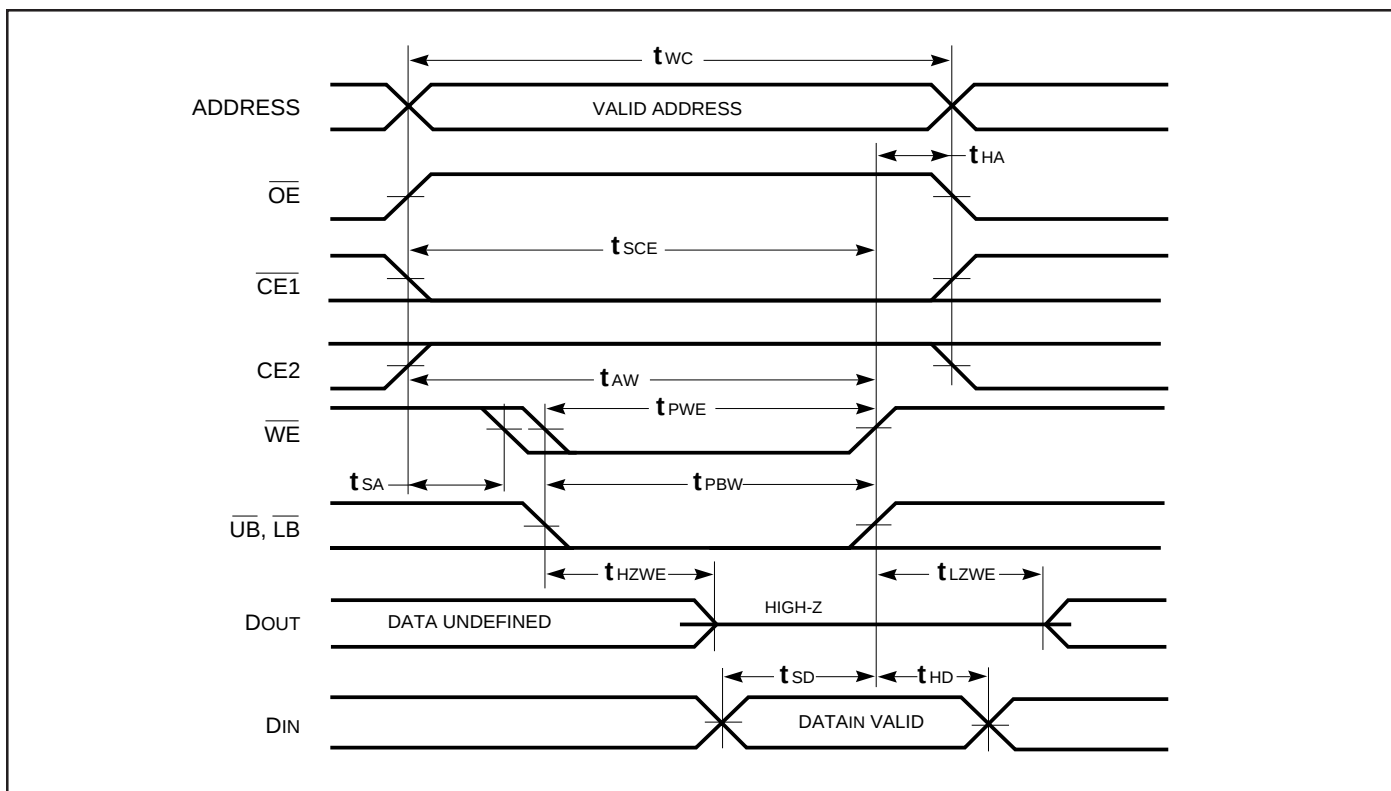
WRITE CYCLE NO. 1^(1,2) ($\overline{CE1}$ or CE2, Controlled, $\overline{OE}$ = HIGH or LOW)



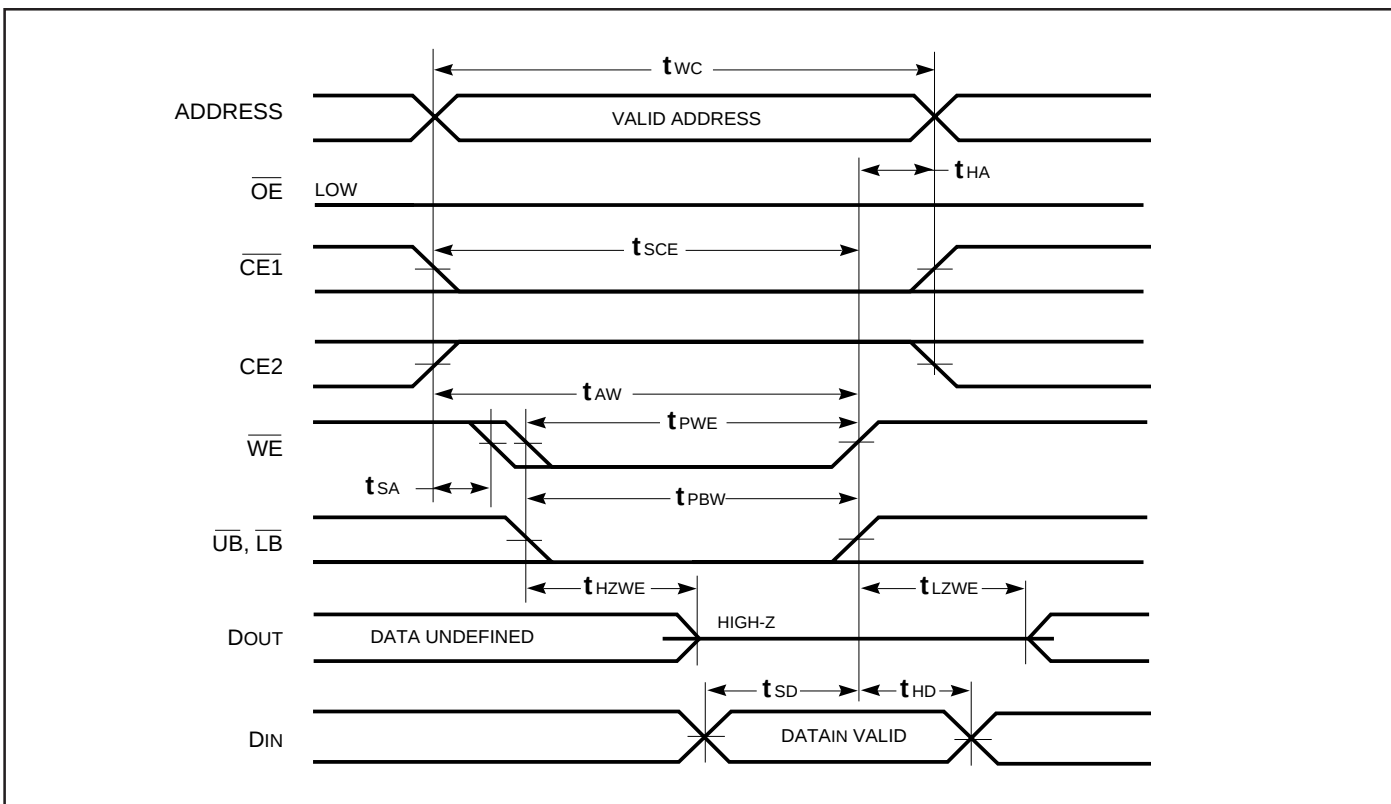
Notes:

- WRITE is an internally generated signal asserted during an overlap of the $\overline{WE}$, $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$ and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.

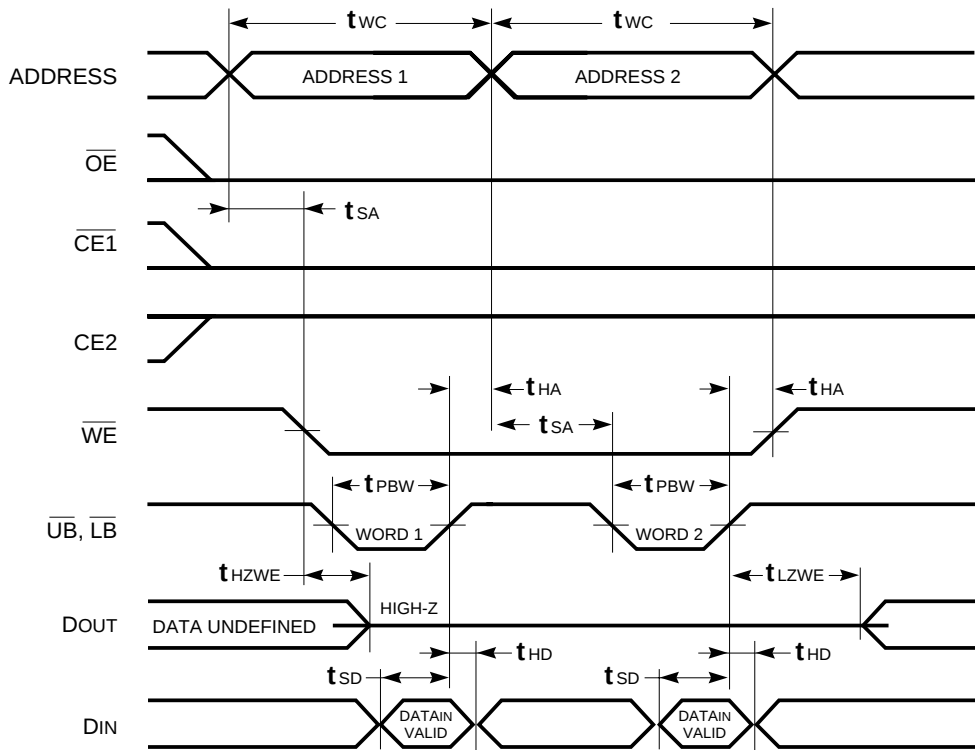
WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled; $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled; $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4 ($\overline{UB}$ / $\overline{LB}$ Controlled)



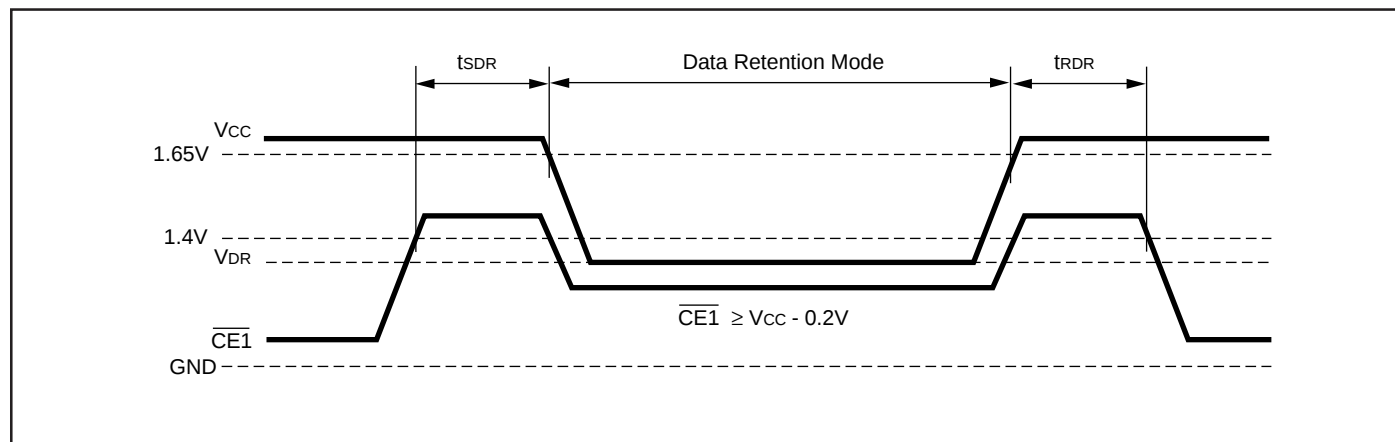
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	See Data Retention Waveform	1.2	2.2	V
I_{DR}	Data Retention Current	$V_{CC} = 1.2V$, $\overline{CE1} \geq V_{CC} - 0.2V^{(1)}$			μA
		Com. (-L)	—	20	
		Com. (-LL)	—	13	
		Ind. (-L)	—	30	
		Ind. (-LL)	—	23	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	10	—	ns

Notes:

- 1) $\overline{CE1} \geq V_{CC} - 0.2V$, ($\overline{CE1}$ controlled) or
- 2) $0V \leq \overline{CE2} \leq 0.2V$ ($\overline{CE2}$ controlled) or
- 3) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2V$, $\overline{CE2} \geq V_{CC} - 0.2V$ ($\overline{LB}/\overline{UB}$ controlled)

DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IC62VV51216L-70T	TSOP-2
	IC62VV51216L-70B	8*10mm TF-BGA
100	IC62VV51216L-100T	TSOP-2
	IC62VV51216L-100B	8*10mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IC62VV51216L-70TI	TSOP-2
	IC62VV51216L-70BI	8*10mm TF-BGA
100	IC62VV51216L-100TI	TSOP-2
	IC62VV51216L-100BI	8*10mm TF-BGA

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IC62VV51216LL-70T	TSOP-2
	IC62VV51216LL-70B	8*10mm TF-BGA
100	IC62VV51216LL-100T	TSOP-2
	IC62VV51216LL-100B	8*10mm TF-BGA

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IC62VV51216LL-70TI	TSOP-2
	IC62VV51216LL-70BI	8*10mm TF-BGA
100	IC62VV51216LL-100TI	TSOP-2
	IC62VV51216LL-100BI	8*10mm TF-BGA



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