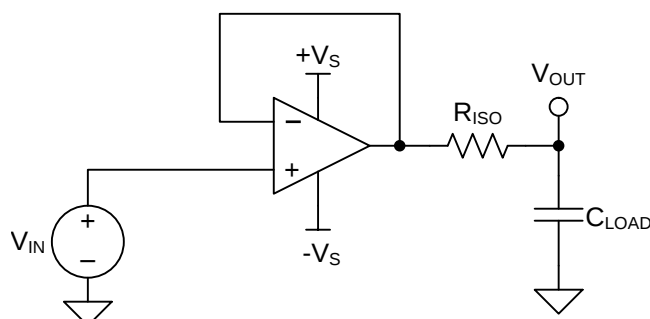


OPA2171-EP 36-V, Single-Supply, SOT553, General-Purpose Operational Amplifiers

1 Features

- Supply Range: 2.7 to 36 V, ± 1.35 V to ± 18 V
- Low Noise: $14 \text{ nV}/\sqrt{\text{Hz}}$
- Low Offset Drift: $\pm 0.3 \text{ } \mu\text{V}/^\circ\text{C}$ (Typ)
- RFI Filtered Inputs
- Input Range Includes the Negative Supply
- Input Range Operates to Positive Supply
- Rail-to-Rail Output
- Gain Bandwidth: 3 MHz
- Low Quiescent Current: 475 μA per Amplifier
- High Common-Mode Rejection: 120 dB (Typ)
- Low-Input Bias Current: 8 pA
- *microPackage*: Dual in VSSOP-8
- **Supports Defense, Aerospace, and Medical Applications:**
 - Controlled Baseline
 - One Assembly/Test Site
 - One Fabrication Site
 - Available in Extended (-55°C to 125°C) Temperature Range
 - Extended Product Life Cycle
 - Extended Product-Change Notification
 - Product Traceability

Unity-Gain Buffer With R_{ISO} Stability Compensation



2 Applications

- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Strain Gauge Amplifiers
- Precision Integrators
- Battery-Powered Instruments
- Test Equipment

3 Description

The OPA2171-EP is a 36-V, single-supply, low-noise operational amplifier with the ability to operate on supplies ranging from 2.7 V (± 1.35 V) to 36 V (± 18 V). These devices are available in micro-packages and offer low offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most operational amplifiers, which are specified at only one supply voltage, the OPA2171-EP is specified from 2.7 to 36 V. Input signals beyond the supply rails do not cause phase reversal. The OPA2171-EP is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. Note that these devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

The OPA2171-EP operational amplifier is specified from -55°C to 125°C .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2171-EP	VSSOP (8)	2.30 mm $\times$ 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



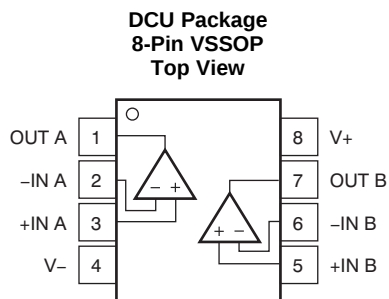
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1 Features	1	7.3 Feature Description.....	14
2 Applications	1	7.4 Device Functional Modes.....	15
3 Description	1	8 Application and Implementation	16
4 Revision History	2	8.1 Application Information.....	16
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6 Specifications	4	9 Power Supply Recommendations	19
6.1 Absolute Maximum Ratings	4	10 Layout	20
6.2 ESD Ratings.....	4	10.1 Layout Guidelines	20
6.3 Recommended Operating Conditions.....	4	10.2 Layout Example	20
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4 Revision History

DATE	REVISION	NOTES
September 2015	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted⁽¹⁾

		MIN	MAX	UNIT
Supply voltage		±20		V
Signal input pins	Voltage	(V ₋) – 0.5	(V ₊) + 0.5	V
	Current	–10	10	mA
Output short circuit ⁽²⁾		Continuous		
Junction temperature			150	°C
Storage temperature, T _{stg}		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V ₊ – V ₋)	4.5 (±2.25)		36 (±18)	V
Operating temperature, T _j	–55		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		OPA2171-EP	UNIT
		DCU (VSSOP)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	175.2	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	74.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	22.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	22.8	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

at $T_J = 25^\circ\text{C}$, $V_S = 2.7$ to 36 V , $V_{CM} = V_{OUT} = V_S / 2$, and $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V _{OS}			0.25	±1.8	mV
Over temperature		T _J = −55°C to 125°C		0.3	±2	mV
Drift	dV _{OS} /dT	T _J = −55°C to 125°C		0.3		μV/°C
vs power supply	PSRR	V _S = 4 to 36 V, T _A = −55°C to 125°C		1	±5	μV/V
Channel separation, dc		dc		5		μV/V
INPUT BIAS CURRENT						
Input bias current	I _B			±8	±15	pA
Over temperature		T _J = −55°C to 125°C			±4	nA
Input offset current	I _{OS}			±4		pA
Over temperature		T _J = −55°C to 125°C			±4	nA
NOISE						
Input voltage noise		f = 0.1 to 10 Hz		3		μV _{PP}
Input voltage noise density	e _n	f = 100 Hz		25		nV/√Hz
		f = 1 kHz		14		nV/√Hz
INPUT VOLTAGE						
Common-mode voltage range ⁽¹⁾	V _{CM}		(V−) − 0.1 V		(V+) − 2 V	V
Common-mode rejection ratio	CMRR	V _S = ±2 V, (V−) − 0.1 V < V _{CM} < (V+) − 2 V, T _J = −55°C to 125°C	87	104		dB
		V _S = ±18 V, (V−) − 0.1 V < V _{CM} < (V+) − 2 V, T _J = −55°C to 125°C	104	120		dB
INPUT IMPEDANCE						
Differential				100 3		MΩ pF
Common-mode				6 3		10 ¹² Ω pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A _{OL}	V _S = 4 to 36 V, (V−) + 0.35 V < V _O < (V+) − 0.35 V, T _J = −55°C to 125°C	110	130		dB
FREQUENCY RESPONSE						
Gain bandwidth product	GBP			3.0		MHz
Slew rate	SR	G = +1		1.5		V/μs
Settling time	t _S	To 0.1%, V _S = ±18 V, G = +1, 10-V step		6		μs
		To 0.01% (12 bit), V _S = ±18 V, G = +1, 10-V step		10		μs
Overload recovery time		V _{IN} × Gain > V _S		2		μs
Total harmonic distortion + noise	THD+N	G = +1, f = 1kHz, V _O = 3V _{RMS}		0.0002%		
OUTPUT						
Voltage output swing from rail	V _O	V _S = 5 V, R _L = 10 kΩ		30		mV
Over temperature		R _L = 10 kΩ, A _{OL} ≥ 110 dB, T _J = −55°C to 125°C	(V−) + 0.35		(V+) − 0.35	V
Short-circuit current	I _{SC}			+25/−35		mA
Capacitive load drive	C _{LOAD}			See Typical Characteristics		pF
Open-loop output resistance	R _O	f = 1 MHz, I _O = 0 A		150		Ω

(1) The input range can be extended beyond $(V+) - 2\text{ V}$ up to $V+$. See [Typical Characteristics](#) and [Application and Implementation](#) for additional information.

Electrical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_S = 2.7$ to 36 V , $V_{CM} = V_{OUT} = V_S / 2$, and $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY					
Specified voltage range V_S		2.7		36	V
Quiescent current per amplifier I_Q	$I_O = 0\text{ A}$		475	595	μA
Over temperature	$I_O = 0\text{ A}$, $T_J = -55^\circ\text{C}$ to 125°C			650	μA
TEMPERATURE					
Operating temperature T_J		-55		125	$^\circ\text{C}$

6.6 Typical Characteristics

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 5
Offset Voltage vs Power Supply	Figure 6
I_B and I_{OS} vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
CMRR and PSRR vs Frequency (Referred-to Input)	Figure 10
CMRR vs Temperature	Figure 11
PSRR vs Temperature	Figure 12
0.1-Hz to 10-Hz Noise	Figure 13
Input Voltage Noise Spectral Density vs Frequency	Figure 14
THD+N Ratio vs Frequency	Figure 15
THD+N vs Output Amplitude	Figure 16
Quiescent Current vs Temperature	Figure 17
Quiescent Current vs Supply Voltage	Figure 18
Open-Loop Gain and Phase vs Frequency	Figure 19
Closed-Loop Gain vs Frequency	Figure 20
Open-Loop Gain vs Temperature	Figure 21
Open-Loop Output Impedance vs Frequency	Figure 22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 23 , Figure 24
No Phase Reversal	Figure 25
Positive Overload Recovery	Figure 26
Negative Overload Recovery	Figure 27
Small-Signal Step Response (100 mV)	Figure 28 , Figure 29
Large-Signal Step Response	Figure 30 , Figure 31
Large-Signal Settling Time (10-V Positive Step)	Figure 32
Large-Signal Settling Time (10-V Negative Step)	Figure 33
Short-Circuit Current vs Temperature	Figure 34
Maximum Output Voltage vs Frequency	Figure 35
Channel Separation vs Frequency	Figure 36

$V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

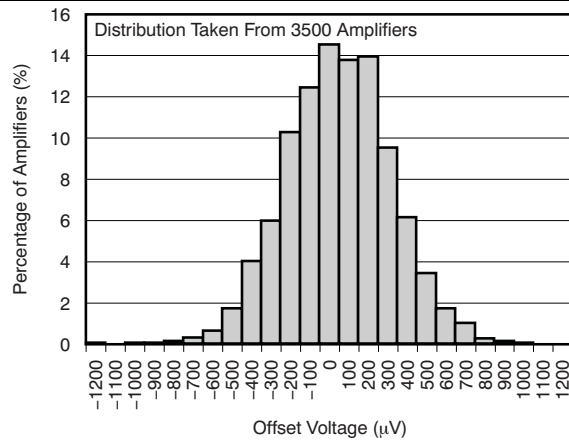


Figure 1. Offset Voltage Production Distribution

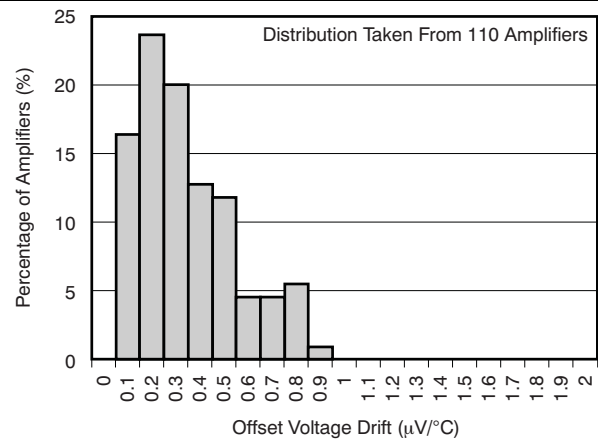


Figure 2. Offset Voltage Drift Distribution

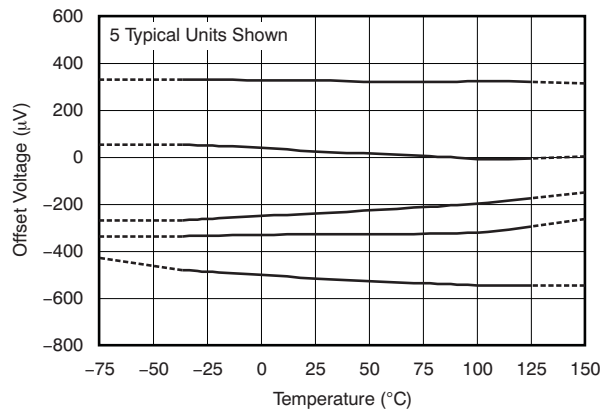


Figure 3. Offset Voltage vs Temperature

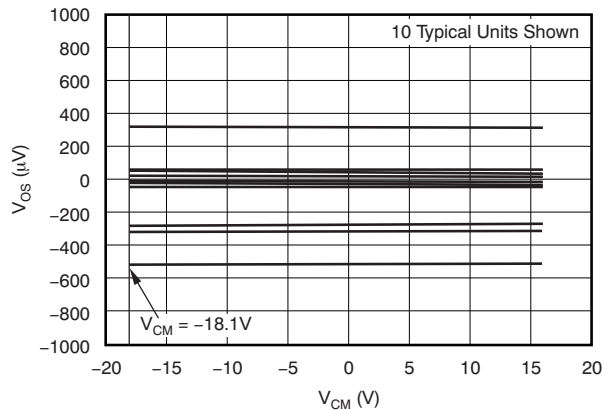


Figure 4. Offset Voltage vs Common-Mode Voltage

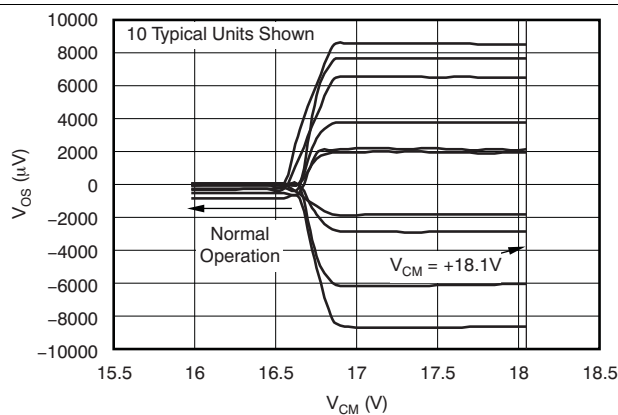


Figure 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

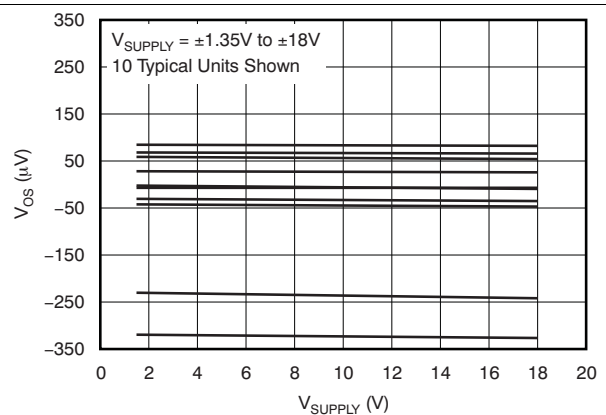


Figure 6. Offset Voltage vs Power Supply

$V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

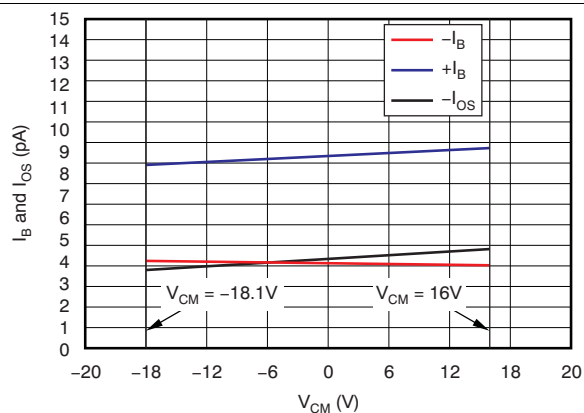


Figure 7. I_B and I_{OS} vs Common-Mode Voltage

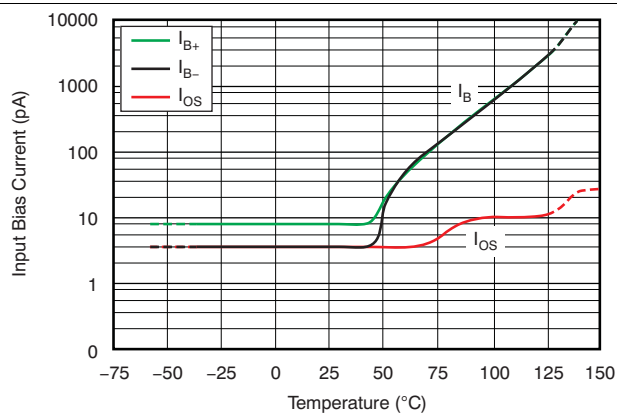


Figure 8. Input Bias Current vs Temperature

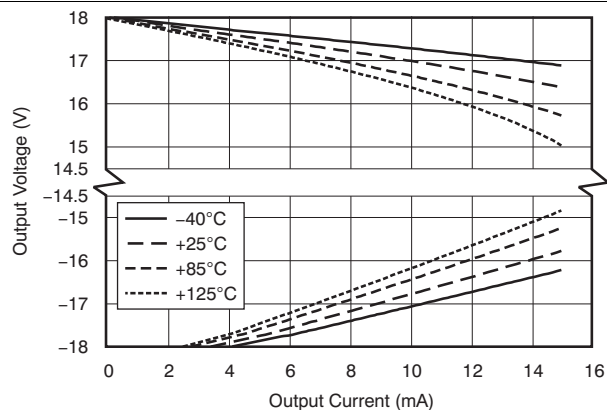


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

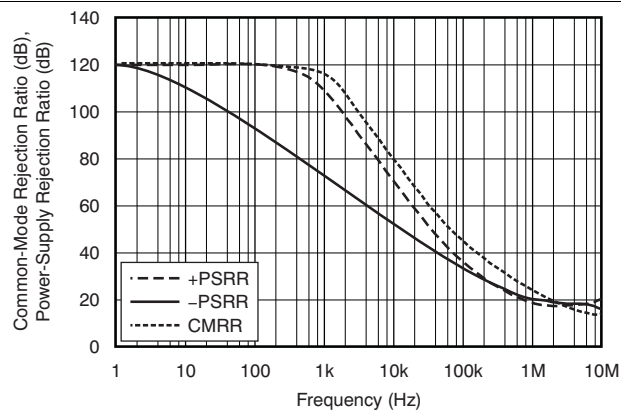


Figure 10. CMRR and PSRR vs Frequency (Referred-to Input)

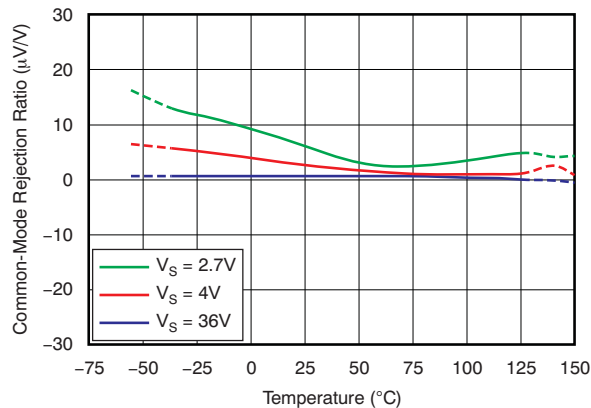


Figure 11. CMRR vs Temperature

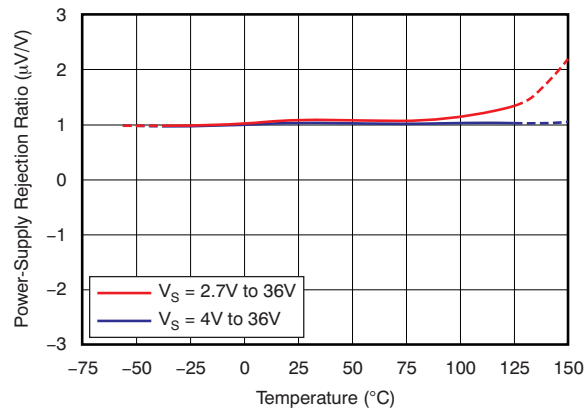


Figure 12. PSRR vs Temperature

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$V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

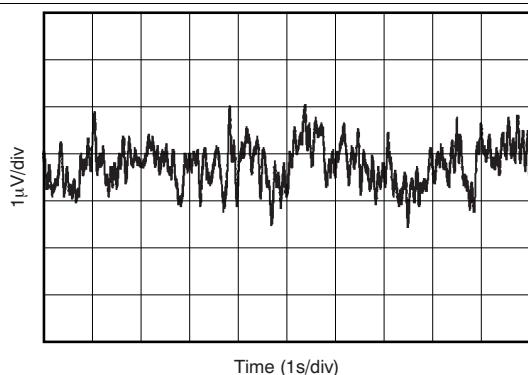


Figure 13. 0.1-Hz to 10-Hz Noise

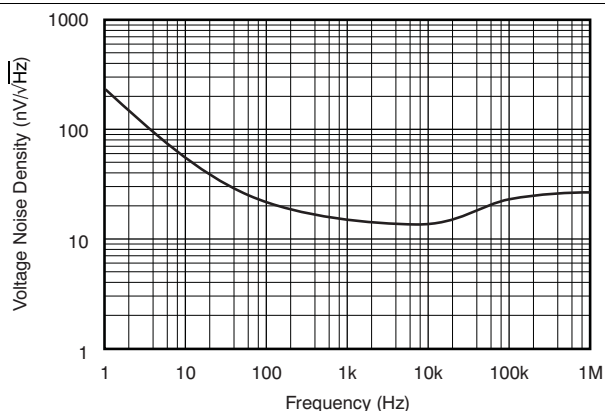


Figure 14. Input Voltage Noise Spectral Density vs Frequency

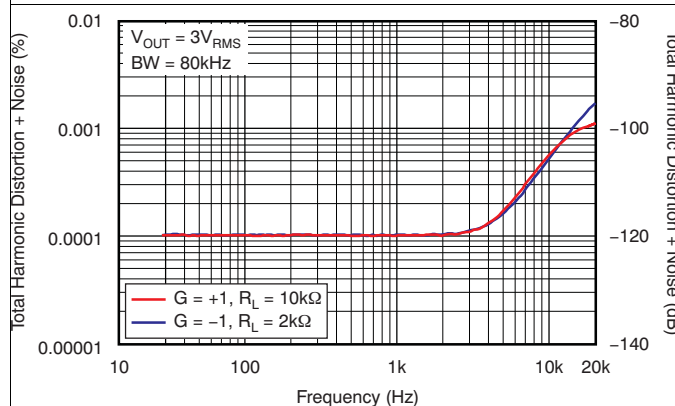


Figure 15. THD+N Ratio vs Frequency

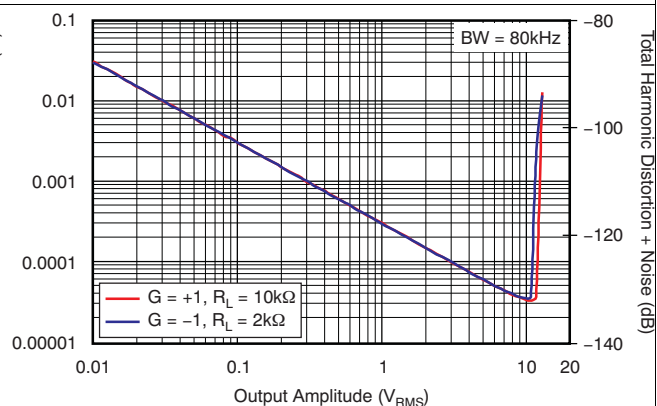


Figure 16. THD+N vs Output Amplitude

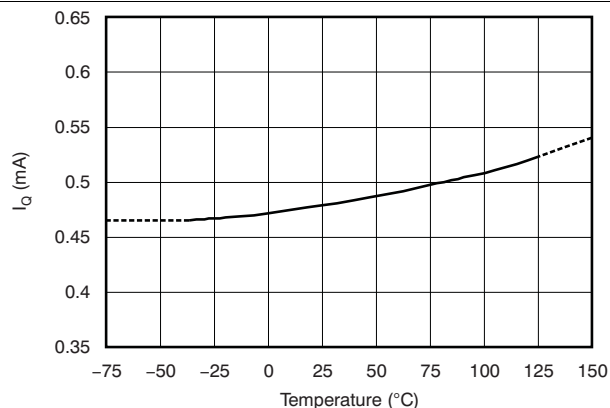


Figure 17. Quiescent Current vs Temperature

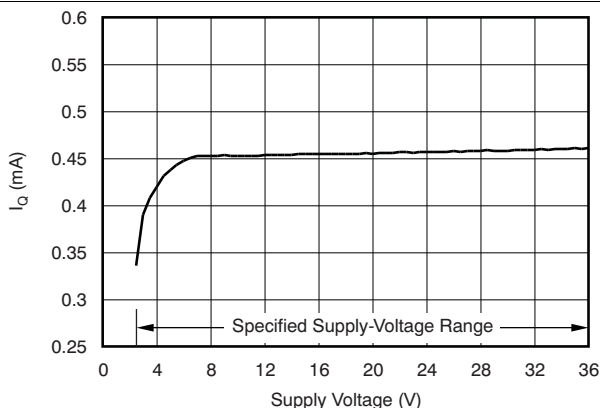


Figure 18. Quiescent Current vs Supply Voltage

$V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

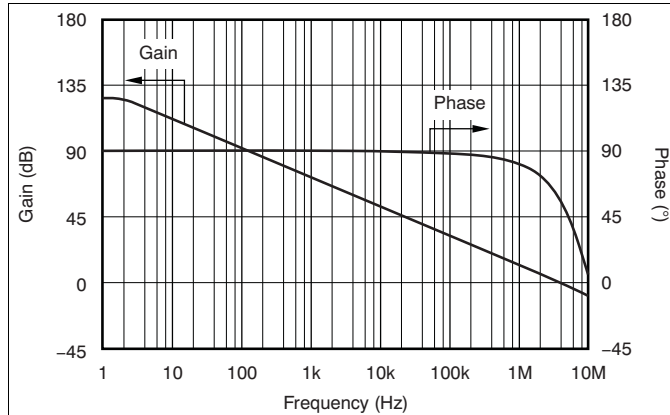


Figure 19. Open-Loop Gain and Phase vs Frequency

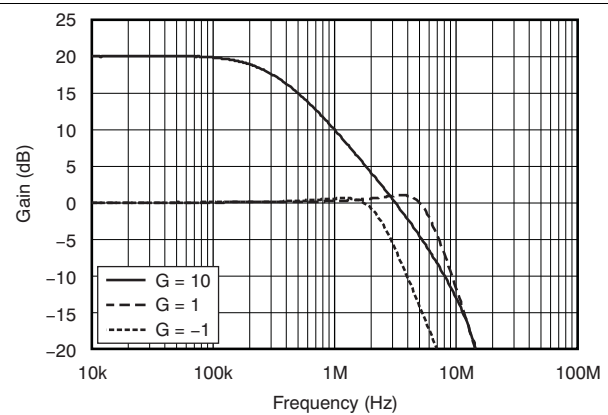


Figure 20. Closed-Loop Gain vs Frequency

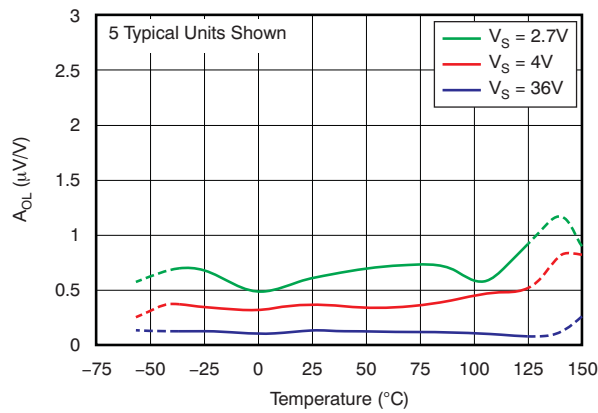


Figure 21. Open-Loop Gain vs Temperature

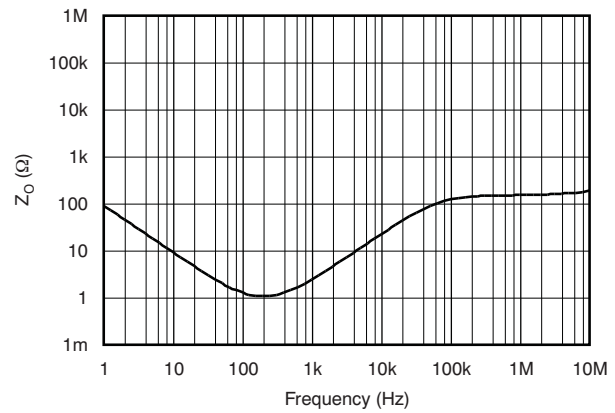


Figure 22. Open-Loop Output Impedance vs Frequency

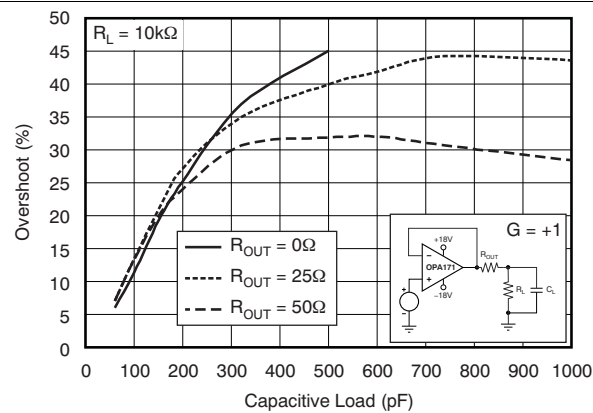


Figure 23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

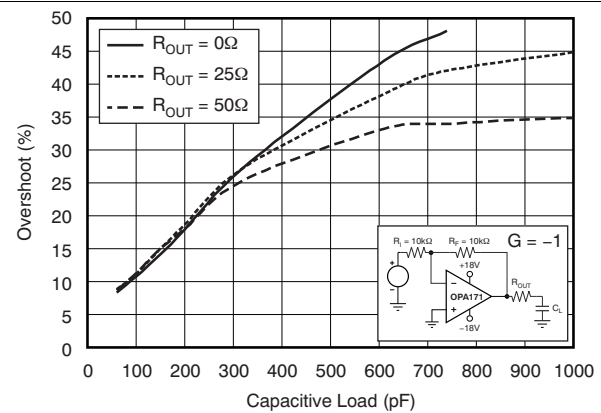


Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

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$V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

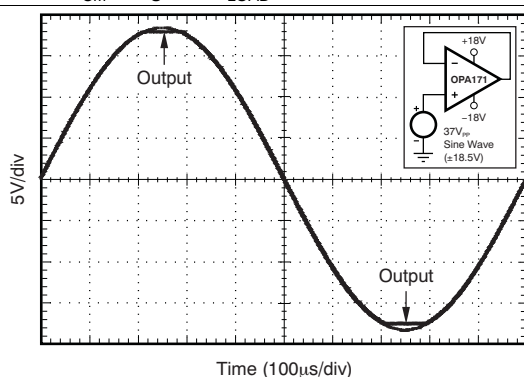


Figure 25. No Phase Reversal

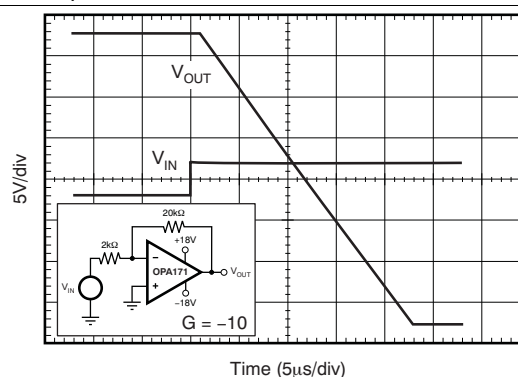


Figure 26. Positive Overload Recovery

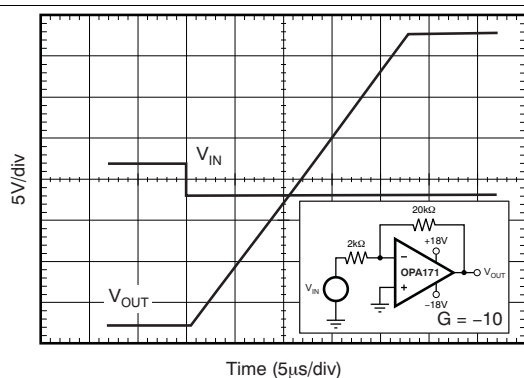


Figure 27. Negative Overload Recovery

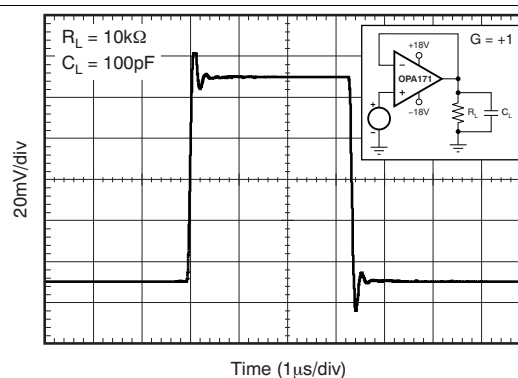


Figure 28. Small-Signal Step Response (100 mV)

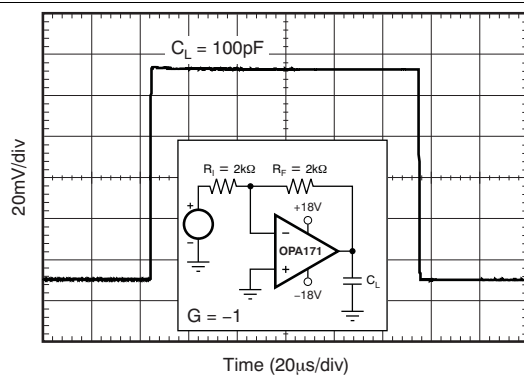


Figure 29. Small-Signal Step Response (100 mV)

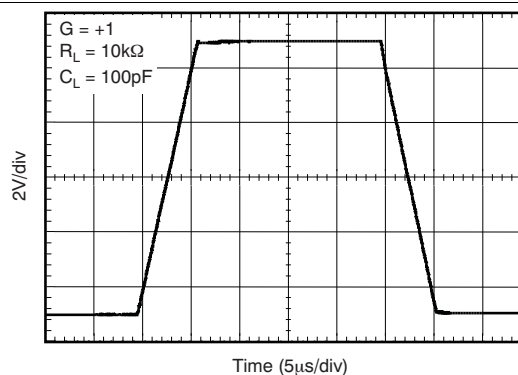


Figure 30. Large-Signal Step Response

$V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$, unless otherwise noted.

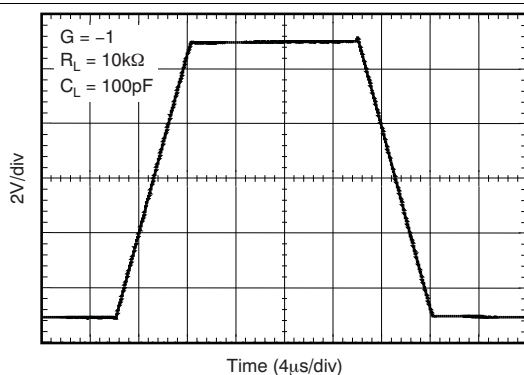


Figure 31. Large-Signal Step Response

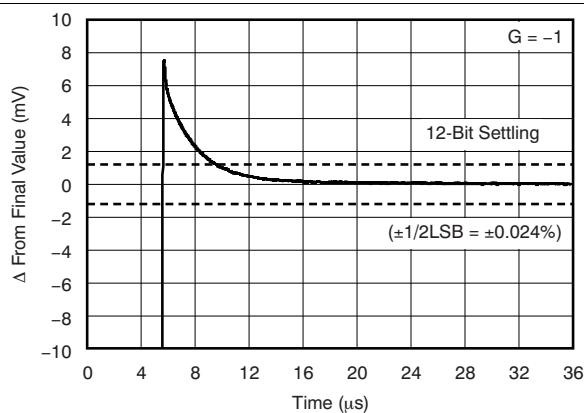


Figure 32. Large-Signal Settling Time (10-V Positive Step)

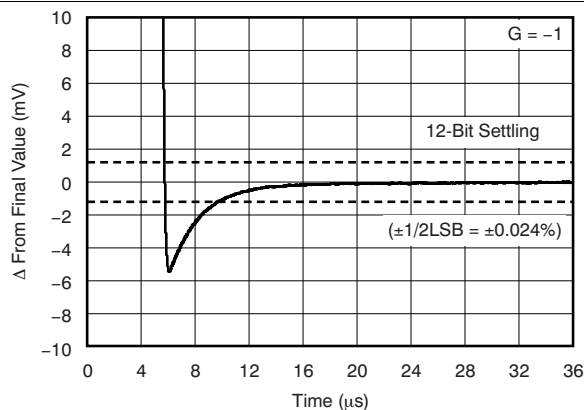


Figure 33. Large-Signal Settling Time (10-V Negative Step)

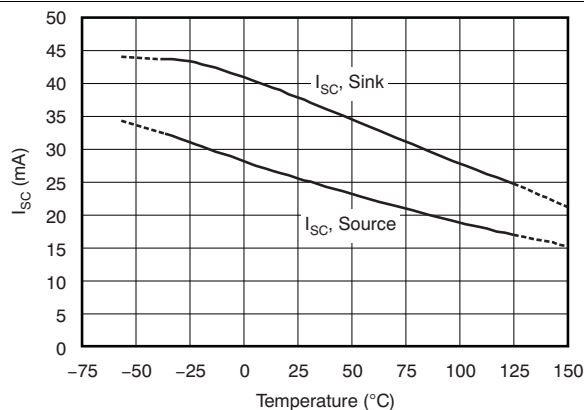


Figure 34. Short-Circuit Current vs Temperature

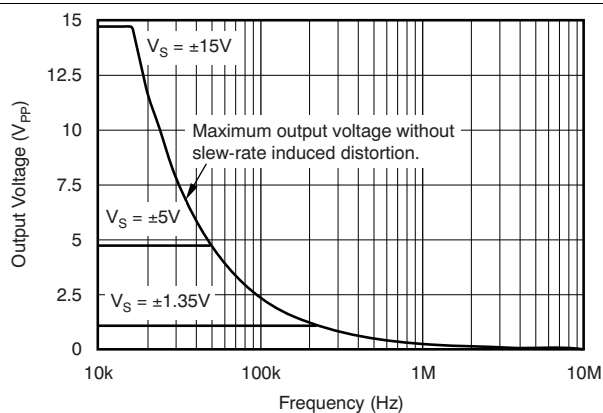


Figure 35. Maximum Output Voltage vs Frequency

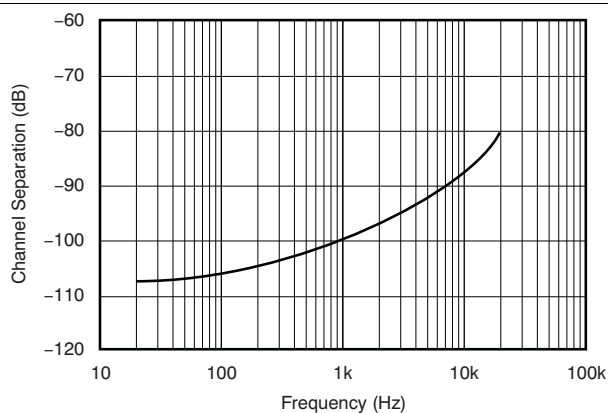


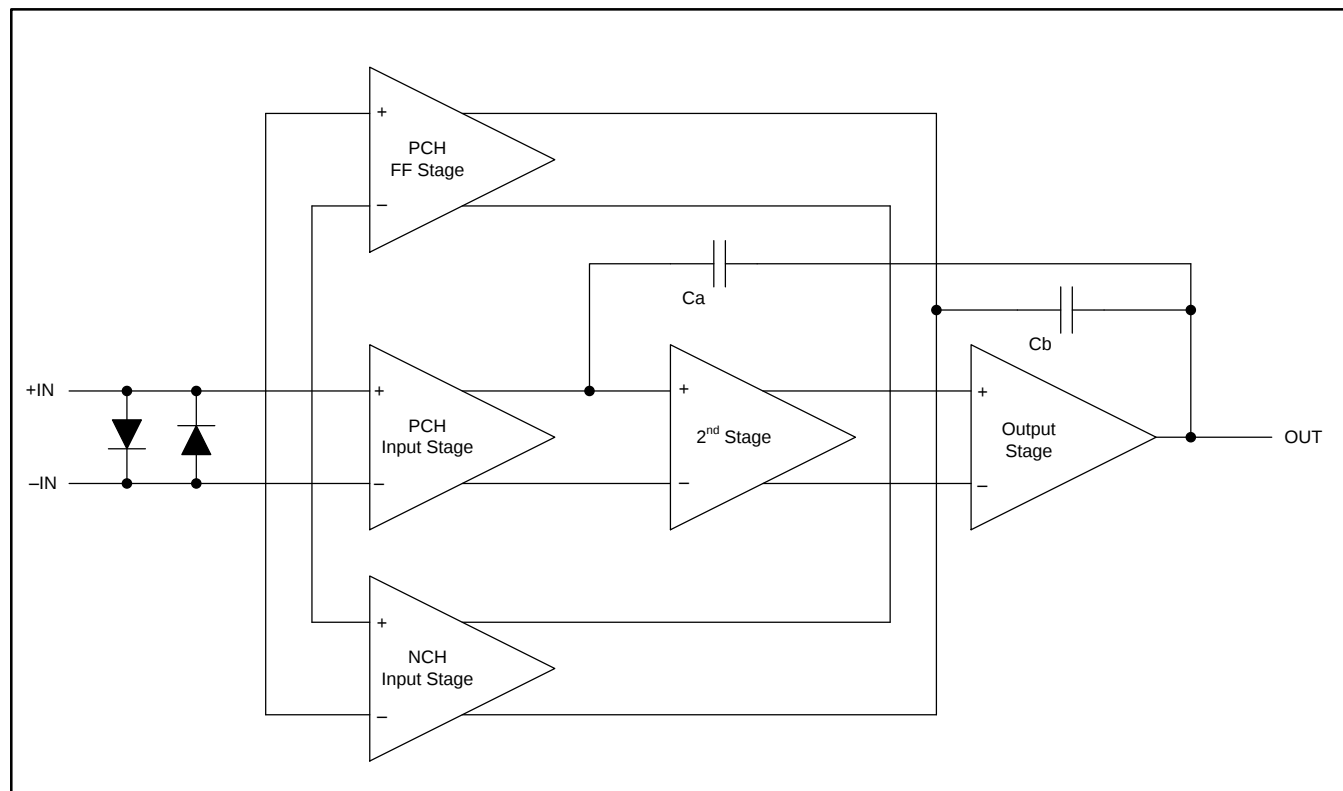
Figure 36. Channel Separation vs Frequency

7 Detailed Description

7.1 Overview

The OPA2171-EP operational amplifier provides high overall performance, making it ideal for many general-purpose applications. The excellent offset drift of only 2 $\mu\text{V}/^\circ\text{C}$ provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL} . As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1- μF capacitors are adequate.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPA2171-EP amplifier is specified for operation from 2.7 to 36 V (± 1.35 to ± 18 V). Many of the specifications apply from -55°C to 125°C . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in [Typical Characteristics](#).

7.3.2 Phase-Reversal Protection

The OPA2171-EP has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA2171-EP prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. [Figure 37](#) shows this performance.

Feature Description (continued)

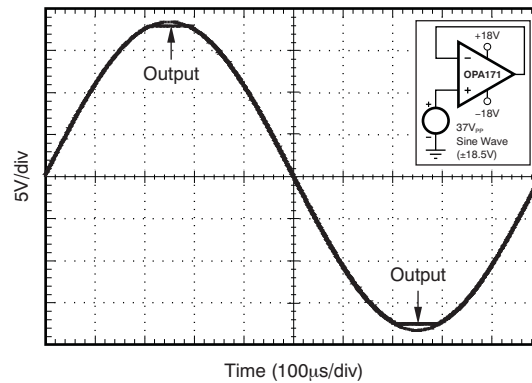


Figure 37. No Phase Reversal

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPA2171-EP extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. [Table 2](#) summarizes the typical performance in this range.

Table 2. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
vs Temperature		12		µV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/µs
Noise at $f = 1\text{kHz}$		30		nV/√Hz

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Electrical Overstress

Designers often ask about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in [Absolute Maximum Ratings](#). Figure 38 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

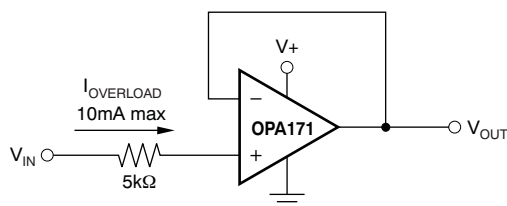


Figure 38. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins. Select the Zener voltage such that the diode does not turn on during normal operation.

However, its Zener voltage should be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

8.2 Typical Application

Figure 39 shows a capacitive load drive solution using an isolation resistor. The OPA2171-EP device can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open loop gain of the system to ensure the circuit has sufficient phase margin.

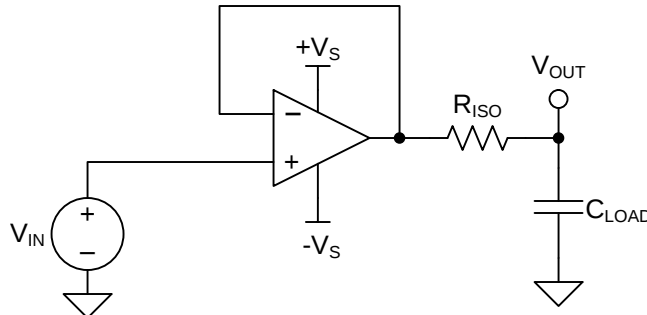


Figure 39. Unity-Gain Buffer with R_{ISO} Stability Compensation

8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (± 15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 μ F, 0.1 μ F, and 1 μ F
- Phase margin: 45° and 60°

8.2.2 Detailed Design Procedure

Figure 39 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 39. Not shown in Figure 39 is the open-loop output resistance of the op amp, R_o .

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by $(R_o + R_{ISO})$ and C_{LOAD} . Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and $1/\beta$ is 20 dB/decade. Figure 40 depicts the concept. The $1/\beta$ curve for a unity-gain buffer is 0 dB.

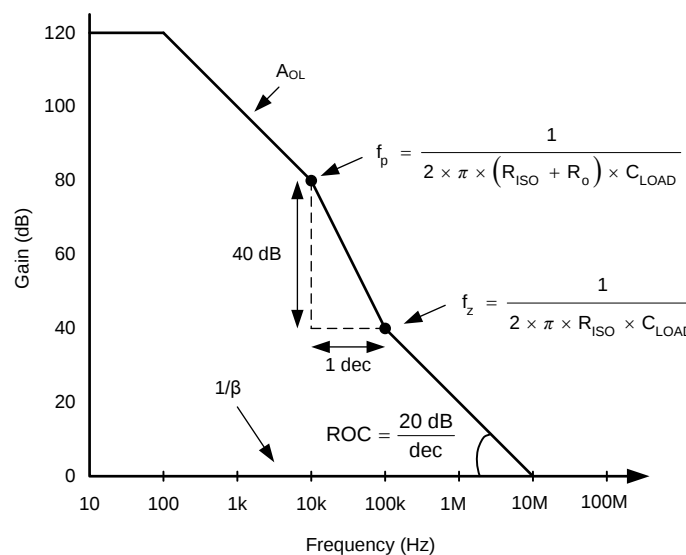


Figure 40. Unity-Gain Amplifier with R_{ISO} Compensation

Typical Application (continued)

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o . In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60° . For more details on this design and other alternative devices that can be used in place of the OPA171, refer to the Precision Design, *Capacitive Load Drive Solution using an Isolation Resistor (TIPD128)*.

Table 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.2.1 Capacitive Load and Stability

The dynamic characteristics of the OPA2171-EP have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to $50\ \Omega$) in series with the output. Figure 41 and Figure 42 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT} . Also, refer to *Applications Bulletin AB-028 (SBOA015)*, available for download from www.ti.com for details of analysis techniques and application circuits.

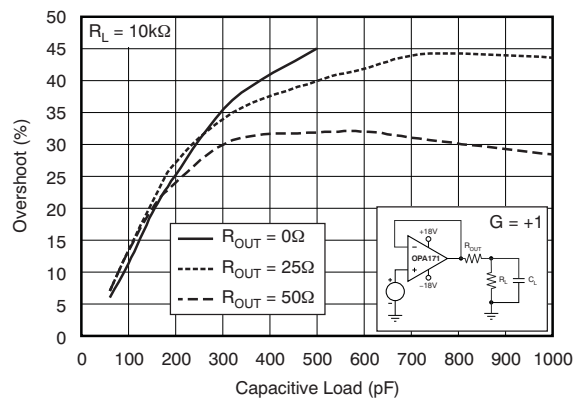


Figure 41. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

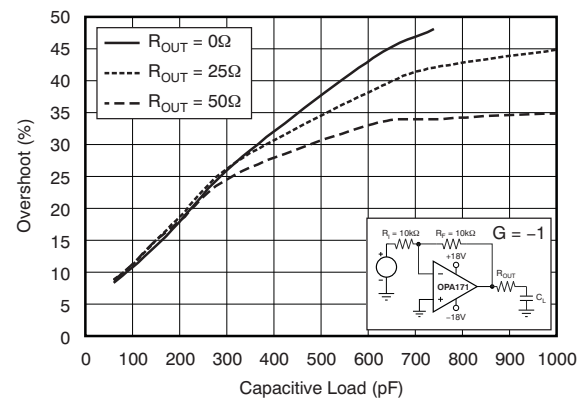


Figure 42. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8.2.3 Application Curve

The OPA2171-EP device meets the supply voltage requirements of 30 V. The OPA2171-EP device was tested for various capacitive loads and R_{ISO} was adjusted to achieve an overshoot corresponding to [Table 3](#). [Figure 43](#) shows the test results.

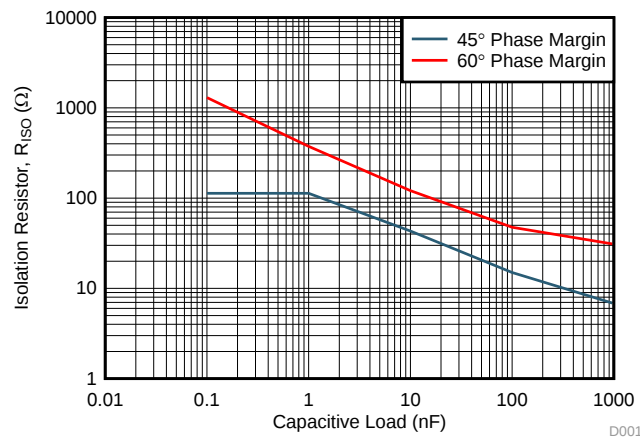


Figure 43. R_{ISO} vs C_{LOAD}

9 Power Supply Recommendations

The OPA2171-EP is specified for operation from 4.5 V to 36 V (± 2.25 V to ± 18 V); many specifications apply from -40°C to 125°C . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For detailed information on bypass capacitor placement, see the [Layout](#) section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, TI recommends good printed circuit board (PCB) layout practices. Low-loss, 0.1- μ F bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

10.2 Layout Example

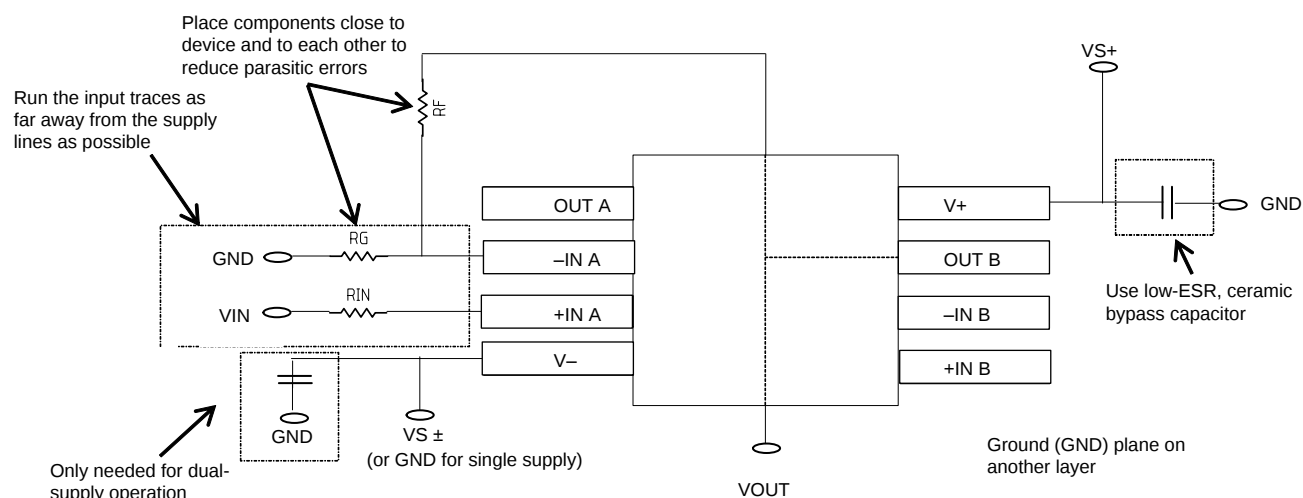


Figure 44. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2171MDCUTEP	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ZGAA
OPA2171MDCUTEP.A	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ZGAA
V62/15605-01XE	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ZGAA

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2171-EP :

- Catalog : [OPA2171](#)

- Automotive : [OPA2171-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


*All dimensions are nominal

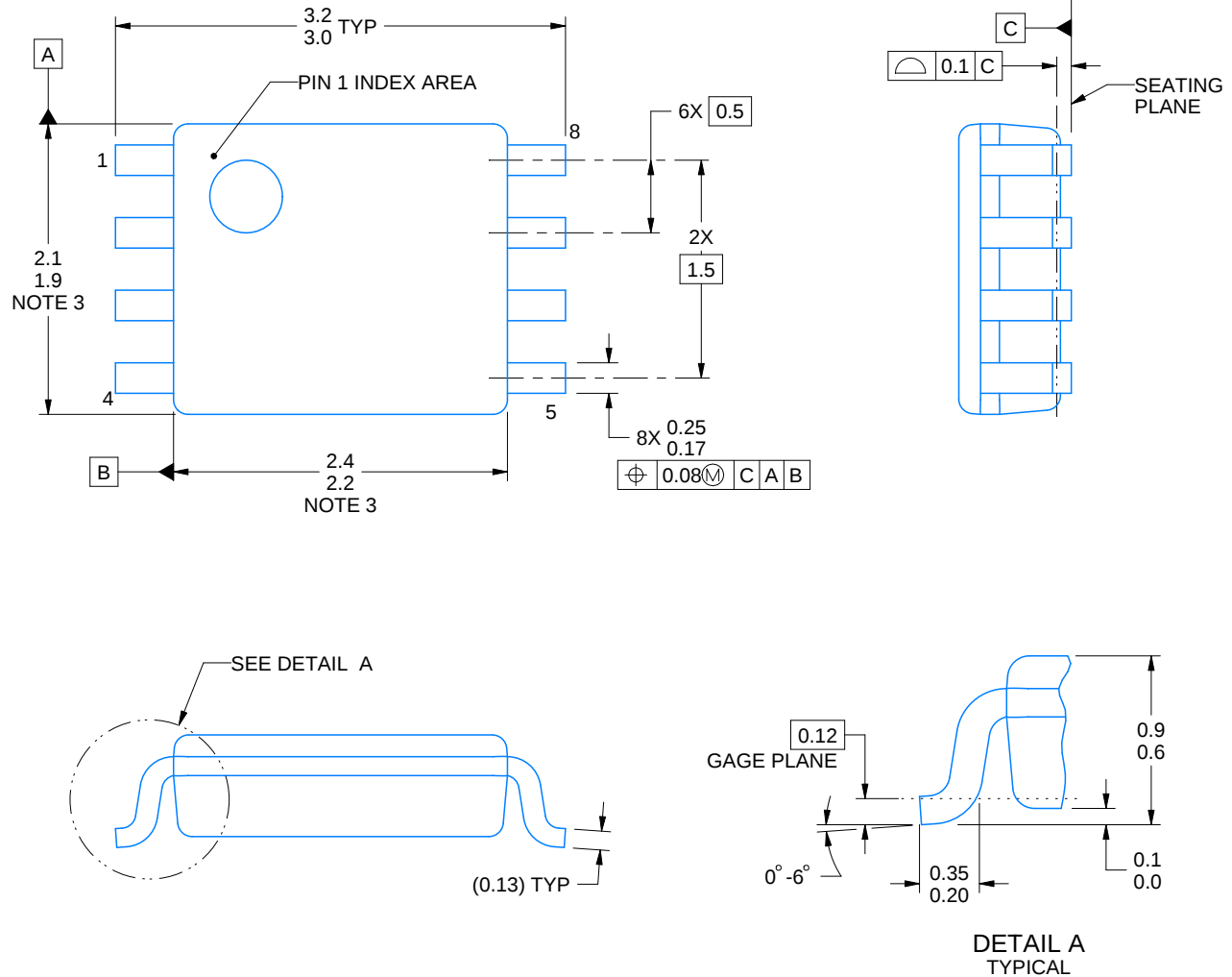
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2171MDCUTEP	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2171MDCUTEP	VSSOP	DCU	8	250	202.0	201.0	28.0



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NOTES:

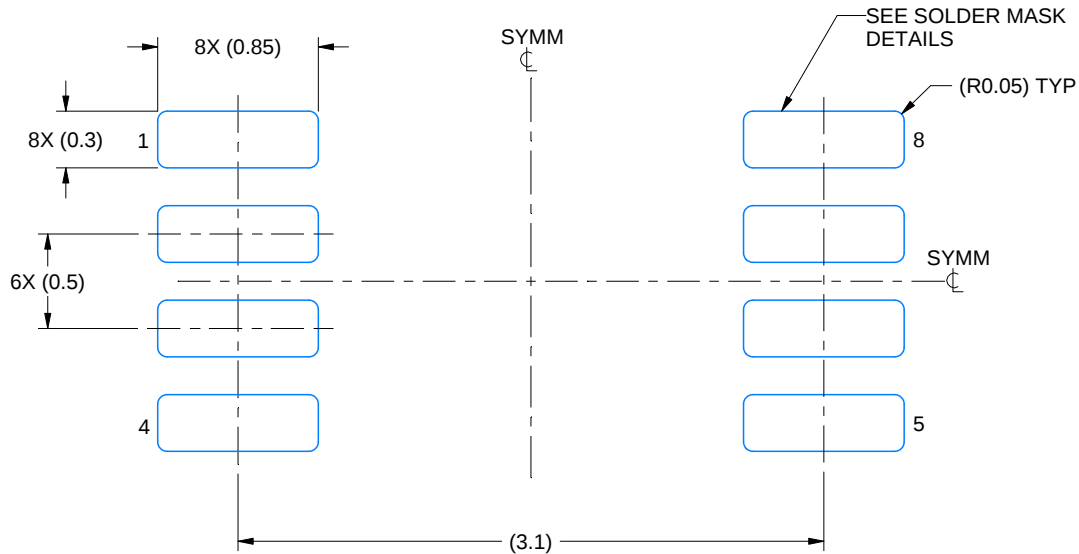
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

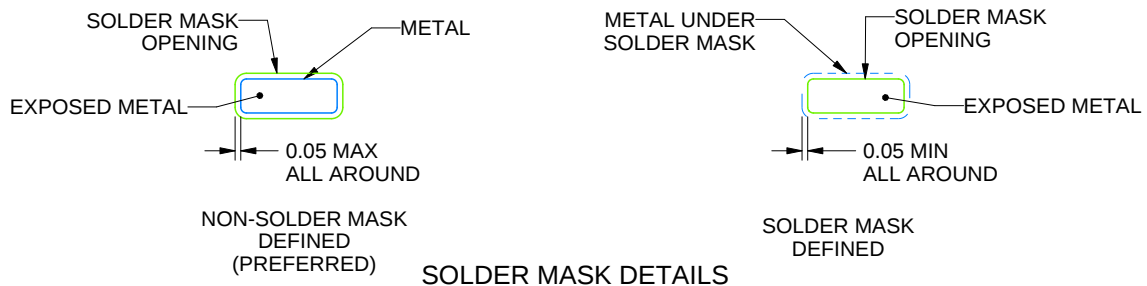
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

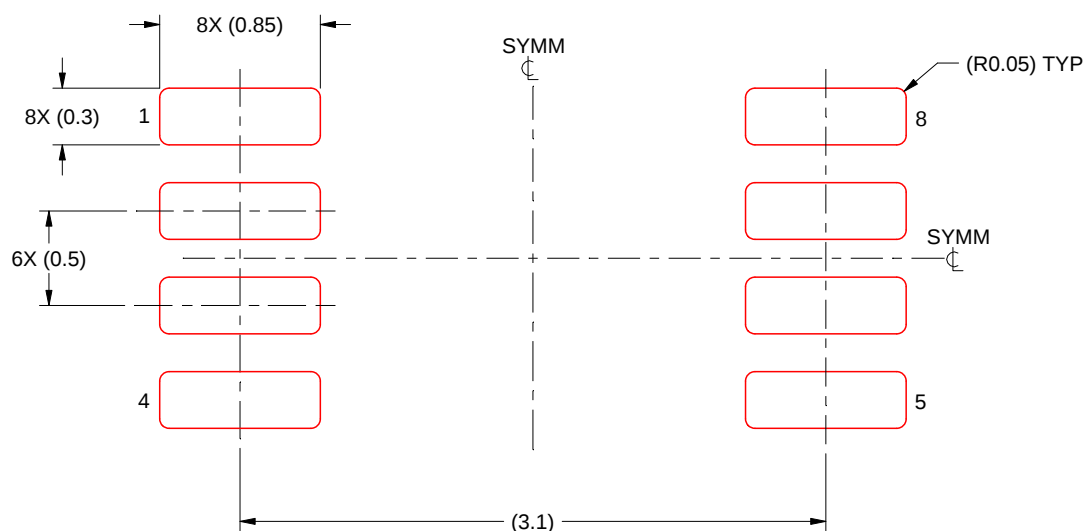
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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