

DATA SHEET

PDTC114Y series
NPN resistor-equipped transistors;
 $R1 = 10 \text{ k}\Omega$, $R2 = 47 \text{ k}\Omega$

Product specification
Supersedes data of 1999 May 21

2003 Apr 14

**NPN resistor-equipped transistors;
R1 = 10 kΩ, R2 = 47 kΩ**

PDTC114Y series

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	–	50	V
I_o	output current (DC)	–	100	mA
R1	bias resistor	10	–	kΩ
R2	bias resistor	47	–	kΩ

DESCRIPTION

NPN resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP COMPLEMENT
	PHILIPS	EIAJ		
PDTC114YE	SOT416	SC-75	33	–
PDTC114YK	SOT346	SC-59	47	PDTA114YK
PDTC114YM	SOT883	SC-101	DU	PDTA114YM
PDTC114YS	SOT54 (TO-92)	SC-43	TC114Y	PDTA114YS
PDTC114YT	SOT23	–	*27 ⁽¹⁾	PDTA114YT
PDTC114YU	SOT323	SC-70	*30 ⁽¹⁾	PDTA114YU

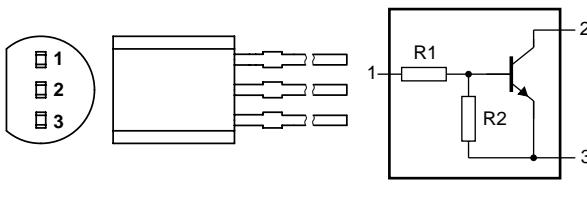
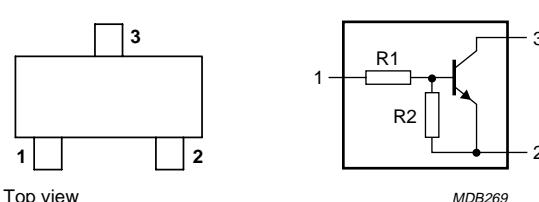
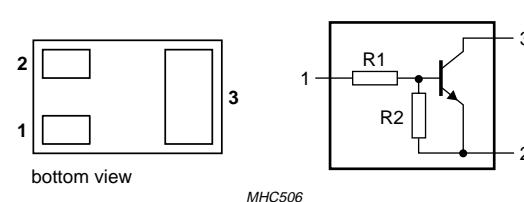
Note

1. * = p: Made in Hong Kong.
- * = t: Made in Malaysia.
- * = W: Made in China.

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTC114YS		1 2 3	base collector emitter
PDTC114YE PDTC114YK PDTC114YT PDTC114YU		1 2 3	base emitter collector
PDTC114YM		1 2 3	base emitter collector

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage positive negative		– –	+40 –6	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation SOT54 SOT23 SOT346 SOT323 SOT416 SOT883	T _{amb} ≤ 25 °C note 1 note 1 note 1 note 1 note 1 notes 2 and 3	– – – – – –	500 250 250 200 150 250	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 µm copper strip line.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient SOT54 SOT23 SOT346 SOT323 SOT416 SOT883	in free air note 1 note 1 note 1 note 1 note 1 notes 2 and 3	250 500 500 625 833 500	K/W

Notes

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2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 µm copper strip line.

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CHARACTERISTICS

$T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{\text{CB}} = 50 \text{ V}$; $I_E = 0$	—	—	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{\text{CE}} = 30 \text{ V}$; $I_B = 0$	—	—	1	μA
		$V_{\text{CE}} = 30 \text{ V}$; $I_B = 0$; $T_j = 150 \text{ }^{\circ}\text{C}$	—	—	50	μA
I_{EBO}	emitter-base cut-off current	$V_{\text{EB}} = 5 \text{ V}$; $I_C = 0$	—	—	150	μA
h_{FE}	DC current gain	$V_{\text{CE}} = 5 \text{ V}$; $I_C = 5 \text{ mA}$	100	—	—	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5 \text{ mA}$; $I_B = 0.25 \text{ mA}$	—	—	100	mV
$V_{i(\text{off})}$	input-off voltage	$I_C = 100 \mu\text{A}$; $V_{\text{CE}} = 5 \text{ V}$	—	0.7	0.5	V
$V_{i(\text{on})}$	input-on voltage	$I_C = 1 \text{ mA}$; $V_{\text{CE}} = 0.3 \text{ V}$	1.4	0.8	—	V
$R1$	input resistor		7	10	13	$\text{k}\Omega$
$\frac{R2}{R1}$	resistor ratio		3.7	4.7	5.7	
C_c	collector capacitance	$I_E = i_e = 0$; $V_{\text{CB}} = 10 \text{ V}$; $f = 1 \text{ MHz}$	—	—	2.5	pF

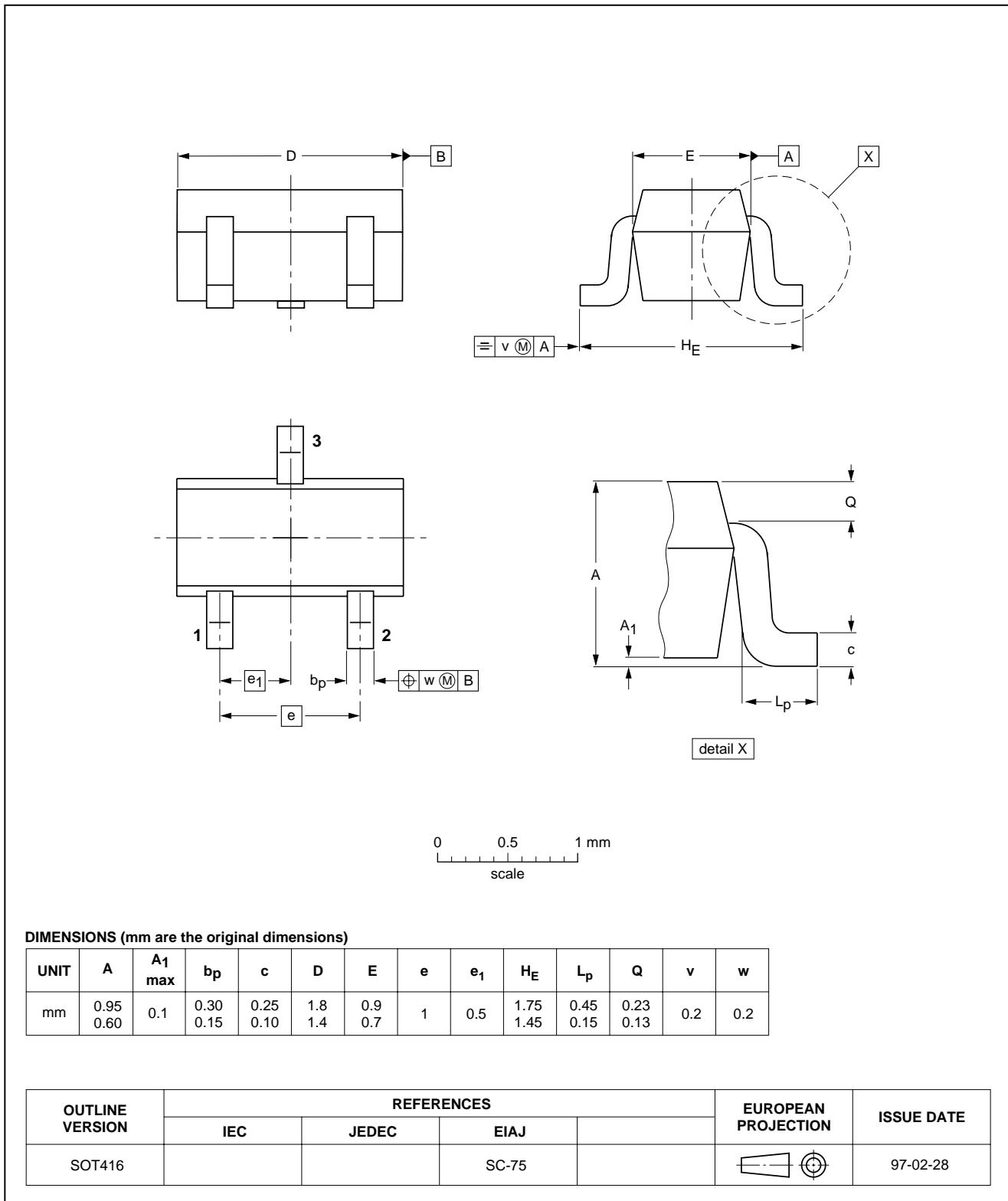
NPN resistor-equipped transistors;
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PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT416

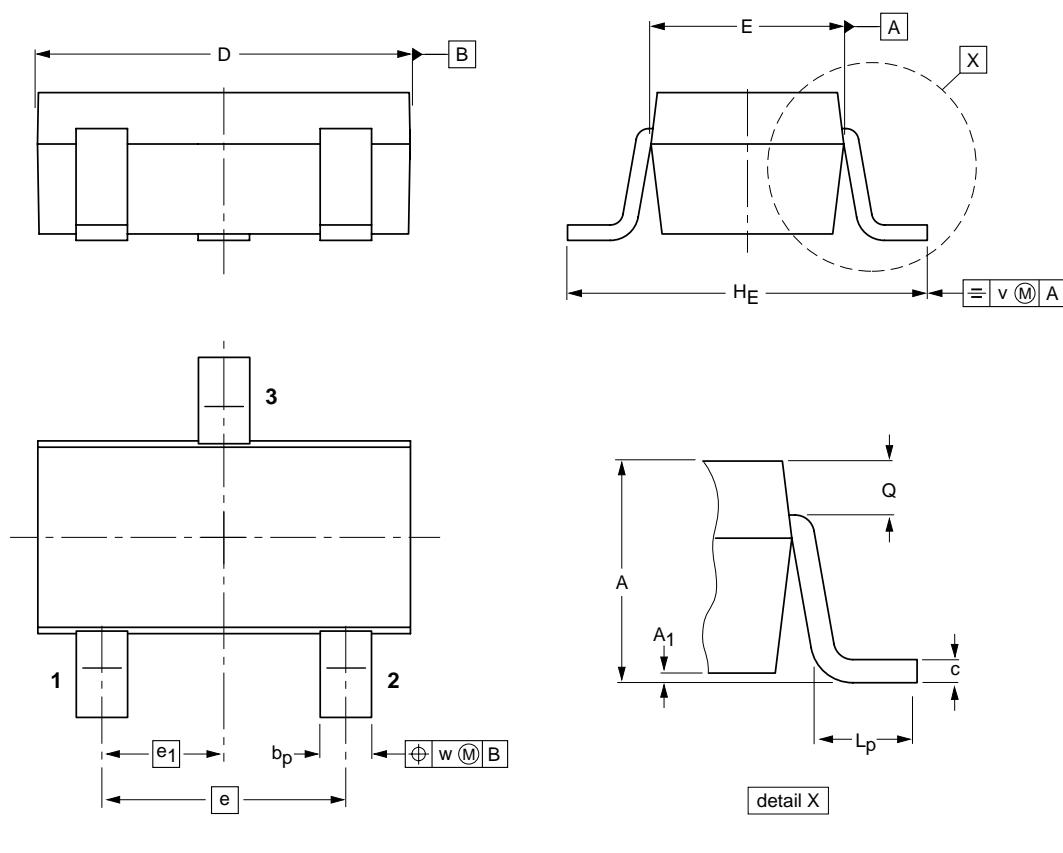


NPN resistor-equipped transistors;
 R1 = 10 k Ω , R2 = 47 k Ω

PDTC114Y series

Plastic surface mounted package; 3 leads

SOT346



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.3	0.1	0.50	0.26	3.1	1.7	1.9	0.95	3.0	0.6	0.33	0.2	0.2
	1.0	0.013	0.35	0.10	2.7	1.3	1.9	0.95	2.5	0.2	0.23		

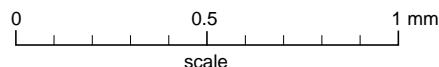
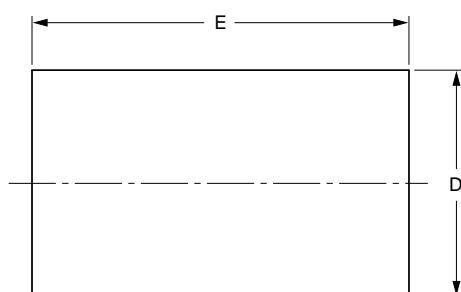
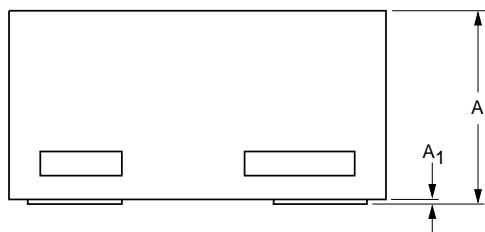
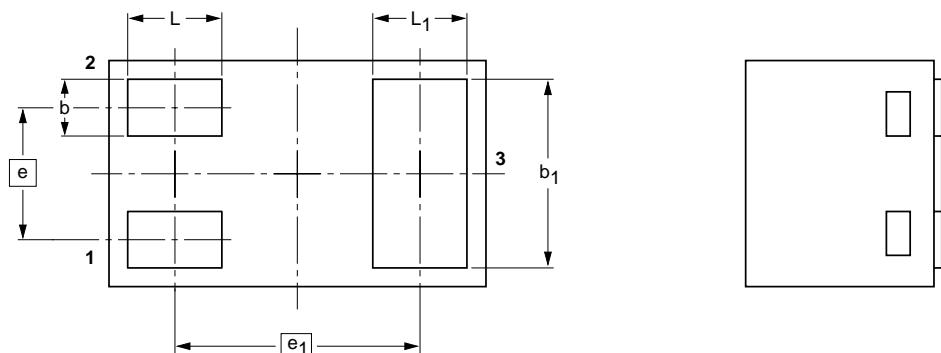
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT346		TO-236	SC-59			98-07-17

NPN resistor-equipped transistors;
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PDTC114Y series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₁ max.	b	b ₁	D	E	e	e ₁	L	L ₁
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

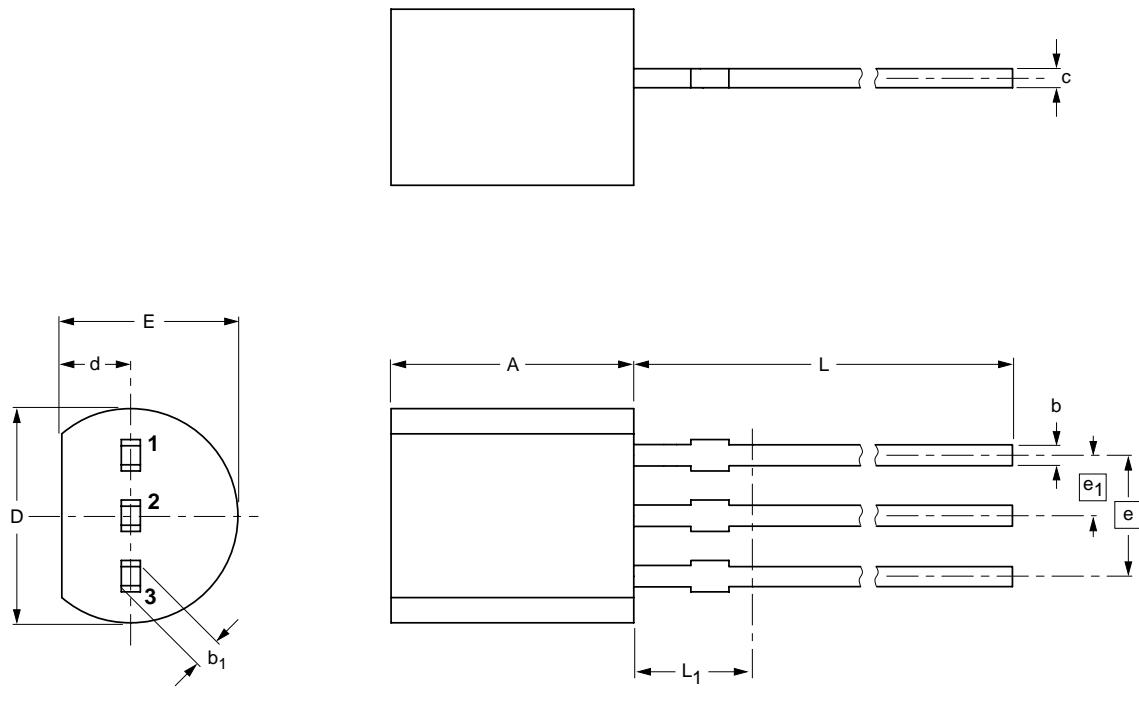
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA	SC-101		
SOT883						03-02-05- 03-04-03

NPN resistor-equipped transistors;
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PDTC114Y series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾
mm	5.2	0.48	0.66	0.45	4.8	1.7	4.2	2.54	1.27	14.5	
	5.0	0.40	0.56	0.40	4.4	1.4	3.6			12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

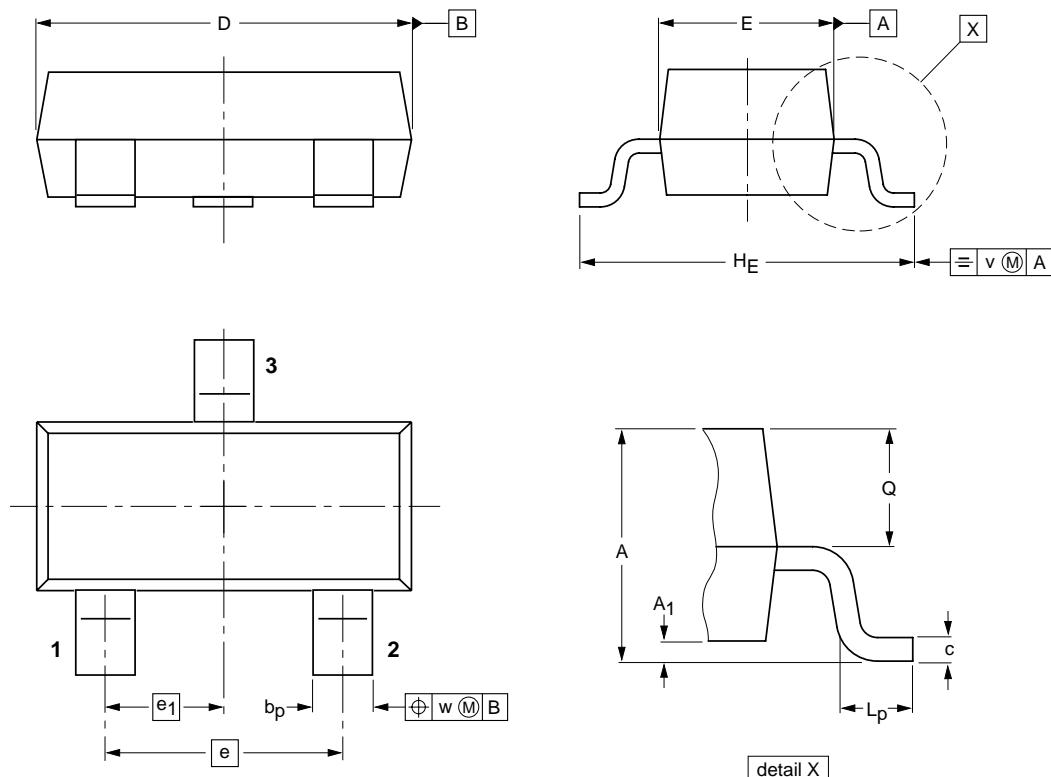
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

NPN resistor-equipped transistors;
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Plastic surface mounted package; 3 leads

SOT23



0 1 2 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

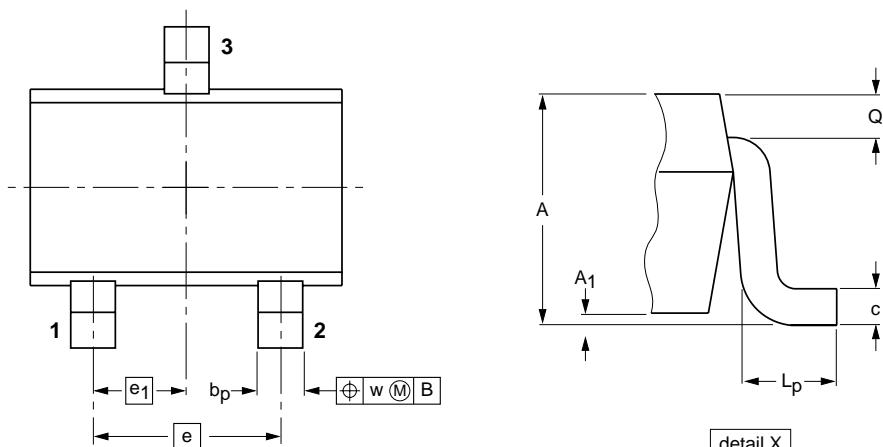
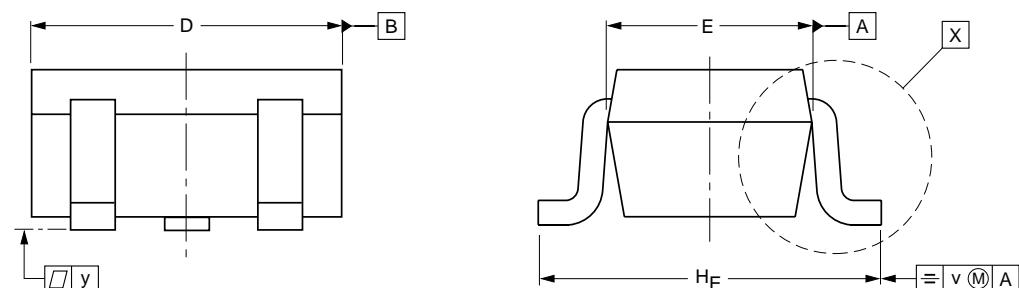
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				-97-02-28 99-09-13

NPN resistor-equipped transistors;
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PDTC114Y series

Plastic surface mounted package; 3 leads

SOT323



0 1 2 mm
 scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ	SC-70		
SOT323						97-02-28

NPN resistor-equipped transistors;
 R1 = 10 kΩ, R2 = 47 kΩ

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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NOTES

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