

# LM3880 Three-Rail Simple Power Supply Sequencer

## 1 Features

- Simple solution for sequencing three voltage rails from a single input signal
- Easily cascade up to three devices to sequence as many as nine voltage rails
- Powerup and powerdown control
- Tiny 2.9-mm x 1.6-mm footprint
- Low quiescent current: 25  $\mu$ A
- Input voltage range: 2.7 V to 5.5 V
- Standard timing options available

## 2 Applications

- Advanced driver assistance systems (ADAS)
- Automotive camera modules
- Security cameras
- Servers
- Networking elements
- FPGA power supply sequencing
- Microprocessor and microcontroller sequencing
- Multiple supply sequencing

## 3 Description

The LM3880 simple power supply sequencer offers the easiest method to control powerup sequencing and powerdown sequencing of multiple Independent voltage rails. By staggering the startup sequence, it is possible to avoid latch conditions or large in-rush currents that can affect the reliability of the system.

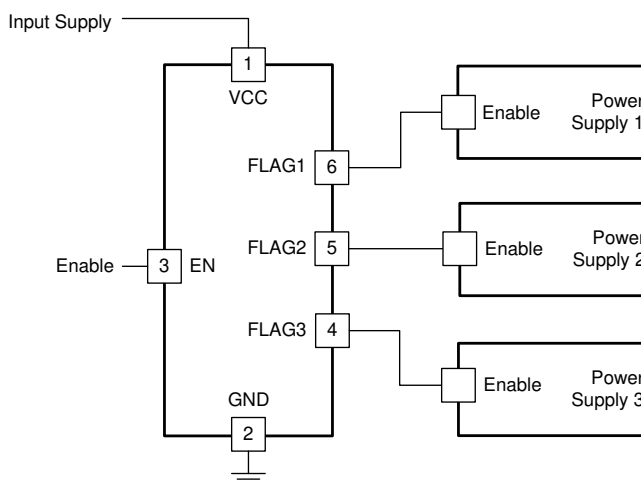
Available in a 6-pin SOT-23 package, the simple sequencer contains a precision enable pin and three open-drain output flags. The open-drain output flags permit that they can be pulled up to distinct voltage supplies separate from the sequencer  $V_{DD}$  (only if they do not exceed the recommended maximum voltage of 0.3 V greater than  $V_{DD}$ ), so as to interface with ICs requiring a range of different enable signals. When the LM3880 is enabled, the three output flags sequentially release, after individual time delays, thus permitting the connected power supplies to start up. The output flags follow a reverse sequence during power down to avoid latch conditions.

EPROM capability allows every delay and sequence to be fully adjustable. Contact Texas Instruments to request a non-standard configuration.

### Device Information (1)

| PART NUMBER | PACKAGE     | BODY SIZE (NOM)   |
|-------------|-------------|-------------------|
| LM3880      | DBV SOT (6) | 2.90 mm x 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



**Simple Power Supply Sequencing**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision L (November 2018) to Revision M (March 2021)</b> | <b>Page</b> |
|---------------------------------------------------------------------------|-------------|
| • Specified device dimensions in <a href="#">Features</a> section.....    | <b>1</b>    |
| • Updated application curve titles.....                                   | <b>14</b>   |

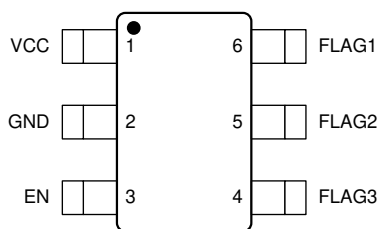
| <b>Changes from Revision K (February 2016) to Revision L (November 2018)</b>                                   | <b>Page</b> |
|----------------------------------------------------------------------------------------------------------------|-------------|
| • Updated <a href="#">Features</a> section to specify how many rails can be sequenced by a single device ..... | <b>1</b>    |
| • Added feature that devices can be cascaded .....                                                             | <b>1</b>    |
| • Specified device dimensions in <a href="#">Features</a> section.....                                         | <b>1</b>    |
| • Specified FPGA Power Supply Sequencing in Applications.....                                                  | <b>1</b>    |
| • Added note in description about open drain FLAG pins.....                                                    | <b>1</b>    |
| • Added I/O column to <i>Pin Functions</i> table.....                                                          | <b>3</b>    |
| • Changed <i>Part Nomenclature</i> section to <i>Device Nomenclature</i> section.....                          | <b>19</b>   |

| <b>Changes from Revision J (December 2014) to Revision K (February 2016)</b>                                                 | <b>Page</b> |
|------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Changed <i>Handling Ratings</i> to <i>ESD Ratings</i> and moved storage temperature to <i>Absolute Maximum Ratings</i> ... | <b>4</b>    |
| • Removed “Customized Timing and Sequence” section .....                                                                     | <b>12</b>   |
| • Added cross references to timing diagrams.....                                                                             | <b>19</b>   |

| <b>Changes from Revision I (March 2013) to Revision J (August 2014)</b>                                                                                                                                                                                                                                                                                  | <b>Page</b> |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Added <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | <b>4</b>    |

| <b>Changes from Revision H (March 2013) to Revision I (March 2013)</b> | <b>Page</b> |
|------------------------------------------------------------------------|-------------|
| • Changed layout of National Data Sheet to TI format.....              | <b>19</b>   |

## 5 Pin Configuration and Functions



**Figure 5-1. DBV Package 6-Pin SOT-23 Top View**

### Pin Functions

| PIN   |     | I/O <sup>(1)</sup> | DESCRIPTION          |
|-------|-----|--------------------|----------------------|
| NAME  | NO. |                    |                      |
| EN    | 3   | I                  | Precision enable pin |
| FLAG1 | 6   | O                  | Open-drain output 1  |
| FLAG2 | 5   | O                  | Open-drain output 2  |
| FLAG3 | 4   | O                  | Open-drain output 3  |
| GND   | 2   | G                  | Ground               |
| VCC   | 1   | I                  | Input supply         |

(1) I = input, O = output, G = ground

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

|                                      | MIN  | MAX | UNIT |
|--------------------------------------|------|-----|------|
| VCC                                  | −0.3 | 6   | V    |
| EN, FLAG1, FLAG2, FLAG3              | −0.3 | 6   | V    |
| Maximum Flag ON current              |      | 50  | mA   |
| Maximum Junction temperature         |      | 150 | °C   |
| Lead temperature (Soldering, 5 s)    |      | 260 | °C   |
| Storage temperature T <sub>stg</sub> | −65  | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 6.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

### 6.2 ESD Ratings

|                                                                                                                        | VALUE | UNIT |
|------------------------------------------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup> | ±2    | kV   |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                         | MIN  | MAX                   | UNIT |
|-------------------------|------|-----------------------|------|
| VCC to GND              | 2.7  | 5.5                   | V    |
| EN, FLAG1, FLAG2, FLAG3 | −0.3 | V <sub>CC</sub> + 0.3 | V    |
| Junction temperature    | −40  | 125                   | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | LM3880       | UNIT |
|-------------------------------|----------------------------------------------|--------------|------|
|                               |                                              | DBV (SOT-23) |      |
|                               |                                              | 6 PINS       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 187.6        | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 127.4        | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 31.5         | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 23.3         | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 31.0         | °C/W |

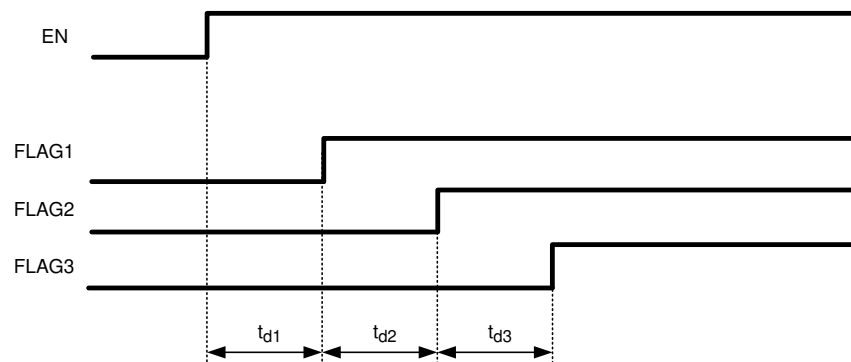
- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Limits apply to all timing options and  $V_{CC} = 3.3\text{ V}$ , unless otherwise specified. Minimum and Maximum limits apply over the full Operating Temperature Range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ) and are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$  and are provided for reference purposes only.

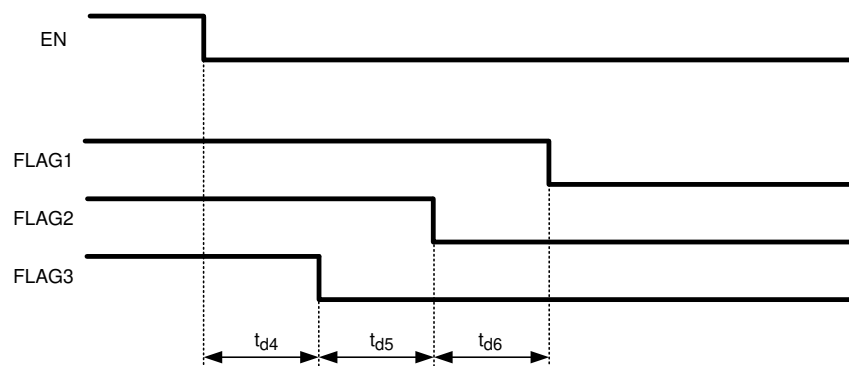
| PARAMETER                                                          | TEST CONDITIONS             | MIN <sup>(1)</sup> | TYP <sup>(2)</sup> | MAX <sup>(1)</sup> | UNIT          |
|--------------------------------------------------------------------|-----------------------------|--------------------|--------------------|--------------------|---------------|
| $I_Q$ Operating Quiescent current                                  |                             |                    | 25                 | 80                 | $\mu\text{A}$ |
| <b>OPEN-DRAIN FLAGS</b>                                            |                             |                    |                    |                    |               |
| $I_{FLAG}$ FLAGx Leakage Current                                   | $V_{FLAGx} = 3.3\text{ V}$  |                    | 1                  | 20                 | nA            |
| $V_{OL}$ FLAGx Output Voltage Low                                  | $I_{FLAGx} = 1.2\text{ mA}$ |                    |                    | 0.4                | V             |
| <b>POWER-UP SEQUENCE</b>                                           |                             |                    |                    |                    |               |
| $t_{d1}$ Timer delay 1 accuracy                                    | All Other Timing Options    | -15%               |                    | 15%                |               |
|                                                                    | 2 ms Timing Option          | -20%               |                    | 20%                |               |
| $t_{d2}$ Timer delay 2 accuracy                                    | All Other Timing Options    | -15%               |                    | 15%                |               |
|                                                                    | 2 ms Timing Option          | -20%               |                    | 20%                |               |
| $t_{d3}$ Timer delay 3 accuracy                                    | All Other Timing Options    | -15%               |                    | 15%                |               |
|                                                                    | 2 ms Timing Option          | -20%               |                    | 20%                |               |
| <b>POWER-DOWN SEQUENCE</b>                                         |                             |                    |                    |                    |               |
| $t_{d4}$ Timer delay 4 accuracy                                    | All Other Timing Options    | -15%               |                    | 15%                |               |
|                                                                    | 2 ms Timing Option          | -20%               |                    | 20%                |               |
| $t_{d5}$ Timer delay 5 accuracy                                    | All Other Timing Options    | -15%               |                    | 15%                |               |
|                                                                    | 2 ms Timing Option          | -20%               |                    | 20%                |               |
| $t_{d6}$ Timer delay 6 accuracy                                    | All Other Timing Options    | -15%               |                    | 15%                |               |
|                                                                    | 2 ms Timing Option          | -20%               |                    | 20%                |               |
| <b>TIMING DELAY ERROR</b>                                          |                             |                    |                    |                    |               |
| $(t_{d(x)} - 400 \mu\text{s}) / t_{d(x+1)}$ Ratio of timing delays | For x = 1 or 4              | 95%                |                    | 105%               |               |
|                                                                    | For x = 1 or 4, 2 ms option | 90%                |                    | 110%               |               |
| $t_{d(x)} / t_{d(x+1)}$ Ratio of timing delays                     | For x = 2 or 5              | 95%                |                    | 105%               |               |
|                                                                    | For x = 2 or 5, 2 ms option | 90%                |                    | 110%               |               |
| <b>ENABLE PIN</b>                                                  |                             |                    |                    |                    |               |
| $V_{EN}$ EN pin threshold                                          |                             | 1.0                | 1.25               | 1.4                | V             |
| $I_{EN}$ EN pin pullup current                                     | $V_{EN} = 0\text{ V}$       |                    | 7                  |                    | $\mu\text{A}$ |

- (1) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate the TI average outgoing quality level (AOQL).
- (2) Typical numbers are at  $25^\circ\text{C}$  and represent the most likely parametric norm.



All standard options use Sequence 1 for output flags rise and fall order. Refer to section 11.1.2 for details of other possible sequences.

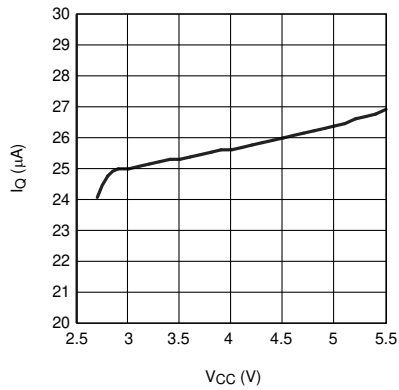
**Figure 6-1. Timing Requirements**



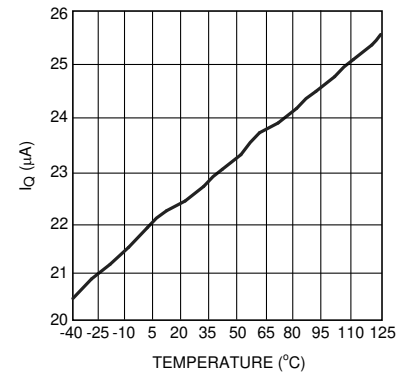
All standard options use Sequence 1 for output flags rise and fall order. Refer to section 11.1.2 for details of other possible sequences.

**Figure 6-2. Power-Down Sequence**

## 6.6 Typical Characteristics

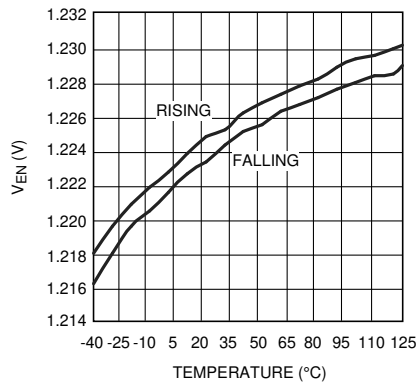


**Figure 6-3. Quiescent Current vs Supply Voltage**

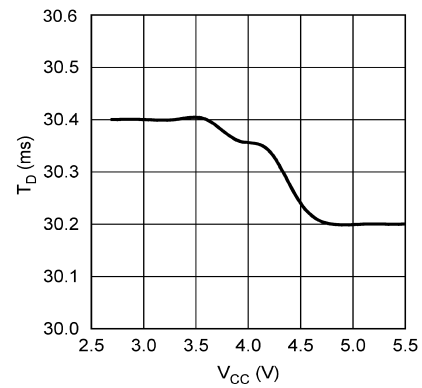


$V_{CC} = 3.3\text{ V}$

**Figure 6-4. Quiescent Current vs Temperature**

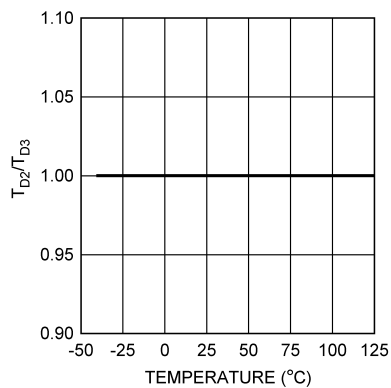


**Figure 6-5. Enable Threshold vs Temperature**

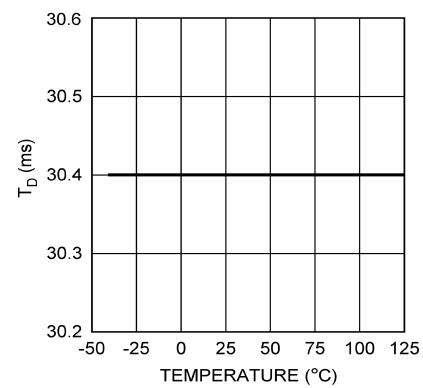


$t_{\text{DELAY}} = 30\text{ ms}$

**Figure 6-6. Time Delay vs Supply Voltage**



**Figure 6-7. Time Delay Ratio vs Temperature**

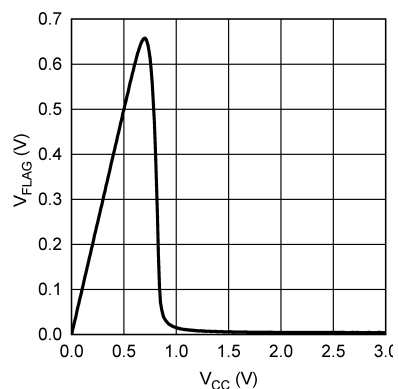


$t_{\text{DELAY}} = 30\text{ ms}$

**Figure 6-8. Time Delay vs Temperature**

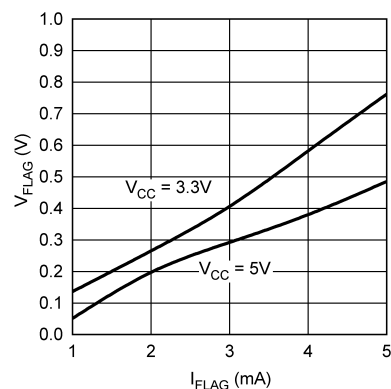
**LM3880**

SNVS451M – AUGUST 2006 – REVISED MARCH 2021



R<sub>FLAG</sub> = 100 kΩ

**Figure 6-9. Flag Voltage vs Supply Voltage**



**Figure 6-10. Flag Voltage vs Input Current**



## 7 Detailed Description

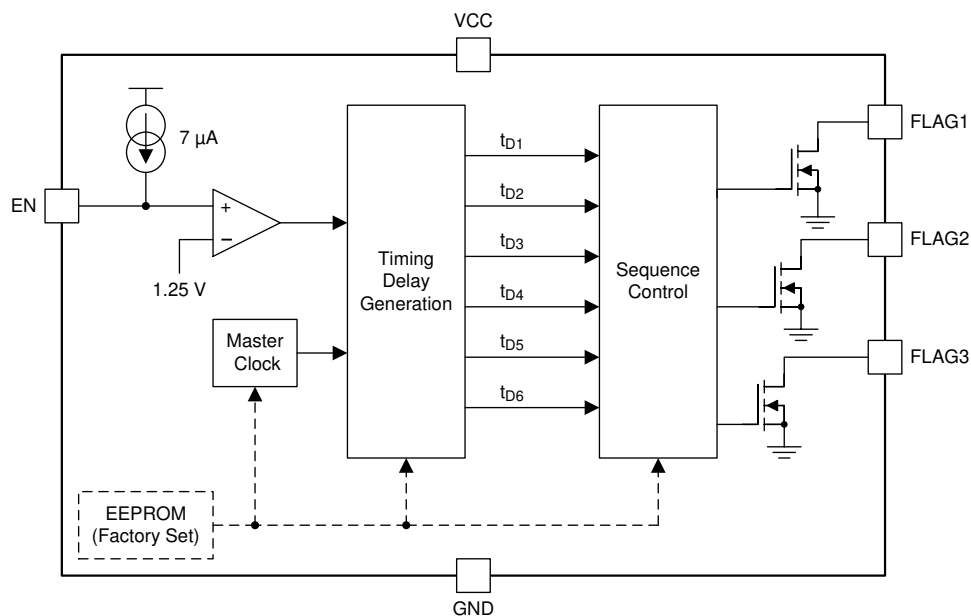
### 7.1 Overview

The LM3880 simple power supply sequencer provides a simple solution for sequencing multiple rails in a controlled manner. Six independent timers are integrated to control the timing sequence (power up and power down) of three open-drain output flags. These flags permit connection to either a shutdown or enable pin of linear regulators and switchers to control the operation of the power supplies. This allows design of a complete power system without concern for large inrush currents or latch-up conditions that can occur.

The timing sequence of the device is controlled entirely by the enable (EN) pin. Upon power up, all the flags are held low until this precision enable is pulled high. When the EN pin is asserted, the power-up sequence starts. An internal counter delays the first flag (FLAG1) from rising until a fixed time period has expired. When the first flag is released, another timer will begin to delay the release of the second flag (FLAG2). This process repeats until all three flags have sequentially been released.

The power-down sequence is the same as power-up sequence, but in reverse. When the EN pin is deasserted a timer will begin that delays the third flag (FLAG3) from pulling low. The second and first flag will then follow in a sequential manner after their appropriate delays. The three timers that are used to control the power-down scheme can also be individually programmed and are completely independent of the power-up timers.

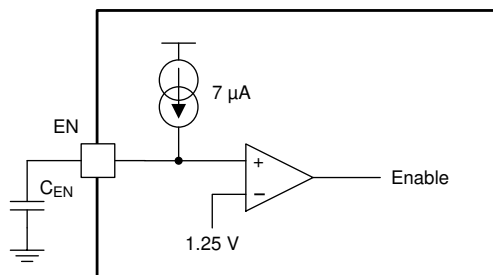
### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Enable Pin Operation

The timing sequence of the LM3880 is controlled by the assertion of the enable signal. The enable pin is designed with an internal comparator, referenced to a bandgap voltage (1.25 V), to provide a precision threshold. This allows a delayed timing to be externally set using a capacitor or to start the sequencing based on a certain event, such as a line voltage reaching 90% of nominal. For an additional delayed sequence from the rail powering VCC, simply attach a capacitor to the EN pin as shown in [Figure 7-1](#).



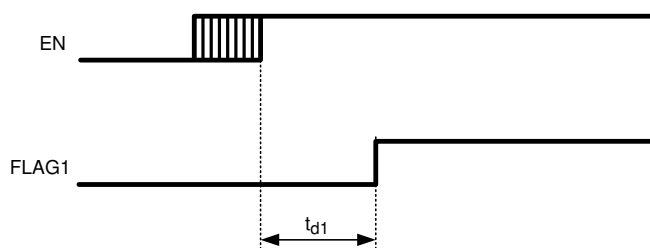
**Figure 7-1. Capacitor Timing**

Using the internal pullup current source to charge the external capacitor ( $C_{EN}$ ) the enable pin delay can be calculated by [Equation 1](#):

$$t_{enable\_delay} = \frac{1.25V \times C_{EN}}{7 \mu A} \quad (1)$$

A resistor divider can also be used to enable the device based on a certain voltage threshold. Take care when sizing the resistor divider to include the effects of the internal current source.

One of the features of the EN pin is that it provides glitch free operation. The first timer will start counting at a rising threshold, but will always reset if the EN pin is deasserted before the first output flag is released. This can be shown in [Figure 7-2](#):

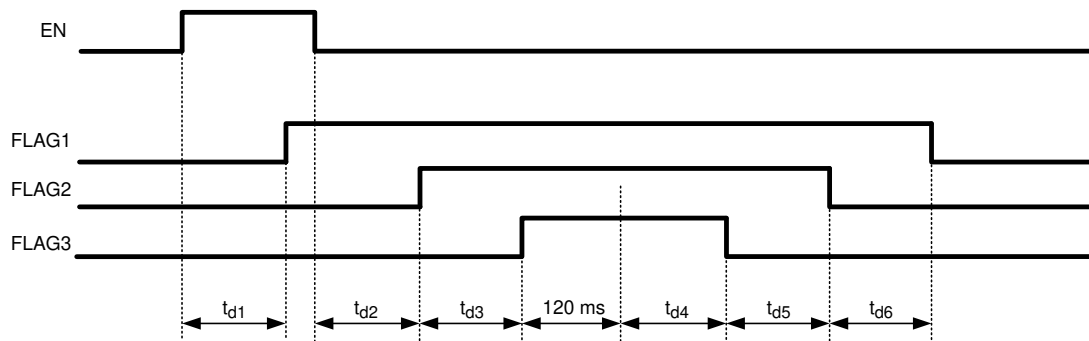


**Figure 7-2. EN Glitch**

### 7.3.2 Incomplete Sequence Operation

If the enable signal remains high for the entire power-up sequence, then the part will operate as shown in the standard timing diagrams. However, if the enable signal is de-asserted before the power-up sequence is completed the part will enter a controlled shutdown. This allows the system to walk through a controlled power cycling, preventing any latch conditions from occurring. This state only occurs if the enable pin is deasserted after the completion of timer 1, but before the entire power-up sequence is completed.

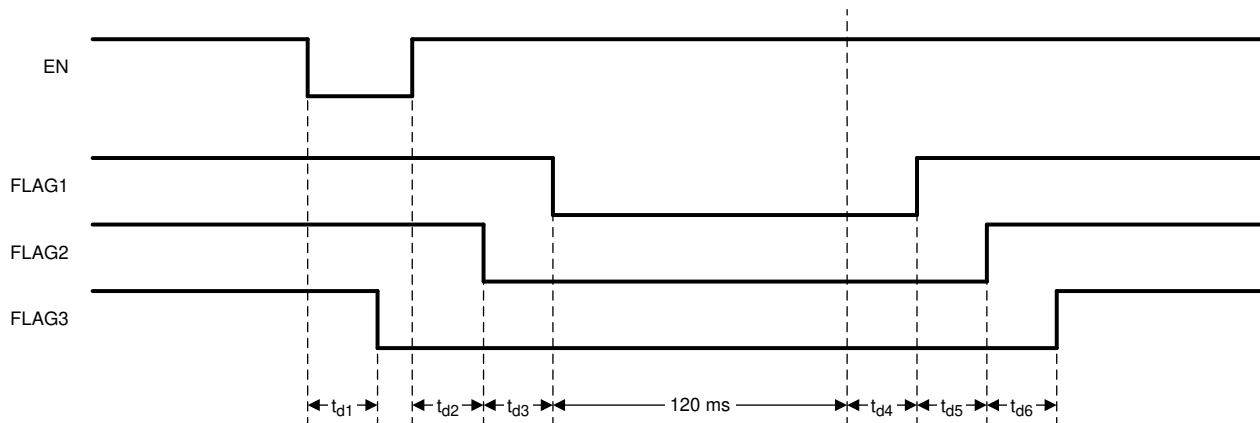
When this event occurs, the falling edge of EN pin resets the current timer and will allow the remaining power-up cycle to complete before beginning the power-down sequence. The power down sequence starts approximately 120 ms after the final power-up flag. This allows output voltages in the system to stabilize before everything is shut down. [Figure 7-3](#) shows this operation.



**Figure 7-3. Incomplete Power-Up Sequence**

When the enable signal is deasserted, the part will commence its power-down sequence. If the enable signal is pulled high before the power-down sequence is completed, the part will ensure completion of the power-down sequence before starting power-up. This ensures that the system does not partially power down and power up and helps prevent latch-up events, such as in FPGAs and microprocessors. This state only occurs if the enable pin is pulled high after the completion of timer 1, but before the entire power-down sequence is completed.

When this event occurs, the rising edge of enable pin resets the current timer and will allow the remaining power-down cycle to complete before beginning the power-up sequence. The power-up sequence starts approximately 120 ms after the final power-down flag. This allows the system to fully shut down before it is powered up. [Figure 7-4](#) shows this operation.



**Figure 7-4. Incomplete Power-Down Sequence**

All the internal timers are generated by a master clock that has an extremely low tempco. This allows for tight accuracy across temperature and a consistent ratio between the individual timers. There is a slight additional delay of approximately 400  $\mu$ s to timers 1 and 4, which is a result of the EPROM refresh. This refresh time is in addition to the programmed delay time and will be almost insignificant to all but the shortest of timer delays.

## 7.4 Device Functional Modes

### 7.4.1 Power Up With EN Pin

The timing sequence of the Simple Power Supply Sequencer is controlled entirely by the enable (EN) pin. Upon power up, all the flags are held low until this precision enable is pulled high. After the EN pin is asserted, the power-up sequence will commence.

### 7.4.2 Power Down With EN Pin

When EN pin is deasserted, the power down sequence will commence. A timer will begin that delays the third flag (FLAG3) from pulling low. The second and first flag will then follow in a sequential manner after their appropriate delays.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Open Drain Flags Pullup

The Simple Power Supply Sequencer contains three open-drain output flags which need to be pulled up for proper operation. 100-k $\Omega$  resistors can be used as pullup resistors.

#### 8.1.2 Enable the Device

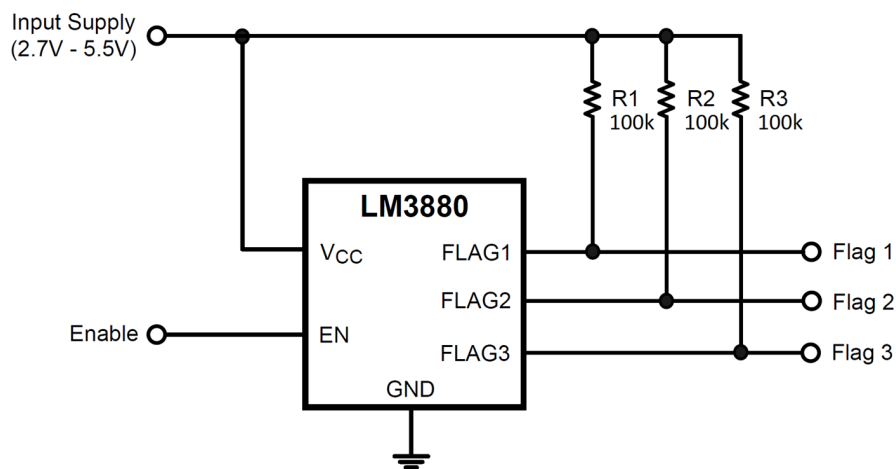
See [Section 7.3.1](#).

### 8.2 Typical Application

#### 8.2.1 Simple Sequencing of Three Power Supplies

The Simple Power Supply Sequencer is used to implement a power-up and power-down sequence of three power supplies.

Sequence 1 for the LM3880, e.g. orderable part number LM3880MF-1AA has a power-up sequence (1 – 2 – 3) and power-down sequence (3 – 2 – 1). See [Table 10-1](#) and [Table 10-2](#) for other sequence options or contact TI if other sequence options are desired.



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**Figure 8-1. Typical Application Circuit**

### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 8-1](#) as the input parameters. The circuit shown in [Figure 8-1](#) can have various power-down sequences depending on the sequence the part is programmed for. See [Table 10-1](#) for power-down sequence options.

**Table 8-1. Design Parameters**

| DESIGN PARAMETER             | EXAMPLE VALUE  |
|------------------------------|----------------|
| Input Supply voltage range   | 2.7 V to 5.5 V |
| Flag Output voltage, EN high | Input Supply   |
| Flag Output voltage, EN low  | 0 V            |
| Flag Timing Delay            | 30 ms          |
| Power-Up Sequence            | 1 - 2 - 3      |
| Power-Down Sequence          | 3 - 2 - 1      |

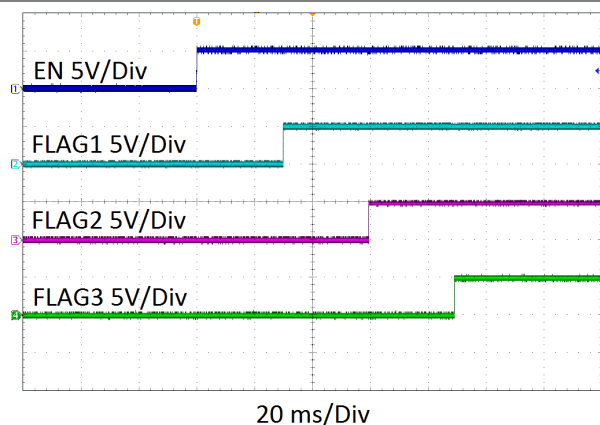
### 8.2.1.2 Detailed Design Procedure

**Table 8-2. List of Materials**

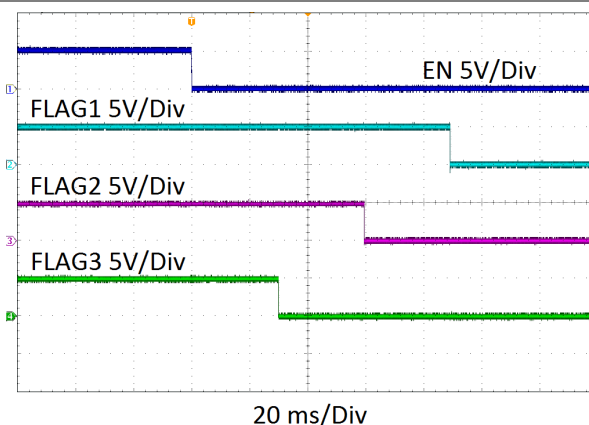
| DESIGNATOR | DESCRIPTION                      | DEVICE           | QUANTITY | MANUFACTURER      |
|------------|----------------------------------|------------------|----------|-------------------|
| U1         | LM3880, Sequence 1, 30 ms timing | LM3880           | 1        | Texas Instruments |
| R1         | 100-k $\Omega$ Resistor, 0603    | CRCW0603100KFKEA | 1        | Vishay            |
| R2         | 100-k $\Omega$ Resistor, 0603    | CRCW0603100KFKEA | 1        | Vishay            |
| R3         | 100-k $\Omega$ Resistor, 0603    | CRCW0603100KFKEA | 1        | Vishay            |

This application uses the Sequence 1 and 30-ms timing options of the simple power supply sequencer. See [Section 8.2.1.3](#) for details on the sequence and timing option.

### 8.2.1.3 Application Curves



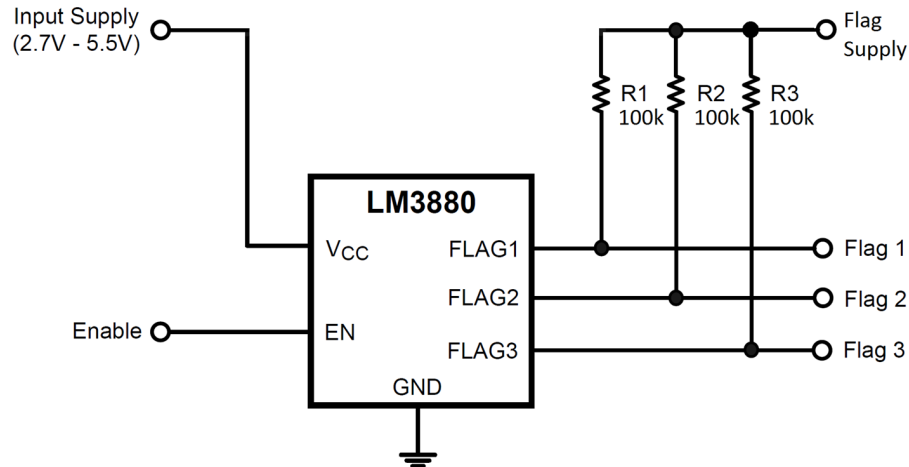
**Figure 8-2. Powerup Sequence for LM3880MF-1AB**



**Figure 8-3. Powerdown Sequence for LM3880MF-1AB**

## 8.2.2 Sequencing Using Independent Flag Supply

For applications requiring a flag output voltage that is different from the VCC, a separate Flag Supply may be used to pullup the open-drain outputs of the simple power supply sequencer. This is useful when interfacing the flag outputs with inputs that require a different voltage than VCC. The designer must ensure the flag supply voltage is not taken above  $VCC + 0.3\text{ V}$  as specified in the [Section 6.3](#).

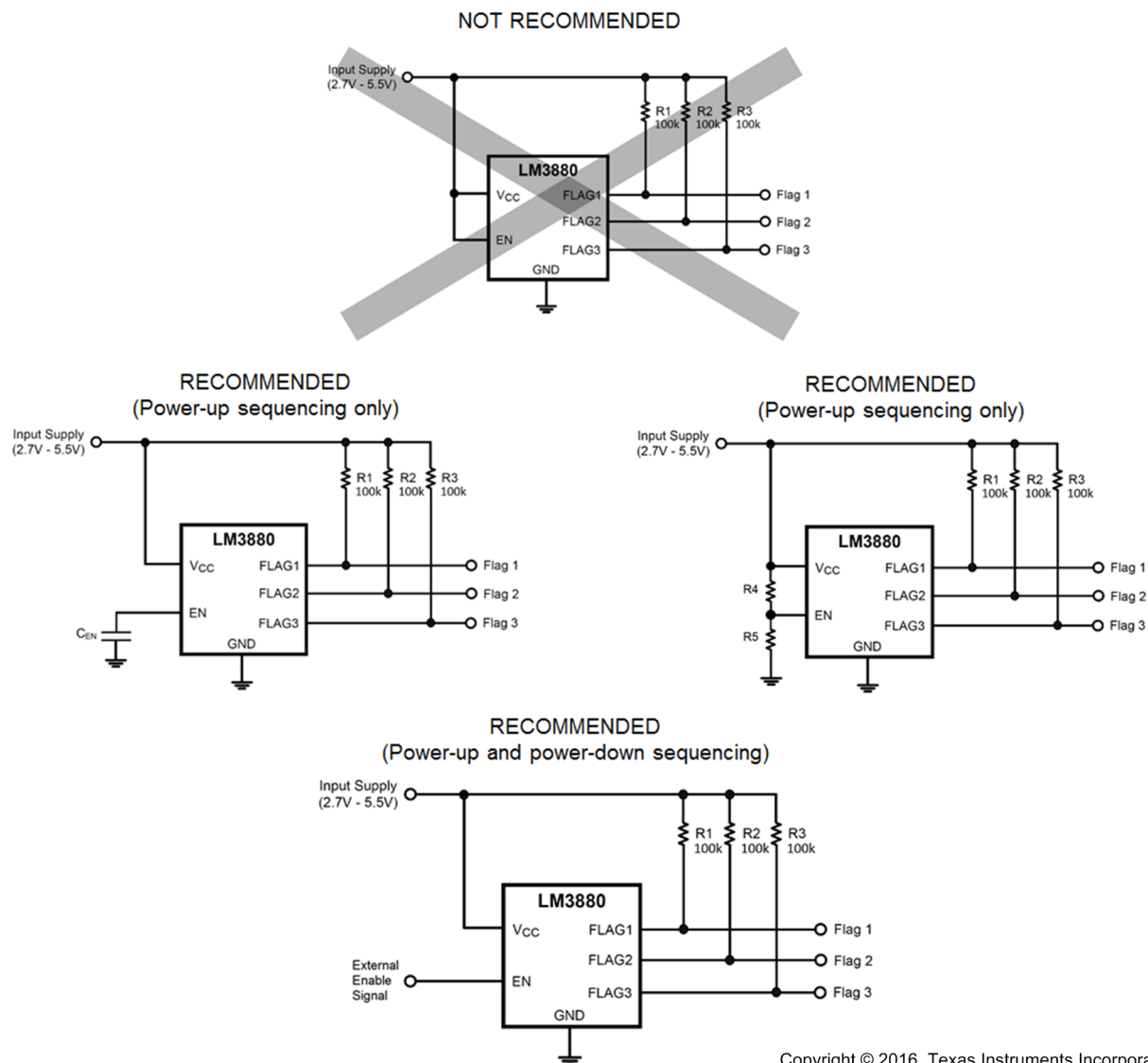


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**Figure 8-4. Sequencing Using Independent Flag Supply**

## 8.3 Dos and Don'ts

Connecting the EN pin to VCC is not recommended. During powerup sequencing, maintain the EN voltage to a level below the EN voltage threshold until VCC rises above the minimum operating voltage. If EN is connected to VCC, undefined operation at the flag outputs can occur, especially during slow VCC rising slew rates. For systems requiring only powerup sequencing, a capacitor at the EN pin can be used to create a delay or a resistor divider can be used to enable the device based on a certain voltage threshold. While these solutions work for powerup sequencing, it does not powerdown the flag outputs in sequential fashion because the flag outputs simply follow the input supply. For systems requiring both powerup and powerdown sequencing, use an external enable signal, such as a GPIO signal from a microcontroller, to properly control powerup and powerdown of the flag outputs.



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**Figure 8-5. Recommended EN Connection**



## Power Supply Recommendations

The VCC pin should be located as close as possible to the input supply (2.7–5.5 V). An input capacitor is not required but is recommended when noise might be present on the VCC pin. A 0.1- $\mu$ F ceramic capacitor may be used to bypass this noise.

## 9 Layout

### 9.1 Layout Guidelines

- Pullup resistors should be connected between the flag output pins and a positive input supply, usually VCC. An independent flag supply may also be used. These resistors should be placed as close as possible to the Simple Power Supply Sequencer and the flag supply. Minimal trace length is recommended to make the connections. A typical value for the pullup resistors is 100 k $\Omega$ .
- For very tight sequencing requirements, minimal and equal trace lengths should be used to connect the flag outputs to the desired inputs. This will reduce any propagation delay and timing errors between the flag outputs along the line.

### 9.2 Layout Example

Figure 9-1 and Figure 9-2 are layout examples for the LM3880. These examples are taken from the LM3880EVAL.

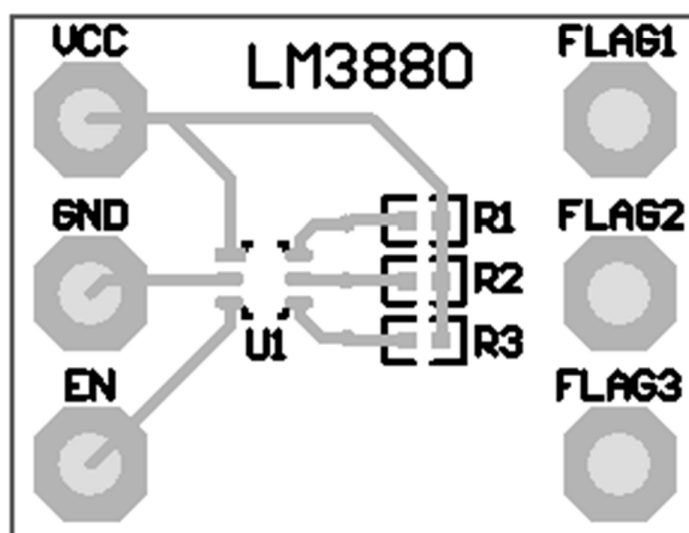


Figure 9-1. LM3880 Top

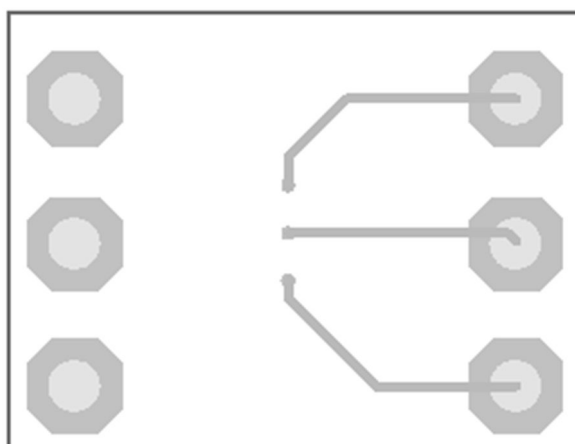


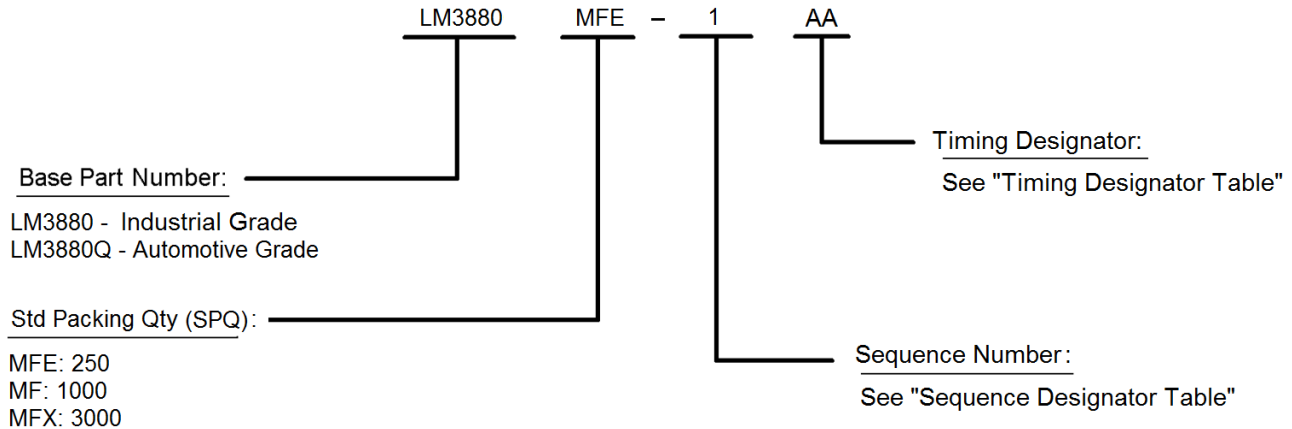
Figure 9-2. LM3880 Bottom

## 10 Device and Documentation Support

### 10.1 Device Support

#### 10.1.1 Device Nomenclature

The list of parts available to order appear in the Package Option Addendum.



**Figure 10-1. Device Nomenclature**

**Table 10-1. Sequence Designator Table <sup>(1)</sup>**

| SEQUENCE NUMBER | FLAG ORDER |            |
|-----------------|------------|------------|
|                 | POWER UP   | POWER DOWN |
| 1               | 1 - 2 - 3  | 3 - 2 - 1  |
| 2               | 1 - 2 - 3  | 3 - 1 - 2  |
| 3               | 1 - 2 - 3  | 2 - 3 - 1  |
| 4               | 1 - 2 - 3  | 2 - 1 - 3  |
| 5               | 1 - 2 - 3  | 1 - 3 - 2  |
| 6               | 1 - 2 - 3  | 1 - 2 - 3  |

(1) See and [Figure 6-2](#).

**Table 10-2. Timing Designator Table <sup>(1)</sup>**

| TIMING DESIGNATOR | DELAYS (ms)     |                 |                 |                 |                 |                 |
|-------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
|                   | t <sub>d1</sub> | t <sub>d2</sub> | t <sub>d3</sub> | t <sub>d4</sub> | t <sub>d5</sub> | t <sub>d6</sub> |
| AA                | 10              | 10              | 10              | 10              | 10              | 10              |
| AB                | 30              | 30              | 30              | 30              | 30              | 30              |
| AC                | 60              | 60              | 60              | 60              | 60              | 60              |
| AD                | 120             | 120             | 120             | 120             | 120             | 120             |
| AE                | 2               | 2               | 2               | 2               | 2               | 2               |
| AF                | 16              | 16              | 16              | 16              | 16              | 16              |

(1) See and [Figure 6-2](#).

### 10.2 Community Resources

### 10.3 Trademarks

All trademarks are the property of their respective owners.

## Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LM3880MF-1AA/NOPB</a>  | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F20A                |
| LM3880MF-1AA/NOPB.A                | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F20A                |
| <a href="#">LM3880MF-1AB/NOPB</a>  | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F21A                |
| LM3880MF-1AB/NOPB.A                | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F21A                |
| <a href="#">LM3880MF-1AC/NOPB</a>  | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F22A                |
| LM3880MF-1AC/NOPB.A                | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F22A                |
| <a href="#">LM3880MF-1AD/NOPB</a>  | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F23A                |
| LM3880MF-1AD/NOPB.A                | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F23A                |
| <a href="#">LM3880MF-1AE/NOPB</a>  | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F25A                |
| LM3880MF-1AE/NOPB.A                | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F25A                |
| <a href="#">LM3880MF-1AF/NOPB</a>  | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F31A                |
| LM3880MF-1AF/NOPB.A                | Active        | Production           | SOT-23 (DBV)   6 | 1000   SMALL T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F31A                |
| <a href="#">LM3880MFE-1AA/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F20A                |
| LM3880MFE-1AA/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F20A                |
| <a href="#">LM3880MFE-1AB/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F21A                |
| LM3880MFE-1AB/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F21A                |
| <a href="#">LM3880MFE-1AC/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F22A                |
| LM3880MFE-1AC/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F22A                |
| <a href="#">LM3880MFE-1AD/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F23A                |
| LM3880MFE-1AD/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F23A                |
| <a href="#">LM3880MFE-1AE/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F25A                |
| LM3880MFE-1AE/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F25A                |
| <a href="#">LM3880MFE-1AF/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F31A                |
| LM3880MFE-1AF/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F31A                |
| <a href="#">LM3880MFX-1AA/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F20A                |
| LM3880MFX-1AA/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F20A                |
| <a href="#">LM3880MFX-1AB/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F21A                |
| LM3880MFX-1AB/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F21A                |
| <a href="#">LM3880MFX-1AC/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F22A                |

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| LM3880MFX-1AC/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F22A                |
| <a href="#">LM3880MFX-1AD/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F23A                |
| LM3880MFX-1AD/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F23A                |
| <a href="#">LM3880MFX-1AE/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F25A                |
| LM3880MFX-1AE/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F25A                |
| <a href="#">LM3880MFX-1AF/NOPB</a> | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F31A                |
| LM3880MFX-1AF/NOPB.A               | Active        | Production           | SOT-23 (DBV)   6 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | F31A                |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF LM3880 :**

- Automotive : [LM3880-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM3880MF-1AA/NOPB  | SOT-23       | DBV             | 6    | 1000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MF-1AB/NOPB  | SOT-23       | DBV             | 6    | 1000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MF-1AC/NOPB  | SOT-23       | DBV             | 6    | 1000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MF-1AD/NOPB  | SOT-23       | DBV             | 6    | 1000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MF-1AE/NOPB  | SOT-23       | DBV             | 6    | 1000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MF-1AF/NOPB  | SOT-23       | DBV             | 6    | 1000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFE-1AA/NOPB | SOT-23       | DBV             | 6    | 250  | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFE-1AB/NOPB | SOT-23       | DBV             | 6    | 250  | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFE-1AC/NOPB | SOT-23       | DBV             | 6    | 250  | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFE-1AD/NOPB | SOT-23       | DBV             | 6    | 250  | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFE-1AE/NOPB | SOT-23       | DBV             | 6    | 250  | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFE-1AF/NOPB | SOT-23       | DBV             | 6    | 250  | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFX-1AA/NOPB | SOT-23       | DBV             | 6    | 3000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFX-1AB/NOPB | SOT-23       | DBV             | 6    | 3000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFX-1AC/NOPB | SOT-23       | DBV             | 6    | 3000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFX-1AD/NOPB | SOT-23       | DBV             | 6    | 3000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |



---

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM3880MFX-1AE/NOPB | SOT-23       | DBV             | 6    | 3000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| LM3880MFX-1AF/NOPB | SOT-23       | DBV             | 6    | 3000 | 178.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |

## TAPE AND REEL BOX DIMENSIONS

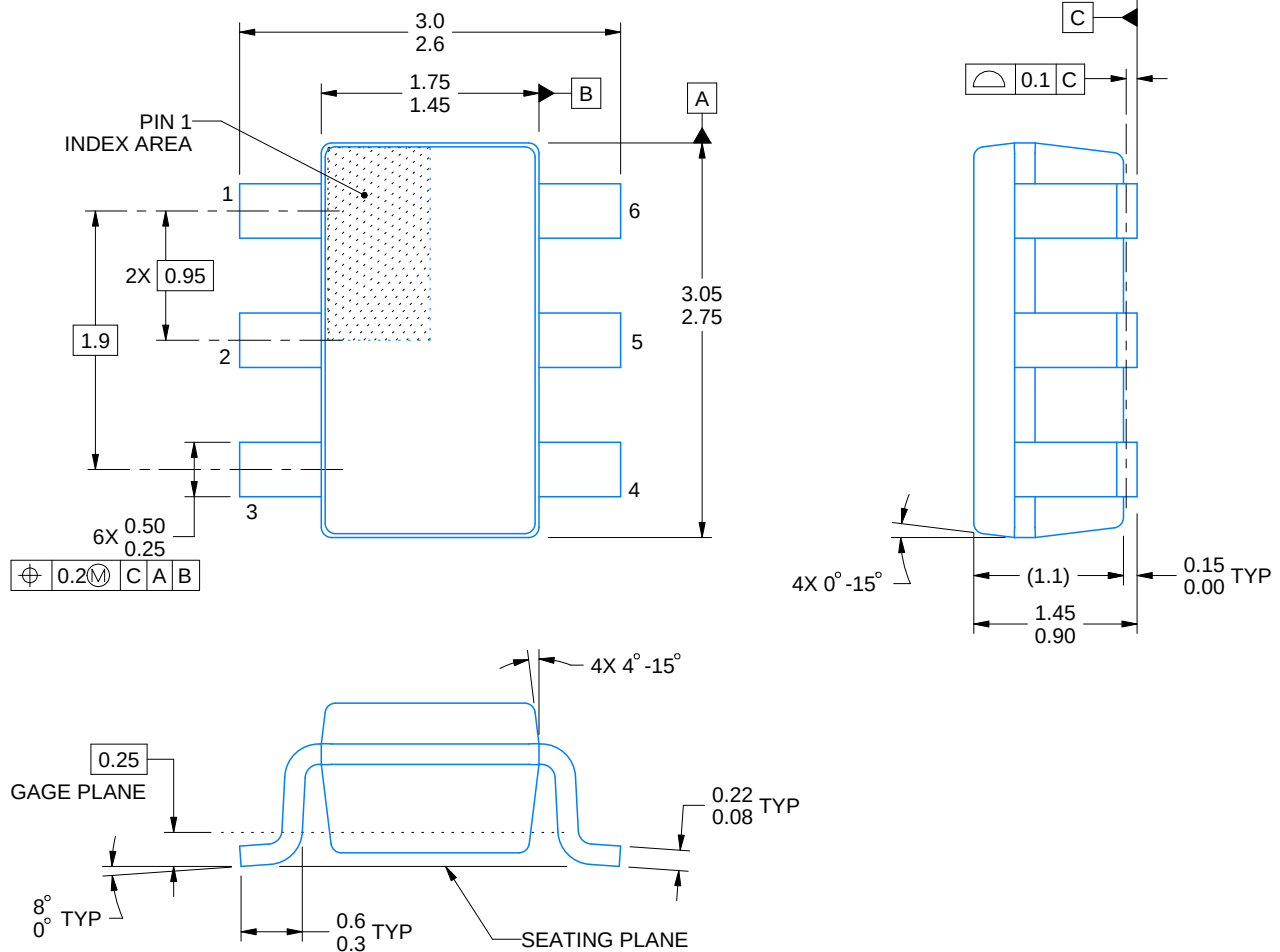


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM3880MF-1AA/NOPB  | SOT-23       | DBV             | 6    | 1000 | 208.0       | 191.0      | 35.0        |
| LM3880MF-1AB/NOPB  | SOT-23       | DBV             | 6    | 1000 | 208.0       | 191.0      | 35.0        |
| LM3880MF-1AC/NOPB  | SOT-23       | DBV             | 6    | 1000 | 208.0       | 191.0      | 35.0        |
| LM3880MF-1AD/NOPB  | SOT-23       | DBV             | 6    | 1000 | 208.0       | 191.0      | 35.0        |
| LM3880MF-1AE/NOPB  | SOT-23       | DBV             | 6    | 1000 | 208.0       | 191.0      | 35.0        |
| LM3880MF-1AF/NOPB  | SOT-23       | DBV             | 6    | 1000 | 208.0       | 191.0      | 35.0        |
| LM3880MFE-1AA/NOPB | SOT-23       | DBV             | 6    | 250  | 208.0       | 191.0      | 35.0        |
| LM3880MFE-1AB/NOPB | SOT-23       | DBV             | 6    | 250  | 208.0       | 191.0      | 35.0        |
| LM3880MFE-1AC/NOPB | SOT-23       | DBV             | 6    | 250  | 208.0       | 191.0      | 35.0        |
| LM3880MFE-1AD/NOPB | SOT-23       | DBV             | 6    | 250  | 208.0       | 191.0      | 35.0        |
| LM3880MFE-1AE/NOPB | SOT-23       | DBV             | 6    | 250  | 208.0       | 191.0      | 35.0        |
| LM3880MFE-1AF/NOPB | SOT-23       | DBV             | 6    | 250  | 208.0       | 191.0      | 35.0        |
| LM3880MFX-1AA/NOPB | SOT-23       | DBV             | 6    | 3000 | 208.0       | 191.0      | 35.0        |
| LM3880MFX-1AB/NOPB | SOT-23       | DBV             | 6    | 3000 | 208.0       | 191.0      | 35.0        |
| LM3880MFX-1AC/NOPB | SOT-23       | DBV             | 6    | 3000 | 208.0       | 191.0      | 35.0        |
| LM3880MFX-1AD/NOPB | SOT-23       | DBV             | 6    | 3000 | 208.0       | 191.0      | 35.0        |
| LM3880MFX-1AE/NOPB | SOT-23       | DBV             | 6    | 3000 | 208.0       | 191.0      | 35.0        |
| LM3880MFX-1AF/NOPB | SOT-23       | DBV             | 6    | 3000 | 208.0       | 191.0      | 35.0        |

**DBV0006A****PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

**NOTES:**

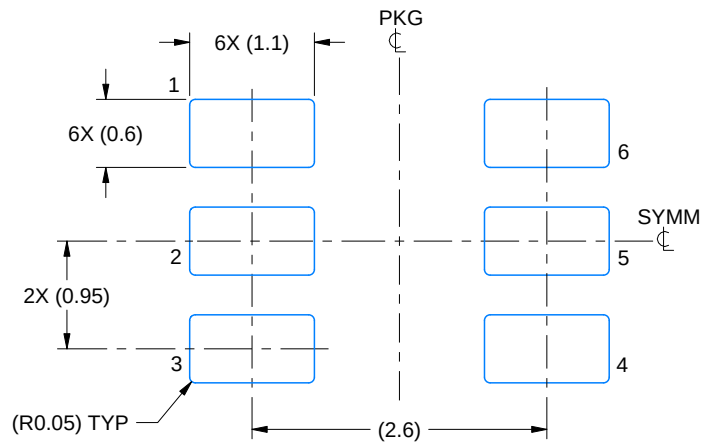
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

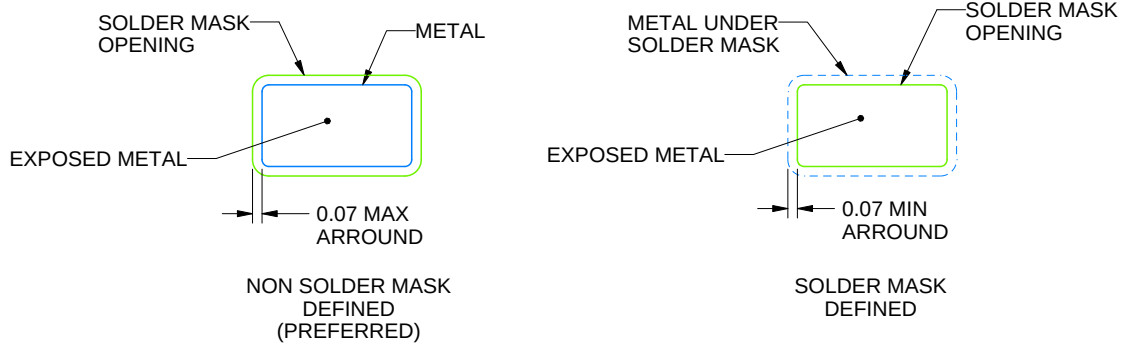
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

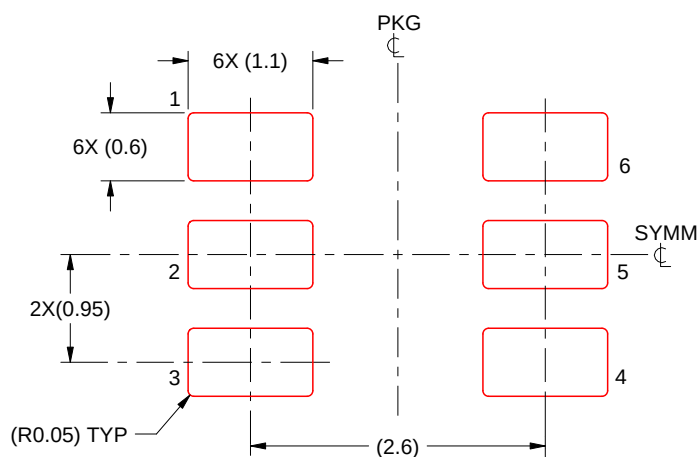
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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