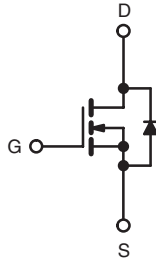
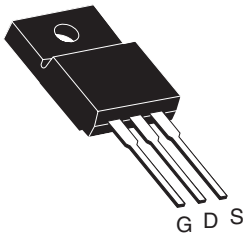


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.67
Q_g (Max.) (nC)	45	
Q_{gs} (nC)	13	
Q_{gd} (nC)	23	
Configuration	Single	

TO-220 FULLPAK

N-Channel MOSFET

FEATURES

- Super Fast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhanced dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Lead (Pb)-free


RoHS
COMPLIANT

APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIB5N50LPbF
	SiHFIB5N50L-E3

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	500	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	4.7	A
		T _C = 100 °C		3.0	
Pulsed Drain Current ^a			I _{DM}	16	
Linear Derating Factor				0.33	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	140	mJ
Avalanche Current ^a			I _{AR}	4.0	A
Repetitive Avalanche Energy ^a			E _{AR}	3.0	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	42	W
Peak Diode Recovery dV/dt ^c			dV/dt	19	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 18\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 4.0\text{ A}$, $dV/dt = 19\text{ V/ns}$, (see fig. 17).
- $I_{SD} \leq 4.0\text{ A}$, $dI/dt \leq 421\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.0	

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.43	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	50	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	2.0	mA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.4 A ^b	-	0.67	0.80	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 2.4 A		2.8	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1000	-	pF
Output Capacitance	C _{oss}			-	110	-	
Reverse Transfer Capacitance	C _{rss}			-	12	-	
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	1360	-	
			V _{DS} = 400 V, f = 1.0 MHz	-	31	-	
Effective Output Capacitance	C _{oss} eff.		V _{DS} = 0 V to 400 V ^c	-	75	-	
Effective Output Capacitance (Energy Related)	C _{oss} eff. (ER)		-	55	-		
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 4.0 A, V _{DS} = 400 V, see fig. 7 and 16 ^b	-	-	45	nC
Gate-Source Charge	Q _{gs}			-	-	13	
Gate-Drain Charge	Q _{gd}			-	-	23	
Internal Gate Resistance	R _G	f = 1 MHz, open drain		-	2.0	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 4.0 A, R _G = 9.0 Ω, V _{GS} = 10 V, see fig. 11a and 11b ^b		-	13	-	ns
Rise Time	t _r			-	17	-	
Turn-Off Delay Time	t _{d(off)}			-	26	-	
Fall Time	t _f			-	10	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	4.7	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	16	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 4.0 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 4.0 A, T _J = 125 °C, dI/dt = 100 A/μs ^b		-	73	110	ns
				-	99	150	
Body Diode Reverse Recovery Charge	Q _{rr}	T _J = 25 °C, I _S = 4.0 A, T _J = 125 °C, dI/dt = 100 A/μs ^b		-	200	310	nC
				-	360	540	
Drain-Source Body Diode Characteristics							
Body Diode Reverse Recovery Current	I _{RRM}	T _J = 25 °C		-	6.7	10	A
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .
 $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

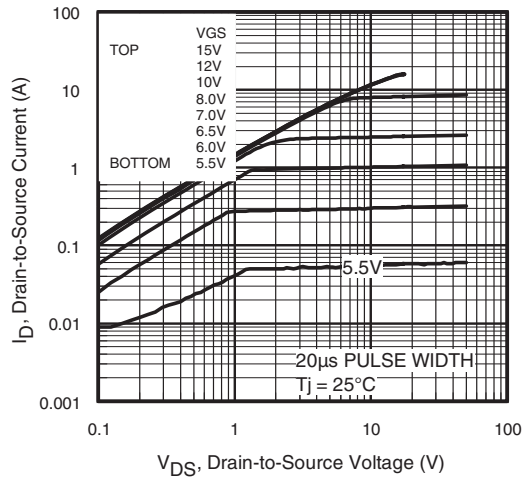


Fig. 1 - Typical Output Characteristics

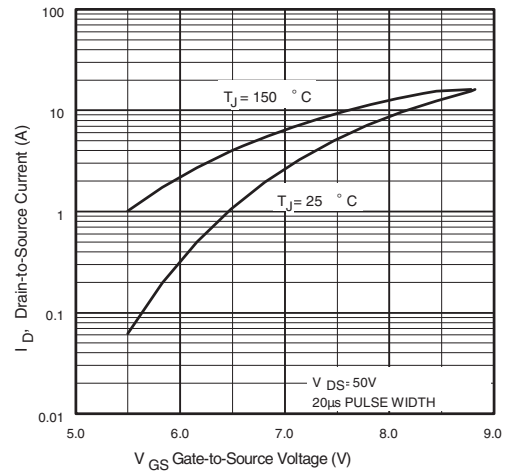


Fig. 3 - Typical Transfer Characteristics

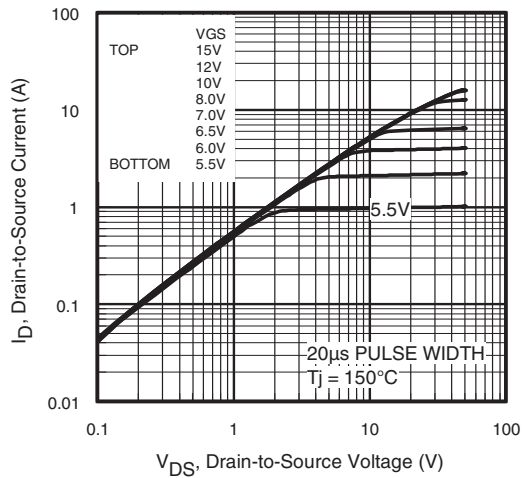


Fig. 2 - Typical Output Characteristics

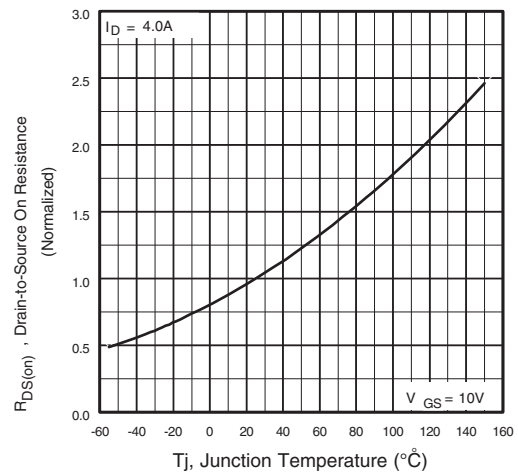


Fig. 4 - Normalized On-Resistance vs. Temperature

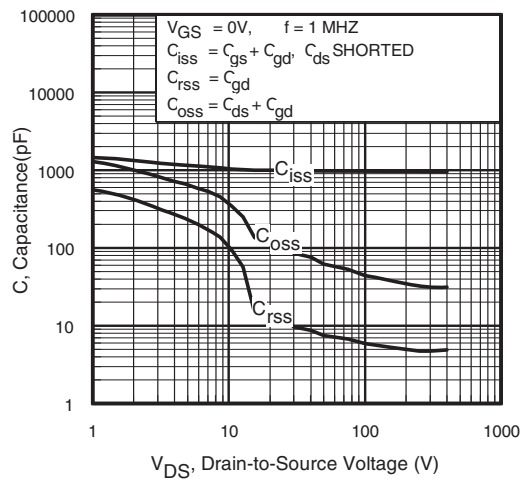


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

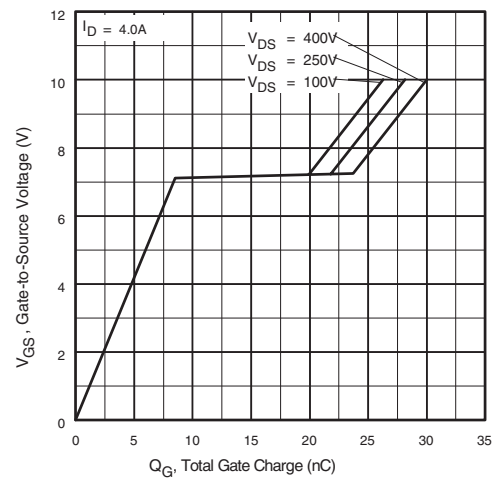


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

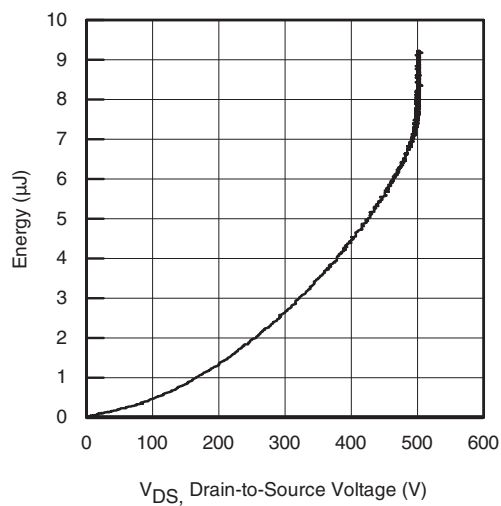


Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

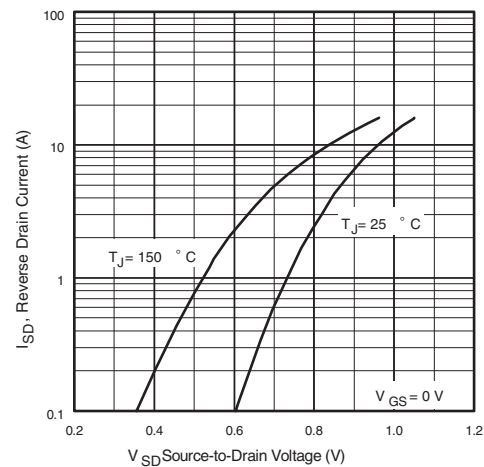


Fig. 8 - Typical Source-Drain Diode Forward Voltage

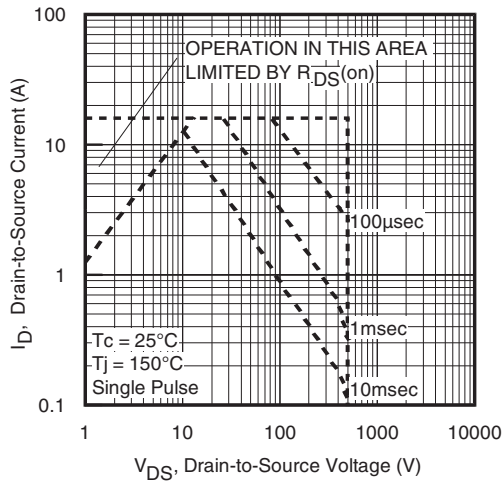


Fig. 9 - Maximum Safe Operating Area

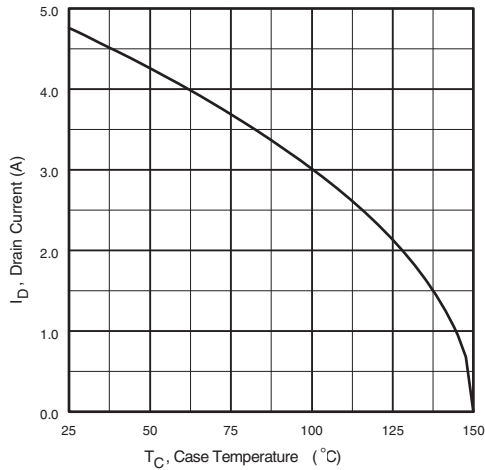


Fig. 10 - Maximum Drain Current vs. Case Temperature

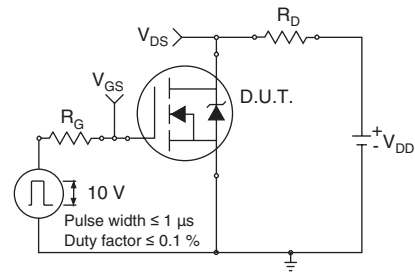


Fig. 11a - Switching Time Test Circuit

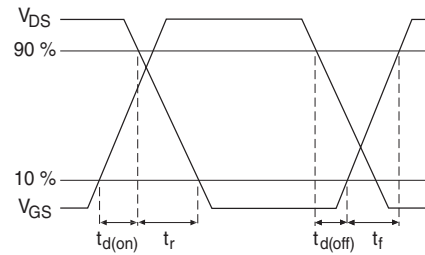


Fig. 11b - Switching Time Waveforms

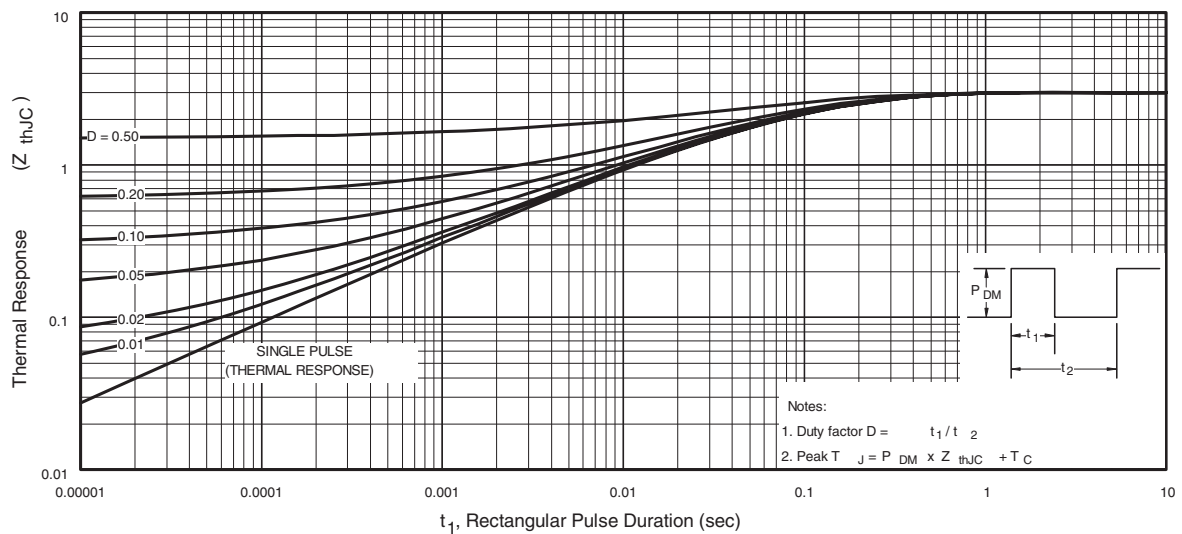


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

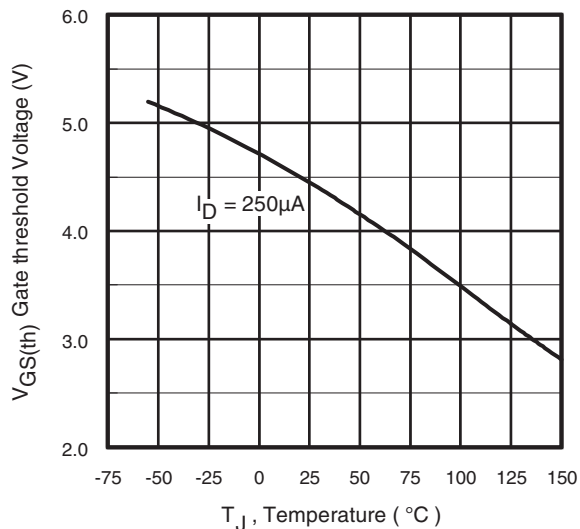


Fig. 13 - Threshold Voltage vs. Temperature

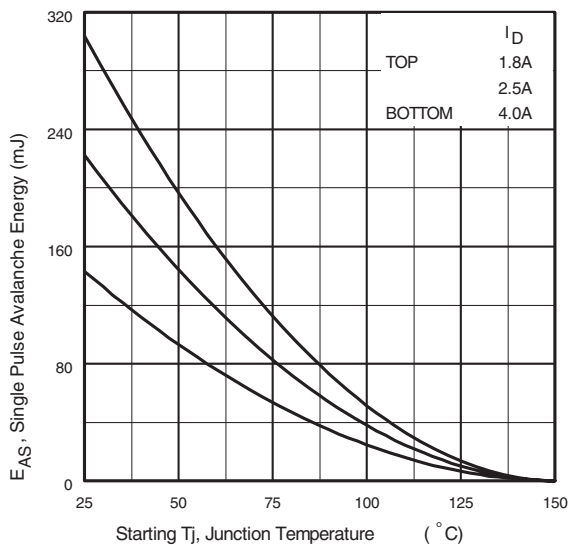


Fig. 14 - Maximum Avalanche Energy vs. Drain Current

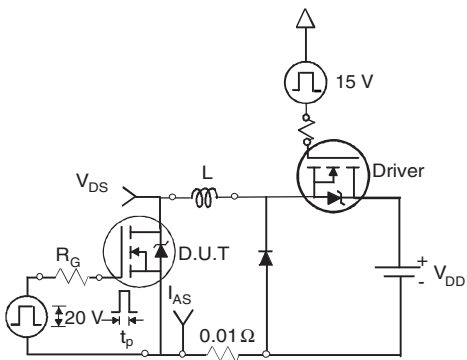


Fig. 15a - Unclamped Inductive Test Circuit

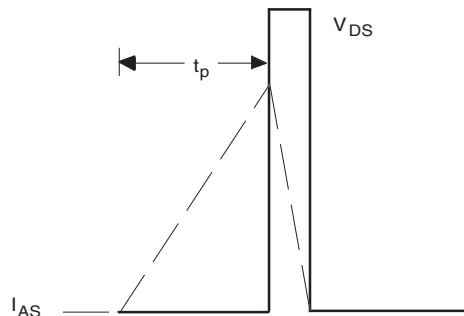


Fig. 15b - Unclamped Inductive Waveforms

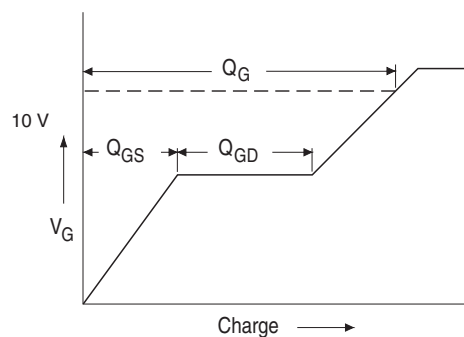


Fig. 16a - Basic Gate Charge Waveform

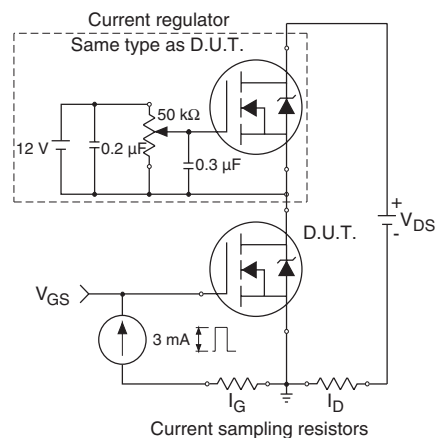


Fig. 16b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

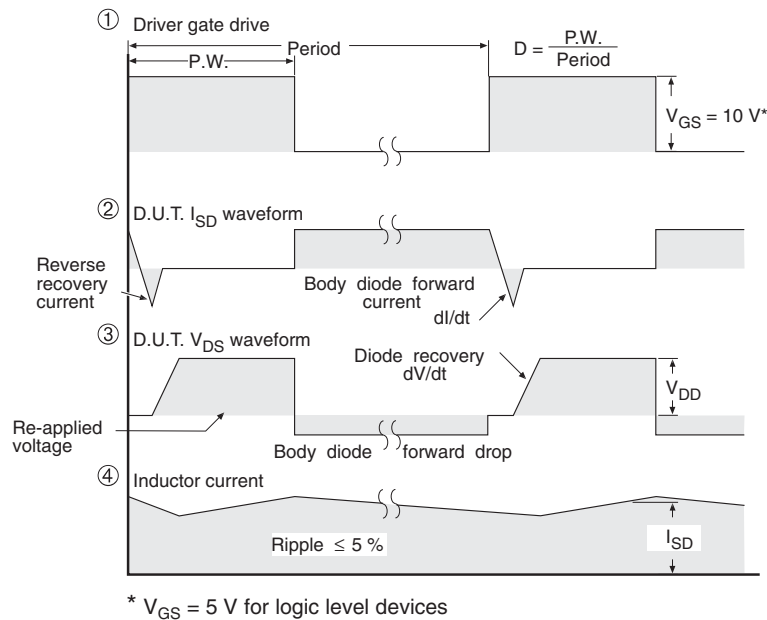
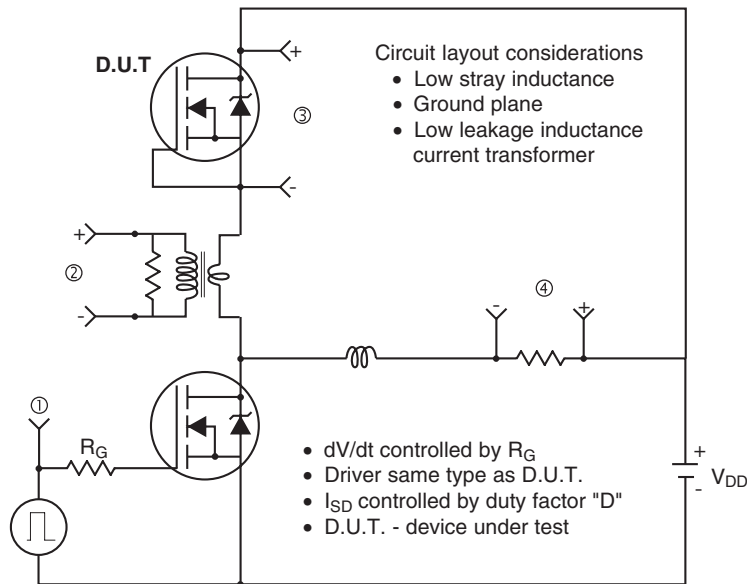


Fig. 17 - For N-Channel

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