ISL32430E, ISL32432E, ISL32433E, ISL32435E, ISL32437E

±40V Fault Protected, 3.3V to 5V, ±15V Common Mode Range, RS-485/RS-422 Transceivers With Cable Invert and ±15kV ESD

FN7920
Rev 0.00
Mar 1, 2012

The ISL32430E through ISL32437E are 3.3V to 5V powered, fault protected, extended common mode range differential transceivers for balanced communication. The RS-485 bus pins (driver outputs and receiver inputs) are protected against overvoltages up to ±40V, and against ±15kV ESD strikes. Additionally, these transceivers operate in environments with common mode voltages up to ±15V (exceeds the RS-485 requirement), making this RS-485 family one of the more robust on the market.

Transmitters are RS-485 compliant with V_{CC} ≥ 4.5V and deliver a 1.1V differential output voltage into the RS-485 specified 54Ω load even with V_{CC} = 3V.

Receiver (Rx) inputs feature a "Full Fail-Safe" design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or on a terminated but undriven (idle) bus. Rx full fail-safe operation is maintained even when the Rx input polarity is switched (cable invert function on ISL32437E).

The ISL32437E includes a cable invert function that reverses the polarity of the Rx and Tx bus pins in case the cable is misconnected during installation.

See Table 1 on page 2 for key features and configurations by device number.

Related Literature

- See FN7921, "ISL32450E, ISL32452E, ISL32453E, ISL32455E, ISL32457E: ±60V Fault Protected, 3.3V to 5V, ±20V Common Mode Range, RS-485/RS-422 Transceivers with Cable Invert and ±15kV ESD"

Features

- Fault Protected RS-485 Bus Pins . . . . . up to ±40V
- Extended Common Mode Range . . . . . ±15V
  Larger Than Required for RS-485
- ±15kV HBM ESD Protection on RS-485 Bus Pins
- Wide Supply Range . . . . . 3V to 5.5V
- Cable Invert Pin (ISL32437E Only)
  Corrects for Reversed Cable Connections While Maintaining Rx Full Fail-safe Functionality
- 1/4 Unit Load for up to 128 Devices on the Bus
- High Transient Overvoltage Tolerance . . . . . ±60V
- Full Fail-safe (Open, Short, Terminated) RS-485 Receivers
- Choice of RS-485 Data Rates . . . . . 250kbps or 1Mbps
- Low Quiescent Supply Current 2.1mA
  Ultra Low Shutdown Supply Current 10µA
- Pb-Free (RoHS Compliant)

Applications

- Utility Meters/Automated Meter Reading Systems
- Air Conditioning Systems
- Security Camera Networks
- Building Lighting and Environmental Control Systems
- Industrial/Process Control Networks

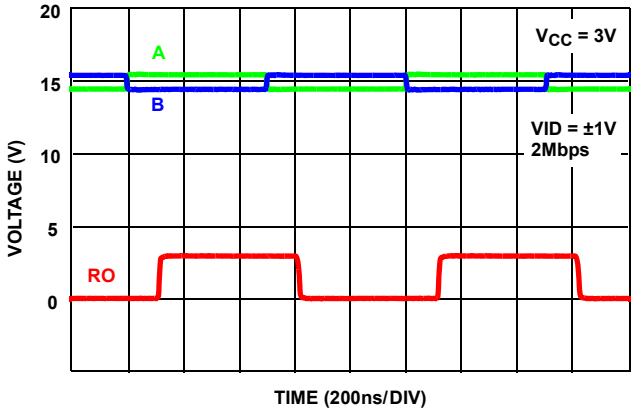


FIGURE 1. EXCEPTIONAL ISL32433E RX OPERATES AT >1Mbps EVEN WITH ±15V COMMON MODE VOLTAGE

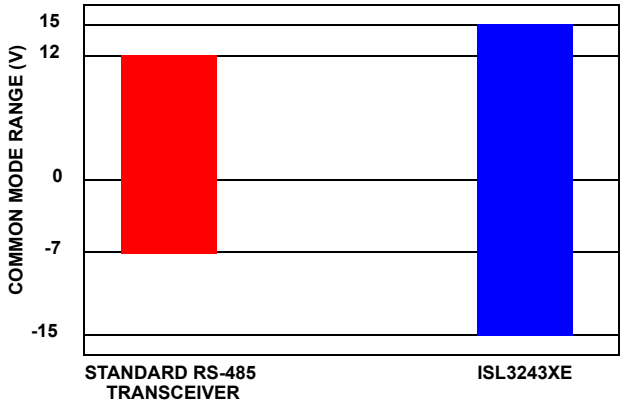


FIGURE 2. TRANSCEIVERS DELIVER SUPERIOR COMMON MODE RANGE vs STANDARD RS-485 DEVICES

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED?	EN PINS?	HOT PLUG	CABLE INVERT (INV) PIN?	QUIESCENT I_{CC} (mA)	LOW POWER SHDN?	PIN COUNT
ISL32430E	Full	0.25	Yes	Yes	No	No	2.1	Yes	10, 14
ISL32432E	Half	0.25	Yes	Yes	No	No	2.1	Yes	8
ISL32433E	Full	1	Yes	Yes	No	No	2.1	Yes	10, 14
ISL32435E	Half	1	Yes	Yes	No	No	2.1	Yes	8
ISL32437E	Half	0.25	Yes	Tx Only	No	Yes	2.1	No	8

Ordering Information

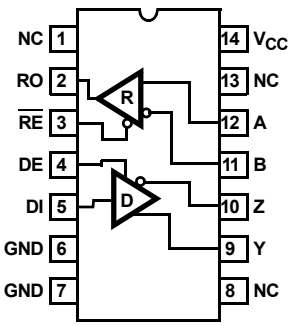
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL32430EIBZ	ISL32430 EIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL32430EIUZ	2430E	-40 to +85	10 Ld MSOP	M10.118
ISL32432EIBZ	32432 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL32432EIUZ	2432E	-40 to +85	8 Ld MSOP	M8.118
ISL32433EIBZ	ISL32433 EIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL32433EIUZ	2433E	-40 to +85	10 Ld MSOP	M10.118
ISL32435EIBZ	32435 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL32435EIUZ	2435E	-40 to +85	8 Ld MSOP	M8.118
ISL32437EIBZ	32437 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL32437EIUZ	2437E	-40 to +85	8 Ld MSOP	M8.118

NOTES:

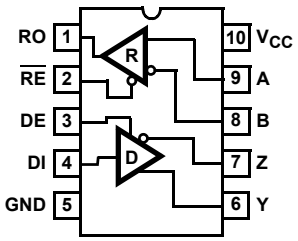
1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL32430E, ISL32432E, ISL32433E, ISL32435E, ISL32437E. For more information on MSL please see tech brief TB363.

Pin Configurations

ISL32430E, ISL32433E
(14 LD SOIC)
TOP VIEW

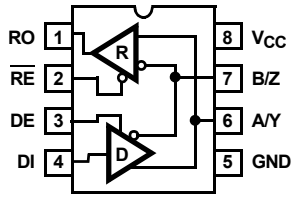


ISL32430E, ISL32433E
(10 LD MSOP)
TOP VIEW

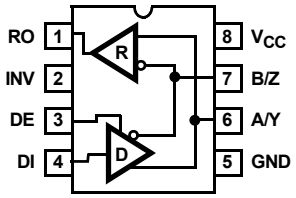


Pin Configurations (Continued)

ISL32432E, ISL32435E
(8 LD SOIC, 8 LD MSOP)
TOP VIEW



ISL32437E
(8 LD SOIC, 8 LD MSOP)
TOP VIEW



Truth Tables

TRANSMITTING					
INPUTS				OUTPUTS	
$\overline{RE}$	DE	DI	INV (Note 4)	Y	Z
X	1	1	0	1	0
X	1	0	0	0	1
X	1	1	1	0	1
X	1	0	1	1	0
0	0	X	X	High-Z	High-Z
1	0	X	X	High-Z*	High-Z*

NOTES:

4. Parts without the INV pin follow the rows with INV = “0” and “X”.
*Low Power Shutdown Mode (See Notes 13 and 18).

RECEIVING					
INPUTS					OUTPUT
$\overline{RE}$ (Note 18)	DE (Half Duplex)	DE (Full Duplex)	A-B	INV (Note 4)	RO
0	0	X	≥ -0.01V	0	1
0	0	X	≤ -0.2V	0	0
0	0	X	≤ 0.01V	1	1
0	0	X	≥ 0.2V	1	0
0	0	X	Inputs Open or Shorted	X	1
1	0	0	X	X	High-Z*
1	1	1	X	X	High-Z

NOTE: *Low Power Shutdown Mode (See Notes 13 and 18).

Pin Descriptions

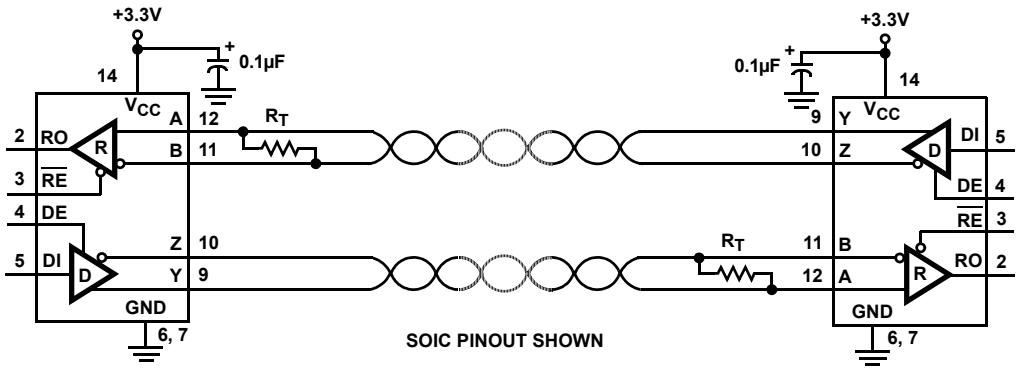
PIN NAME	PIN NUMBER				FUNCTION
	ISL32430E, ISL32433E, 14 LD SOIC	ISL32430E, ISL32433E, 10 LD MSOP	ISL32432E, ISL32435E	ISL32437E	
RO	2	1	1	1	Receiver output. For parts without the cable invert function - or if INV is low - then: If A - B ≥ -10mV, RO is high; if A - B ≤ -200mV, RO is low. If INV is high, then: If B - A ≥ -10mV, RO is high; if B - A ≤ -200mV, RO is low. In all cases, RO = High if A and B are unconnected (floating), or shorted together, or connected to an undriven, terminated bus (i.e., Rx is always failsafe open, shorted, and idle, even if polarity is inverted).
$\overline{RE}$	3	2	2	N/A	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. Internally pulled low.
DE	4	3	3	3	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high, and they are high impedance when DE is low. Internally pulled high.
DI	5	4	4	4	Driver input. For parts without the cable invert function - or if INV is low - a low on DI forces output Y low and output Z high, while a high on DI forces output Y high and output Z low. The output states, relative to DI, invert if INV is high.
GND	6, 7	5	5	5	Ground connection.
A/Y	N/A	N/A	6	6	±40V Fault Protected and ±15kV ESD protected RS-485/RS-422 I/O pin. For parts without the cable invert function - or if INV is low - A/Y is the non-inverting receiver input and non-inverting driver output. If INV is high, A/Y is the inverting receiver input and the inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.

Pin Descriptions (Continued)

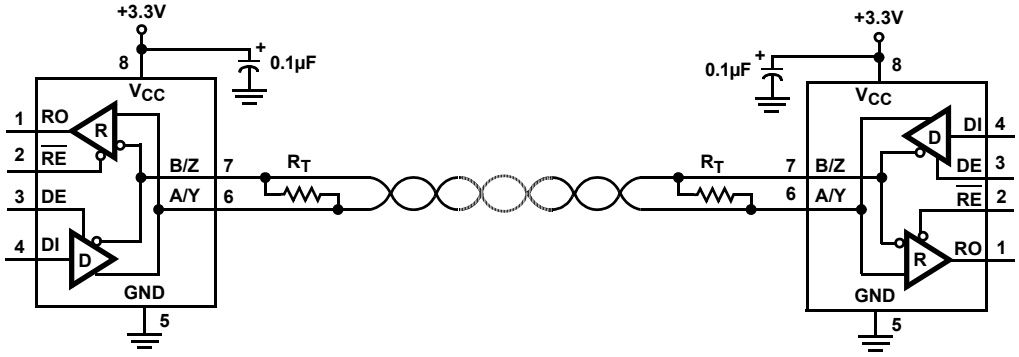
PIN NAME	PIN NUMBER				FUNCTION
	ISL32430E, ISL32433E, 14 LD SOIC	ISL32430E, ISL32433E, 10 LD MSOP	ISL32432E, ISL32435E	ISL32437E	
B/Z	N/A	N/A	7	7	±40V Fault Protected and ±15kV ESD protected RS-485/RS-422 I/O pin. For parts without the cable invert function - or if INV is low - B/Z is the inverting receiver input and inverting driver output. If INV is high, B/Z is the non-inverting receiver input and the non-inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
A	12	9	N/A	N/A	±40V Fault Protected and ±15kV ESD protected RS-485/RS-422 non-inverting receiver input.
B	11	8	N/A	N/A	±40V Fault Protected and ±15kV ESD protected RS-485/RS-422 inverting receiver input.
Y	9	6	N/A	N/A	±40V Fault Protected and ±15kV ESD protected RS-485/RS-422 non-inverting driver output.
Z	10	7	N/A	N/A	±40V Fault Protected and ±15kV ESD protected RS-485/RS-422 inverting driver output.
V_{CC}	14	10	8	8	System power supply input (3V to 5.5V).
INV	N/A	N/A	N/A	2	Receiver and driver Cable Invert (polarity selection) input. When driven high this pin swaps the polarity of the driver output and receiver input pins. If unconnected (floating) or connected low, normal RS-485 polarity conventions apply. Internally pulled low.
NC	1, 8, 13	N/A	N/A	N/A	No Internal Connection.

Typical Operating Circuits

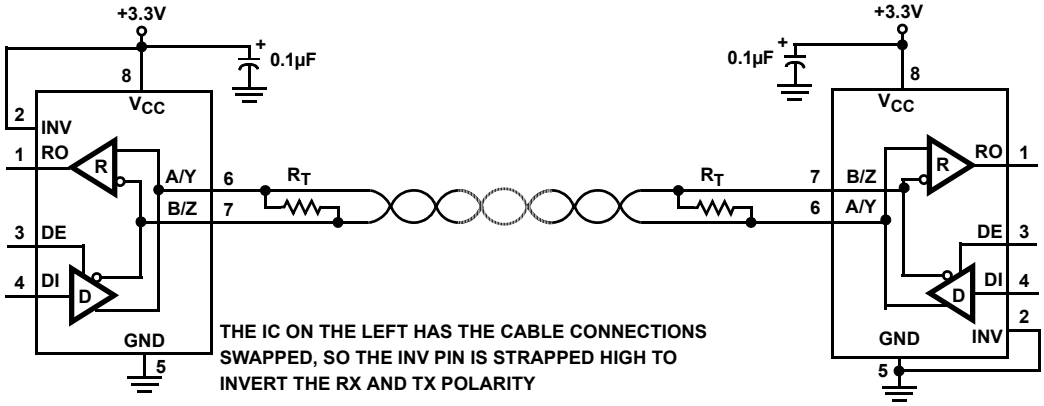
ISL32430E, ISL32433E FULL DUPLEX NETWORK



ISL32432E, ISL32435E HALF DUPLEX NETWORK



ISL32437E HALF DUPLEX NETWORK USING CABLE INVERT FUNCTION



Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$, INV. . . . . -0.3V to V_{CC} + 0.3V
Input/Output Voltages
A/Y, B/Z, A, B, Y, Z . . . . . ±50V
A/Y, B/Z, A, B, Y, Z
(Transient Pulse Through 100Ω, Note 5). . . . . ±60V
RO. . . . . -0.3V to (V_{CC} +0.3V)
Short Circuit Duration
Y, Z . . . . . Indefinite
ESD Rating . . . . . see Specification Table
Latch-up (per JESD78, Level 2, Class A) . . . . . +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 6, 7)	108	47
8 Ld MSOP Package (Notes 6, 7)	140	40
10 Ld MSOP Package (Notes 6, 7)	135	50
14 Ld SOIC Package (Notes 6, 7)	88	39

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage (V_{CC}). . . . . 3.3V or 5V
Temperature Range . . . . . -40°C to +85°C
Bus Pin Common Mode Voltage Range. . . . . -15V to +15V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Tested according to TIA/EIA-485-A, Section 4.2.6 (±60V for 15µs at a 1% duty cycle).
6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 3.6V and 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at the worst case of V_{CC} = 5V or V_{CC} = 3.3V, T_A = +25°C (Note 8). **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 16)	TYP	MAX (Note 16)	UNITS
DC CHARACTERISTICS								
Driver Differential V_{OUT} (No load)	V_{OD1}			Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (Loaded, Figure 3A)	V_{OD2}	R_L = 100Ω (RS-422), V_{CC} ≥ 4.5V		Full	**2**	3	-	V
		R_L = 54Ω (RS-485)	V_{CC} ≥ 4.5V	Full	**1.7**	2.3	-	V
			V_{CC} = 3.3V	Full	**1.35**	1.42	-	V
			V_{CC} ≥ 3V	Full	**1.1**	1.3	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 3A)		Full	-	-	**0.2**	V
Driver Differential V_{OUT} with Common Mode Load (Figure 3B)	V_{OD3}	R_L = 60Ω, -15V ≤ V_{CM} ≤ 15V, V_{CC} ≥ 4.5V		Full	**1.5**	-	-	V
Driver Common-Mode V_{OUT} (Figure 3A)	V_{OC}	R_L = 54Ω or 100Ω		Full	**-1**	-	**3**	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 3A)		Full	-	-	**0.2**	V
Driver Short-Circuit Current	I_{OSD}	DE = V_{CC}, -15V ≤ V_O ≤ 15V (Note 10)		Full	**-250**	-	**250**	mA
	I_{OSD1}	At First Fold-back, 24V ≤ V_O ≤ -24V		Full	**-83**	-	**83**	mA
	I_{OSD2}	At Second Fold-back, 35V ≤ V_O ≤ -35V		Full	**-13**	-	**13**	mA
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$, INV (See Figure 25)		Full	**2.35**	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$, INV		Full	-	-	**0.8**	V
Logic Input Current	I_{IN1}	DI		Full	**-1**	-	**1**	µA
		DE, $\overline{RE}$, INV		Full	**-15**	6	**15**	µA

Electrical Specifications Test Conditions: V_{CC} = 3V to 3.6V and 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at the worst case of V_{CC} = 5V or V_{CC} = 3.3V, T_A = +25°C (Note 8). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 16)	TYP	MAX (Note 16)	UNITS
Input/Output Current (A/Y, B/Z)	I_{IN2}	DE = 0V, V_{CC} = 0V or 3.6V or 5.5V	V_{IN} = 12V	Full	-	-	**250**	µA
			V_{IN} = -7V	Full	**-200**	-	-	µA
			V_{IN} = ±15V	Full	**-800**	-	**850**	µA
			V_{IN} = ±40V, (Note 17)	Full	**-6**	-	**6**	mA
Input Current (A, B) (Full Duplex Versions Only)	I_{IN3}	V_{CC} = 0V or 3.6V or 5.5V	V_{IN} = 12V	Full	-	-	**125**	µA
			V_{IN} = -7V	Full	**-100**	-	-	µA
			V_{IN} = ±15V	Full	**-500**	-	**500**	µA
			V_{IN} = ±40V, (Note 17)	Full	**-3**	-	**3**	mA
Output Leakage Current (Y, Z) (Full Duplex Versions Only)	I_{OZD}	$\overline{RE}$ = 0V, DE = 0V, V_{CC} = 0V or 3.6V or 5.5V	V_{IN} = 12V	Full	-	-	**200**	µA
			V_{IN} = -7V	Full	**-100**	-	-	µA
			V_{IN} = ±15V	Full	**-500**	-	**500**	µA
			V_{IN} = ±40V, (Note 17)	Full	**-3**	-	**3**	mA
Receiver Differential Threshold Voltage	V_{TH}	-15V ≤ V_{CM} ≤ 15V, (For ISL32437E only, A-B if INV = 0; B-A if INV = 1)	V_{CC} ≤ 3.6V	Full	**-200**	-120	**-10**	mV
			V_{CC} ≥ 4.5V	Full	**-250**	-180	**-10**	mV
Receiver Input Hysteresis	ΔV_{TH}	-15V ≤ V_{CM} ≤ 15V		+25	-	30	-	mV
Receiver Output High Voltage	V_{OH1}	V_{ID} = -10mV	I_O = -4mA, V_{CC} ≥ 3V	Full	**2.4**	-	-	V
	V_{OH2}		I_O = -8mA, V_{CC} ≥ 4.5V	Full	**2.4**	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{CC} ≥ 3V, V_{ID} = -200mV		Full	-	-	**0.4**	V
		I_O = 5mA, V_{CC} ≥ 4.5V, V_{ID} = -250mV		Full	-	-	**0.4**	V
Three-State (High Impedance) Receiver Output Current (Note 18)	I_{OZR}	0V ≤ V_O ≤ V_{CC}		Full	**-1**	0.01	**1**	µA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	-	-	**±115**	mA
SUPPLY CURRENT								
No-Load Supply Current (Note 9)	I_{CC}	DE = V_{CC}, $\overline{RE}$ = 0V or V_{CC}, DI = 0V or V_{CC}		Full	-	2.1	**4.5**	mA
Shutdown Supply Current (Note 18)	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}		Full	-	10	**35**	µA
ESD PERFORMANCE								
All Pins		Human Body Model (Tested per JESD22-A114E)		+25	-	±8	-	kV
		Machine Model (Tested per JESD22-A115-A)		+25	-	±700	-	V
RS-485 Pins (A, B, Y, Z, A/Y, B/Z)		Human Body Model, From Bus Pins to GND	Full Duplex	+25	-	±15	-	kV
			Half Duplex	+25	-	±16.5	-	kV
DRIVER SWITCHING CHARACTERISTICS (250kbps Versions; ISL32430E, ISL32432E, ISL32437E)								
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_D = 54Ω, C_D = 50pF (Figure 4)		Full	-	280	**1000**	ns
Driver Differential Output Skew	t_{SKEW}	R_D = 54Ω, C_D = 50pF (Figure 4)		Full	-	4	**100**	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_D = 54Ω, C_D = 50pF (Figure 4)		Full	**250**	650	**1500**	ns
Maximum Data Rate	f_{MAX}	C_D = 820pF (Figure 6)		Full	**250**	-	**-**	kbps
Driver Enable to Output High	t_{ZH}	SW = GND (Figure 5), (Note 11)		Full	-	-	**1600**	ns

Electrical Specifications Test Conditions: V_{CC} = 3V to 3.6V and 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at the worst case of V_{CC} = 5V or V_{CC} = 3.3V, T_A = +25°C (Note 8). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 16)	TYP	MAX (Note 16)	UNITS
Driver Enable to Output Low	t_{ZL}	SW = V_{CC} (Figure 5), (Note 11)	Full	-	-	**1600**	ns
Driver Disable from Output Low	t_{LZ}	SW = V_{CC} (Figure 5)	Full	-	-	**300**	ns
Driver Disable from Output High	t_{HZ}	SW = GND (Figure 5)	Full	-	-	**300**	ns
Time to Shutdown	t_{SHDN}	(Notes 13, 18)	Full	**60**	160	**600**	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	SW = GND (Figure 5), (Notes 13, 14, 18)	Full	-	-	**3000**	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	SW = V_{CC} (Figure 5), (Notes 13, 14, 18)	Full	-	-	**3000**	ns
DRIVER SWITCHING CHARACTERISTICS (1Mbps Versions; ISL32433E and ISL32435E)							
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_D = 54Ω, C_D = 50pF (Figure 4)	Full	-	70	**200**	ns
Driver Differential Output Skew	t_{SKEW}	R_D = 54Ω, C_D = 50pF (Figure 4)	Full	-	4	**25**	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_D = 54Ω, C_D = 50pF (Figure 4)	Full	**50**	130	**300**	ns
Maximum Data Rate	f_{MAX}	C_D = 820pF (Figure 6)	Full	**1**	-	**-**	Mbps
Driver Enable to Output High	t_{ZH}	SW = GND (Figure 5), (Note 11)	Full	-	-	**300**	ns
Driver Enable to Output Low	t_{ZL}	SW = V_{CC} (Figure 5), (Note 11)	Full	-	-	**300**	ns
Driver Disable from Output Low	t_{LZ}	SW = V_{CC} (Figure 5)	Full	-	-	**300**	ns
Driver Disable from Output High	t_{HZ}	SW = GND (Figure 5)	Full	-	-	**300**	ns
Time to Shutdown	t_{SHDN}	(Note 13)	Full	**60**	160	**600**	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	SW = GND (Figure 5), (Notes 13, 14)	Full	-	-	**3000**	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	SW = V_{CC} (Figure 5), (Notes 13, 14)	Full	-	-	**3000**	ns
RECEIVER SWITCHING CHARACTERISTICS (250kbps Versions; ISL32430E, ISL32432E, ISL32437E)							
Maximum Data Rate	f_{MAX}	(Figure 7)	Full	**250**	-	**-**	kbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 7)	Full	-	240	**325**	ns
Receiver Skew $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SKD}	(Figure 7)	Full	-	6	**25**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8), (Notes 12, 18)	Full	-	-	**80**	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8), (Notes 12, 18)	Full	-	-	**80**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8), (Note 18)	Full	-	-	**80**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8), (Note 18)	Full	-	-	**80**	ns
Time to Shutdown	t_{SHDN}	(Notes 13, 18)	Full	**60**	160	**600**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8), (Notes 13, 15, 18)	Full	-	-	**2500**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8), (Notes 13, 15, 18)	Full	-	-	**2500**	ns
RECEIVER SWITCHING CHARACTERISTICS (1Mbps Versions; ISL32433E, ISL32435E)							
Maximum Data Rate	f_{MAX}	(Figure 7)	Full	**1**	-	**-**	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 7)	Full	-	115	**200**	ns

Electrical Specifications Test Conditions: V_{CC} = 3V to 3.6V and 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at the worst case of V_{CC} = 5V or V_{CC} = 3.3V, T_A = +25°C (Note 8). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 16)	TYP	MAX (Note 16)	UNITS
Receiver Skew $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SKD}	(Figure 7)	Full	-	4	**20**	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8), (Note 12)	Full	-	-	**80**	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8), (Note 12)	Full	-	-	**80**	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8)	Full	-	-	**80**	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8)	Full	-	-	**80**	ns
Time to Shutdown	t_{SHDN}	(Note 13)	Full	**60**	160	**600**	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 8), (Notes 13, 15)	Full	-	-	**2500**	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 8), (Notes 13, 15)	Full	-	-	**2500**	ns

NOTES:

8. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
9. Supply current specification is valid for loaded drivers when DE = 0V.
10. Applies to peak current. See “Typical Performance Curves” beginning on page 14 for more information.
11. Keep $\overline{RE}$ = 0 to prevent the device from entering SHDN (does not apply to the ISL32437E).
12. The $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
13. Transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 60ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See “Low Power Shutdown Mode” on page 13.
14. Keep $\overline{RE}$ = VCC, and set the DE signal low time >600ns to ensure that the device enters SHDN.
15. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters SHDN.
16. Compliance to data sheet limits is assured by one or more methods: production test, characterization and/or design.
17. See “Caution” statement below the “Recommended Operating Conditions” section on page 6.
18. Does not apply to the ISL32437E. The ISL32437E has no Rx enable function, and thus no SHDN function.

Test Circuits and Waveforms

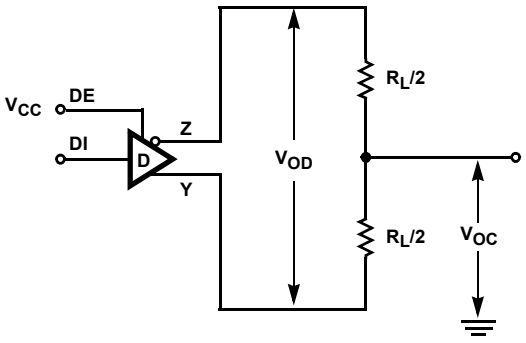


FIGURE 3A. V_{OD} AND V_{OC}

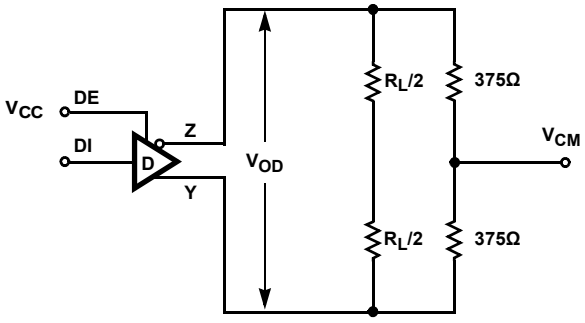


FIGURE 3B. V_{OD} WITH COMMON MODE LOAD

FIGURE 3. DC DRIVER TEST CIRCUITS

Test Circuits and Waveforms (Continued)

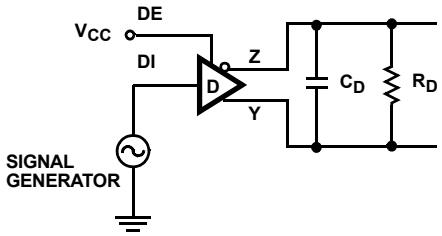


FIGURE 4A. TEST CIRCUIT

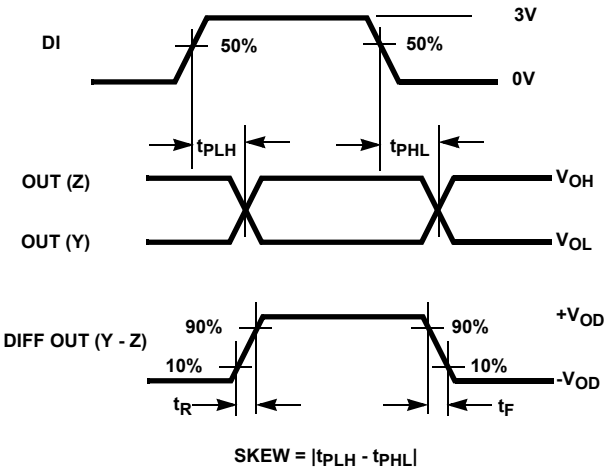
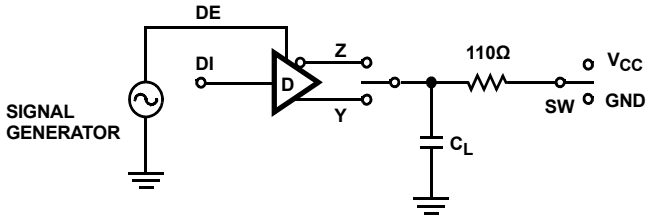


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1/0	GND	50
t_{LZ}	Y/Z	X	0/1	V_{CC}	50
t_{ZH}	Y/Z	0 (Note 11)	1/0	GND	100
t_{ZL}	Y/Z	0 (Note 11)	0/1	V_{CC}	100
$t_{ZH(SHDN)}$	Y/Z	1 (Note 14)	1/0	GND	100
$t_{ZL(SHDN)}$	Y/Z	1 (Note 14)	0/1	V_{CC}	100

FIGURE 5A. TEST CIRCUIT

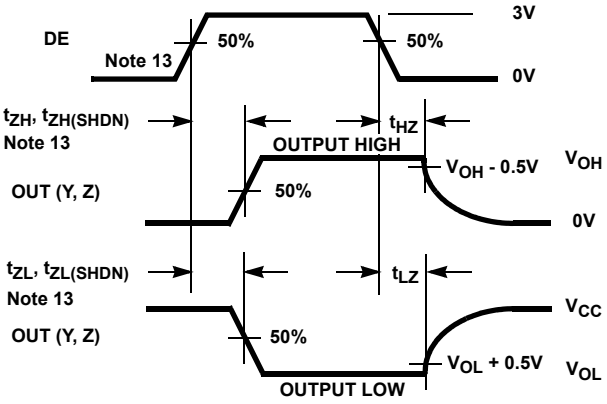


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

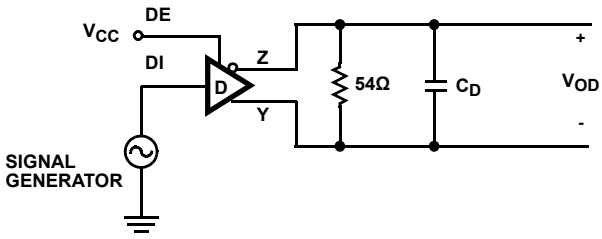


FIGURE 6A. TEST CIRCUIT

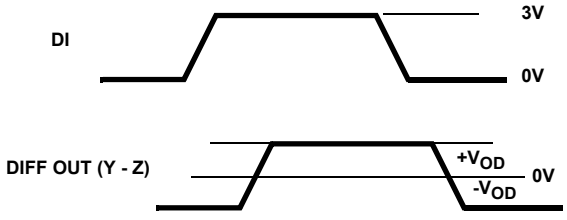


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. DRIVER DATA RATE

Test Circuits and Waveforms (Continued)

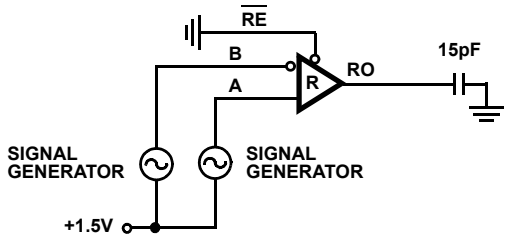


FIGURE 7A. TEST CIRCUIT

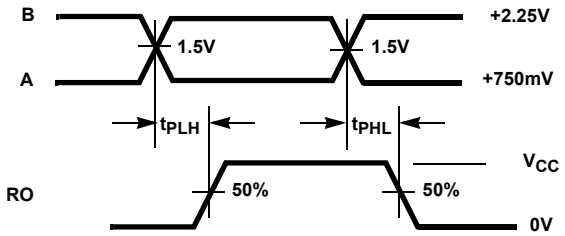
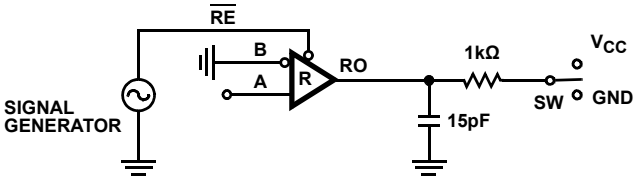


FIGURE 7B. MEASUREMENT POINTS

FIGURE 7. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH} (Note 12)	0	+1.5V	GND
t_{ZL} (Note 12)	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Note 15)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 15)	0	-1.5V	V_{CC}

FIGURE 8A. TEST CIRCUIT

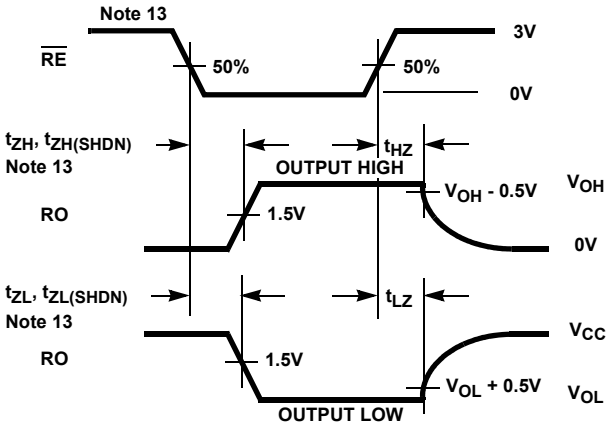


FIGURE 8B. MEASUREMENT POINTS

FIGURE 8. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards used for long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', thus the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

The ISL32430E, ISL32432E, ISL32433E, ISL32435E, ISL32437E are a family of ruggedized RS-485 transceivers that improves on the RS-485 basic requirements, and therefore increases system reliability. The CMR increases to ±15V, while the RS-485 bus pins (receiver inputs and driver outputs) include fault protection against voltages and transients up to ±40V. Additionally, the ±15kV to ±16.5kV built-in ESD protection complements the fault protection.

Receiver (Rx) Features

These devices utilize a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is better than ±200mV (3.3V operation), as required by the RS-422 and RS-485 specifications.

Receiver input (load) current surpasses the RS-422 specification of 3mA, and is four times lower than the RS-485 "Unit Load (UL)" requirement of 1mA maximum. Thus, these products are known as "one-quarter UL" transceivers, and there can be up to 128 of these devices on a network while still complying with the RS-485 loading specification.

The Rx functions with common mode voltages as great as ±15V, making them ideal for industrial, or long networks where induced voltages are a realistic concern.

All the receivers include a "full fail-safe" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated bus with all the transmitters disabled (i.e., an idle bus).

Receivers easily meet the data rates supported by the corresponding driver, and most receiver outputs are three-statable via the active low $\overline{RE}$ input.

The Rx in the 250kbps and 1Mbps versions include noise filtering circuitry to reject high frequency signals. The 1Mbps version typically rejects pulses narrower than 50ns (equivalent to 20Mbps), while the 250kbps Rx rejects pulses below 150ns (6.7Mbps).

Driver (Tx) Features

The RS-485/RS-422 driver is a differential output device that delivers at least 1.7V across a 54Ω load (RS-485), and at least 2V across a 100Ω load (RS-422) with $V_{CC} \geq 4.5V$. The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI, and all drivers are three-statable via the active high DE input.

The 250kbps and 1Mbps driver outputs are slew rate limited to minimize EMI, and to minimize reflections in unterminated or improperly terminated networks.

High Overvoltage (Fault) Protection Increases Ruggedness

The ±40V (referenced to the IC GND) fault protection on the RS-485 pins, makes these transceivers some of the most rugged on the market. This level of protection makes the ISL32430E, ISL32432E, ISL32433E, ISL32435E, ISL32437E perfect for applications where power (e.g., 24V supplies) must be routed in the conduit with the data lines, or for outdoor applications where large transients are likely to occur. When power is routed with the data lines, even a momentary short between the supply and data lines will destroy an unprotected device. The ±40V fault levels of this family are at least **three times higher** than the levels specified for standard RS-485 ICs. The ISL32430E, ISL32432E, ISL32433E, ISL32435E, ISL32437E protection is active whether the Tx is enabled or disabled, and even if the IC is powered down.

If transients or voltages (including overshoots and ringing) greater than ±50V are possible, then additional external protection is required. Use a protection device with the lowest clamping voltage acceptable for the application, and remember that TVS type devices typically clamp 5V to 10V above the designated stand-off voltage (e.g., a "45V TVS" clamps between 50V and 55V).

Wide Common Mode Voltage (CMV) Tolerance Improves Operating Range

RS-485 networks operating in industrial complexes, or over long distances, are susceptible to large CMV variations. Either of these operating environments may suffer from large node-to-node ground potential differences, or CMV pickup from external electromagnetic sources, and devices with only the minimum required +12V to -7V CMR may malfunction. The ISL32430E, ISL32432E, ISL32433E, ISL32435E, ISL32437E's extended ±15V CMR allows for operation in environments that would overwhelm lesser transceivers. Additionally, the Rx will not phase invert (erroneously change state) even with CMVs of ±20V, or differential voltages as large as 40V.

Cable Invert (Polarity Reversal) Function

With large node count RS-485 networks, it is common for some cable data lines to be wired backwards during installation. When this happens, the node is unable to communicate over the network. Once a technician finds the miswired node, he must then rewire the connector, which is time consuming.

The ISL32437E simplifies this task by including a cable invert pin (INV) that allows the technician to invert the polarity of the Rx input and the Tx output pins simply by moving a jumper to change the state of the invert pin. When the invert pin is low, the

IC operates like any standard RS-485 transceiver, and the bus pins have their normal polarity definition of A and Y being noninverting and B and Z being inverting. With the invert pin high, the corresponding bus pins reverse their polarity, so B and Z are now noninverting, and A and Y become inverting.

Intersil's unique cable invert function is superior to that found on competing devices, because the Rx full fail-safe function is maintained, even when the Rx polarity is reversed. Competitor devices implement the Rx invert function simply by inverting the Rx output. This means that with the Rx inputs floating or shorted together, the Rx appropriately delivers a logic 1 in normal polarity, but outputs a logic low when the IC is operated in the inverted mode. Intersil's innovative Rx design guarantees that, with the Rx inputs floating or shorted together (V_{ID} = 0V), the Rx output remains high, regardless of the state of the invert pin.

Data Rate, Cables, and Terminations

RS-485/RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Devices operating at 1Mbps can operate at full data rates with lengths up to 800' (244m). Jitter is the limiting parameter at this faster data rate, so employing encoded data streams (e.g., Manchester coded or Return-to-Zero) may allow increased transmission distances. The slow versions can operate at 115kbps, or less, at the full 4000' (1220m) distance, or at 250kbps for lengths up to 3000' (915m). DC cable attenuation is the limiting parameter, so using better quality cables (e.g., 22 AWG) may allow increased transmission distance.

Twisted pair is the cable of choice for RS-485/RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

Short networks using the 250kbps versions need not be terminated, however, terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus like RS-422) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible.

Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. These transceivers meet this requirement via driver output short circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate a double fold-back short circuit current limiting scheme, which ensures that the output current never exceeds the RS-485 specification, even at the common mode and fault condition voltage range extremes. The first fold-back current level (≈83mA) is set to ensure that the driver never folds back when driving loads with common mode voltages up to ±15V. The very low second fold-back current setting (≈13mA) minimizes power dissipation if the Tx is enabled when a fault occurs.

In the event of a major short circuit condition, devices also include a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about +15°C. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode

These BiCMOS transceivers all use a fraction of the power required by competitive devices, but they (excluding ISL32437E) also include a shutdown feature that reduces the already low quiescent I_{CC} to a 10µA trickle. These devices enter shutdown whenever the receiver and driver are *simultaneously* disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 60ns guarantees that the transceiver will not enter shutdown.

Note that receiver and driver enable times increase when the transceiver enables from shutdown. Refer to Notes 11, 12, 13, 14 and 15, at the end of the "Electrical Specification" table on page 9, for more information.

Typical Performance Curves T_A = +25°C; Unless Otherwise Specified.

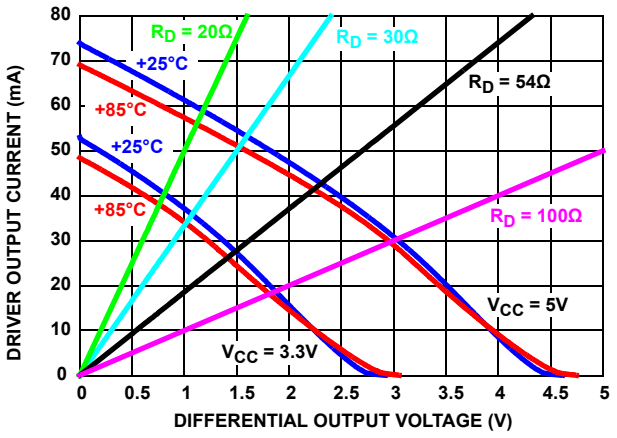


FIGURE 9. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

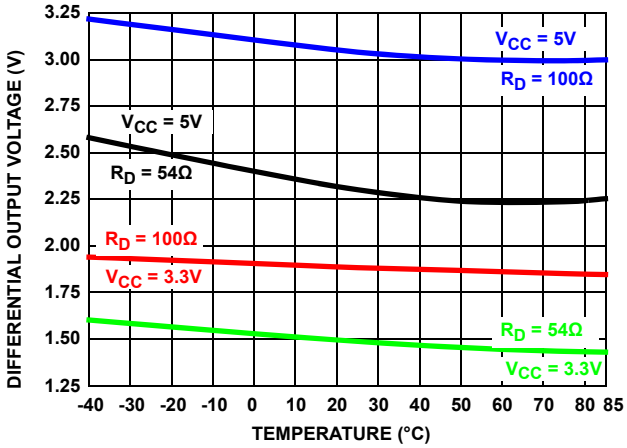


FIGURE 10. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

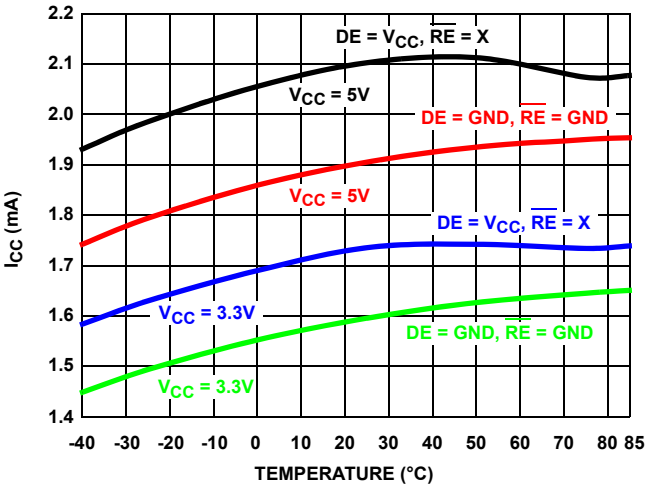


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

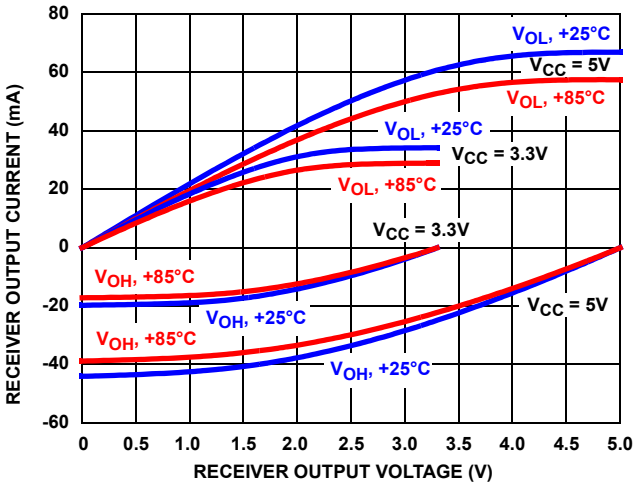


FIGURE 12. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

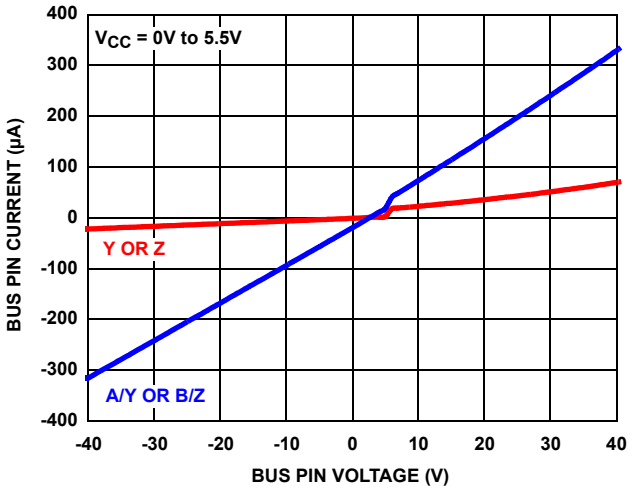


FIGURE 13. BUS PIN CURRENT vs BUS PIN VOLTAGE

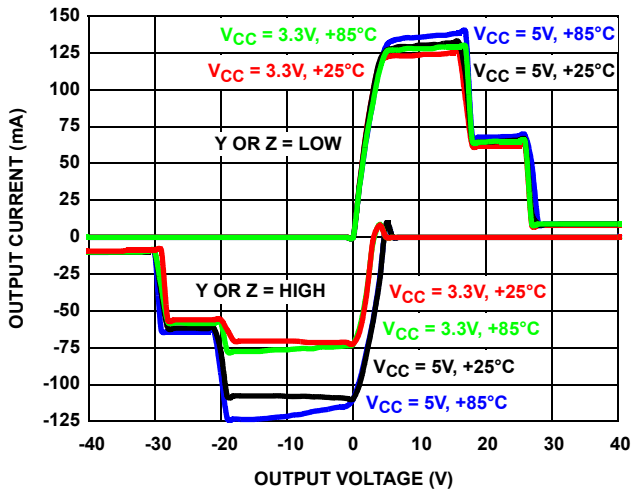


FIGURE 14. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

Typical Performance Curves T_A = +25°C; Unless Otherwise Specified. **(Continued)**

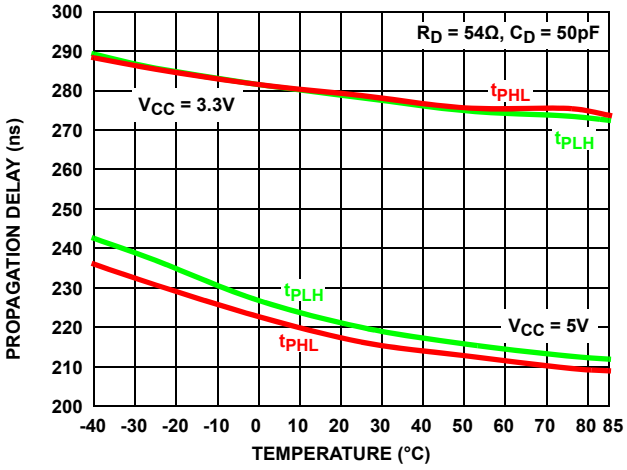


FIGURE 15. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32430E, ISL32432E, ISL32437E)

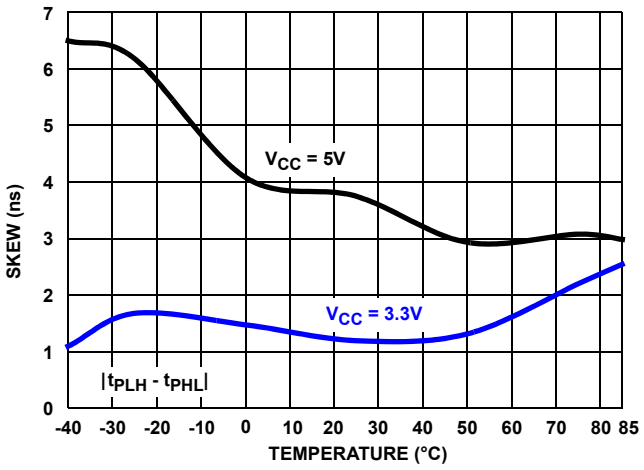


FIGURE 16. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL32430E, ISL32432E, ISL32437E)

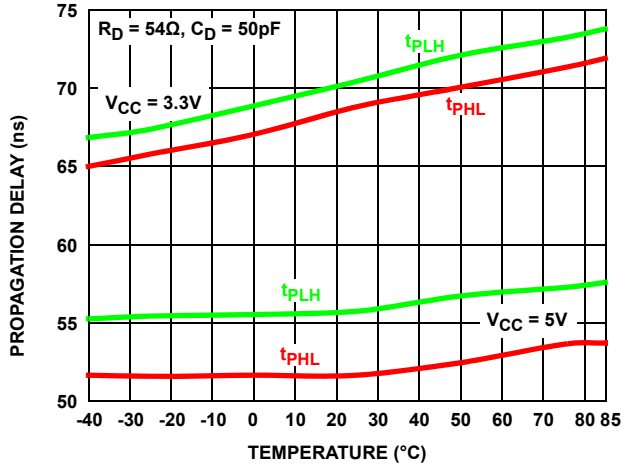


FIGURE 17. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32433E, ISL32435E)

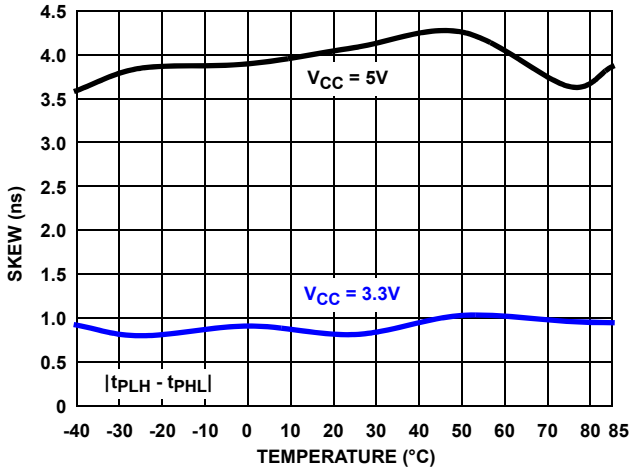


FIGURE 18. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL32433E, ISL32435E)

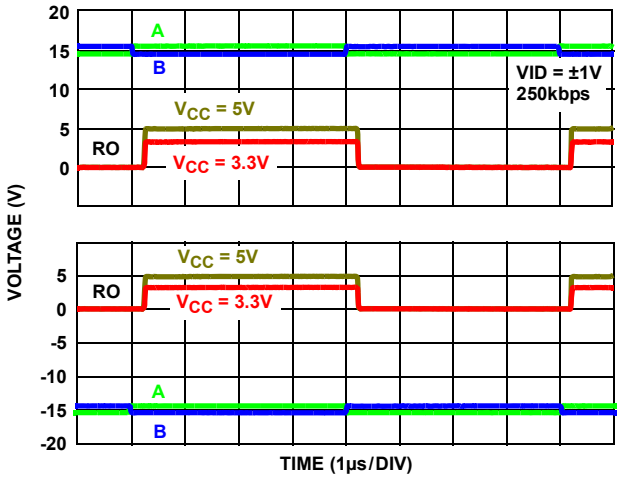


FIGURE 19. ±15V RECEIVER PERFORMANCE (ISL32430E, ISL32432E, ISL32437E)

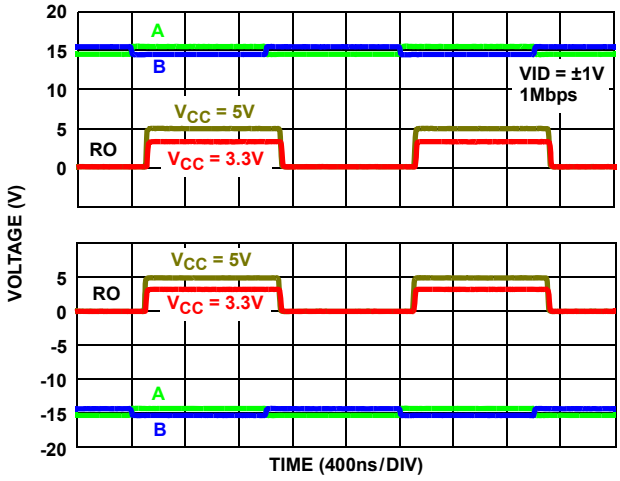


FIGURE 20. ±15V RECEIVER PERFORMANCE (ISL32433E, ISL32435E)

Typical Performance Curves T_A = +25°C; Unless Otherwise Specified. **(Continued)**

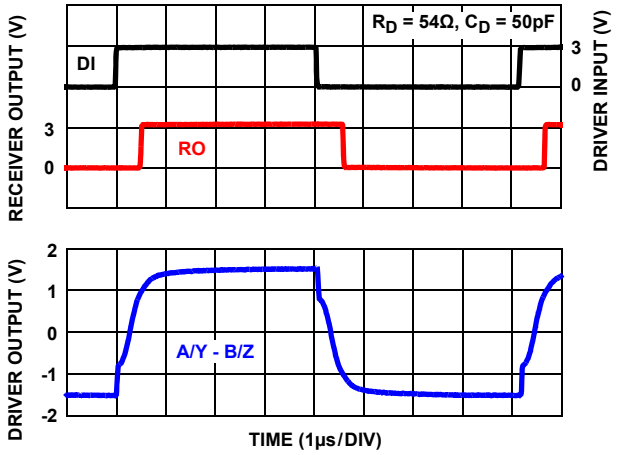


FIGURE 21. V_{CC} = 3.3V, DRIVER AND RECEIVER WAVEFORMS (ISL32430E, ISL32432E, ISL32437E)

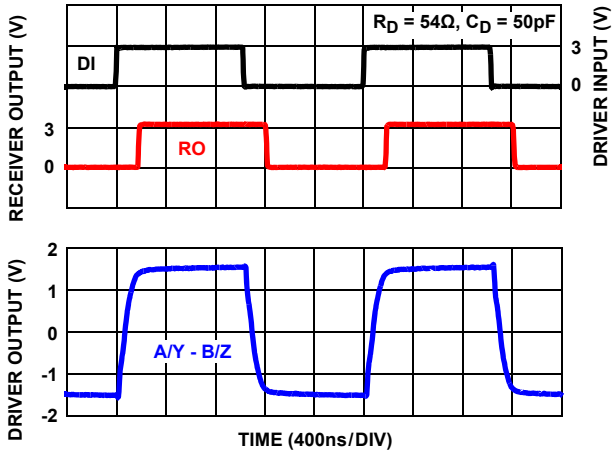


FIGURE 22. V_{CC} = 3.3V, DRIVER AND RECEIVER WAVEFORMS (ISL32433E, ISL32435E)

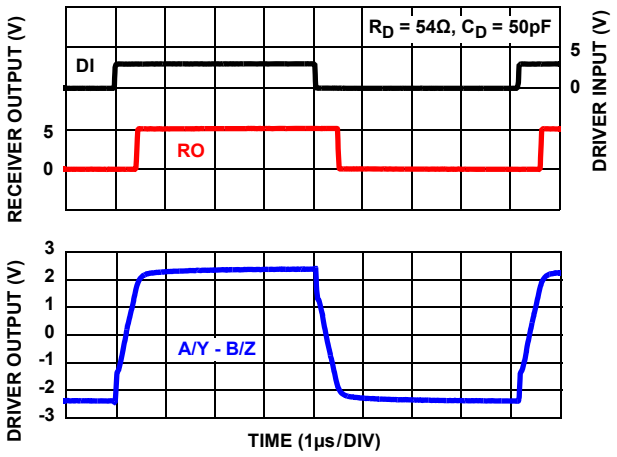


FIGURE 23. V_{CC} = 5V, DRIVER AND RECEIVER WAVEFORMS (ISL32430E, ISL32432E, ISL32437E)

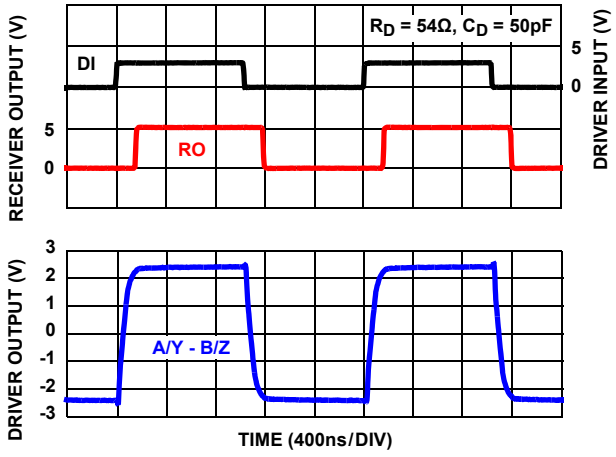


FIGURE 24. V_{CC} = 5V, DRIVER AND RECEIVER WAVEFORMS (ISL32433E, ISL32435E)

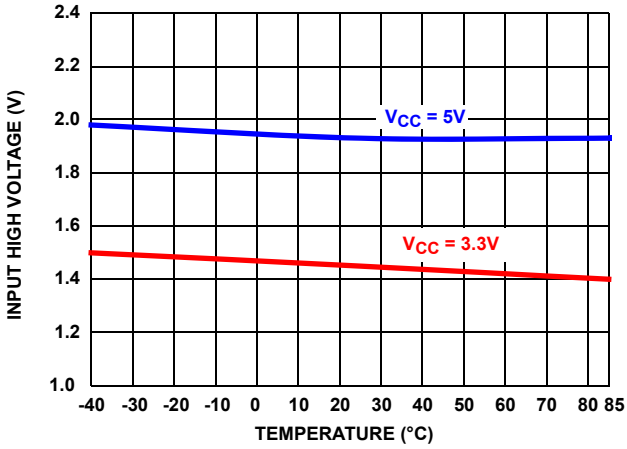


FIGURE 25. LOGIC INPUT HIGH VOLTAGE vs TEMPERATURE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP) :

GND

PROCESS:

Si Gate BiCMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
March 1, 2012	FN7920.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL32430E, ISL32432E, ISL32433E, ISL32435E, ISL32437E

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

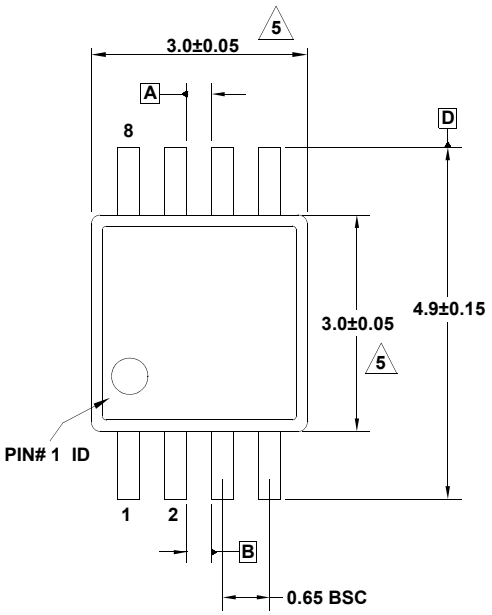
FITs are available from our website at http://rel.intersil.com/reports/search.php

Package Outline Drawing

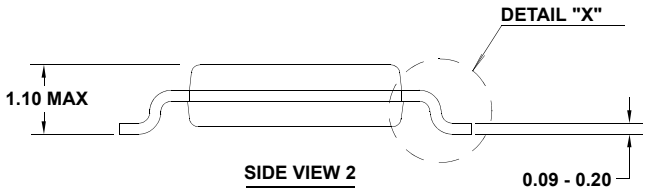
M8.118

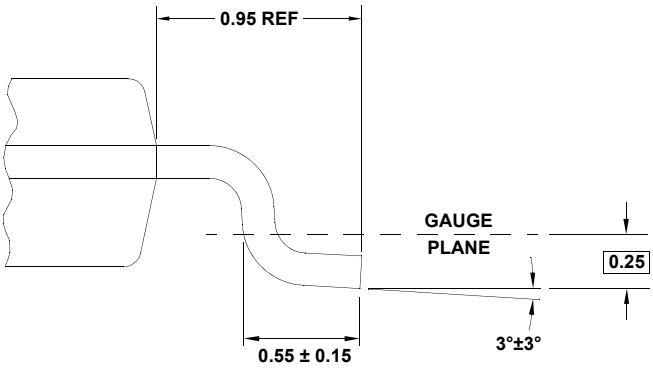
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11

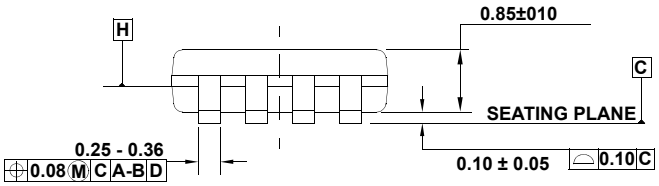


TOP VIEW

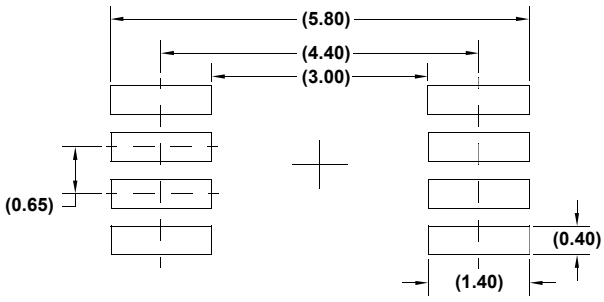




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

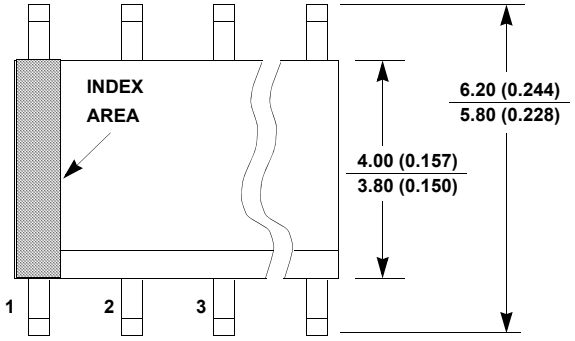
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

Package Outline Drawing

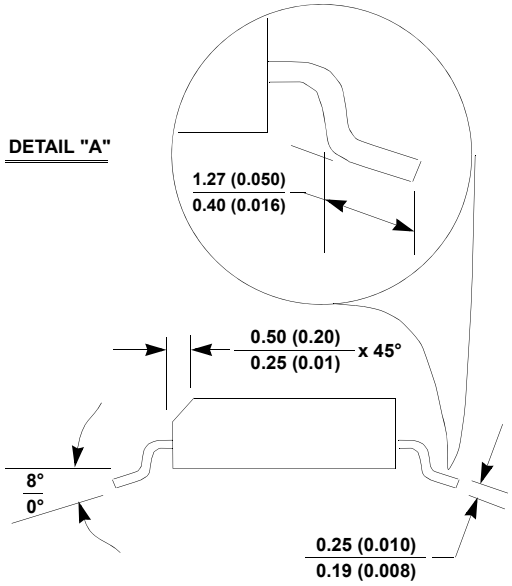
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

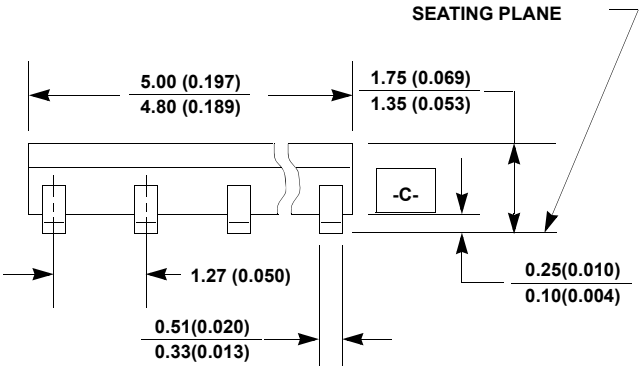
Rev 4, 1/12



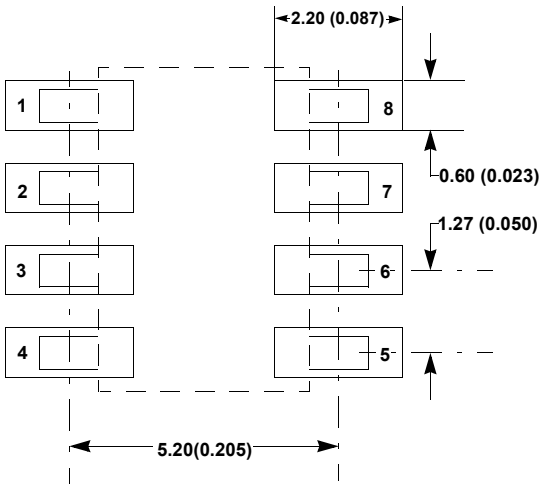
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"

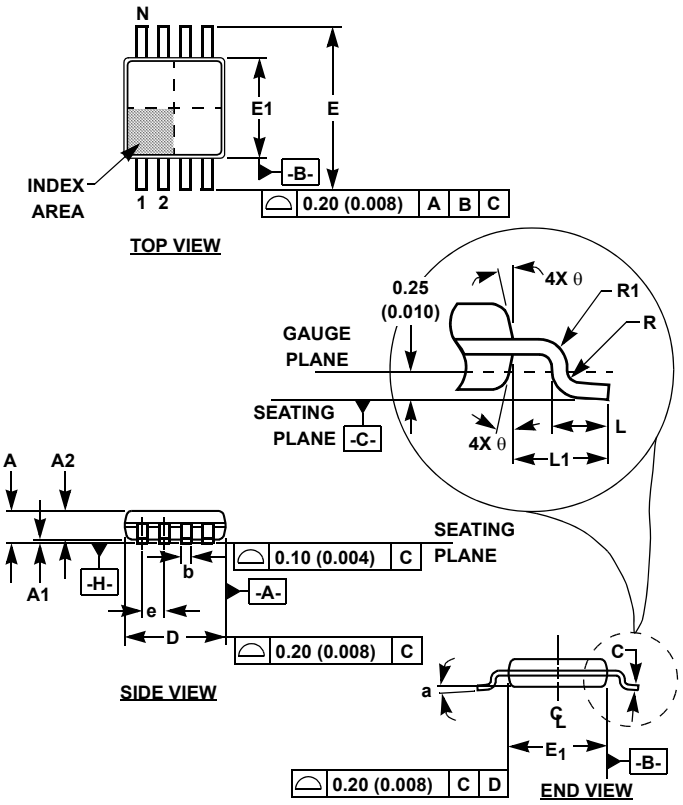


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 0 12/02

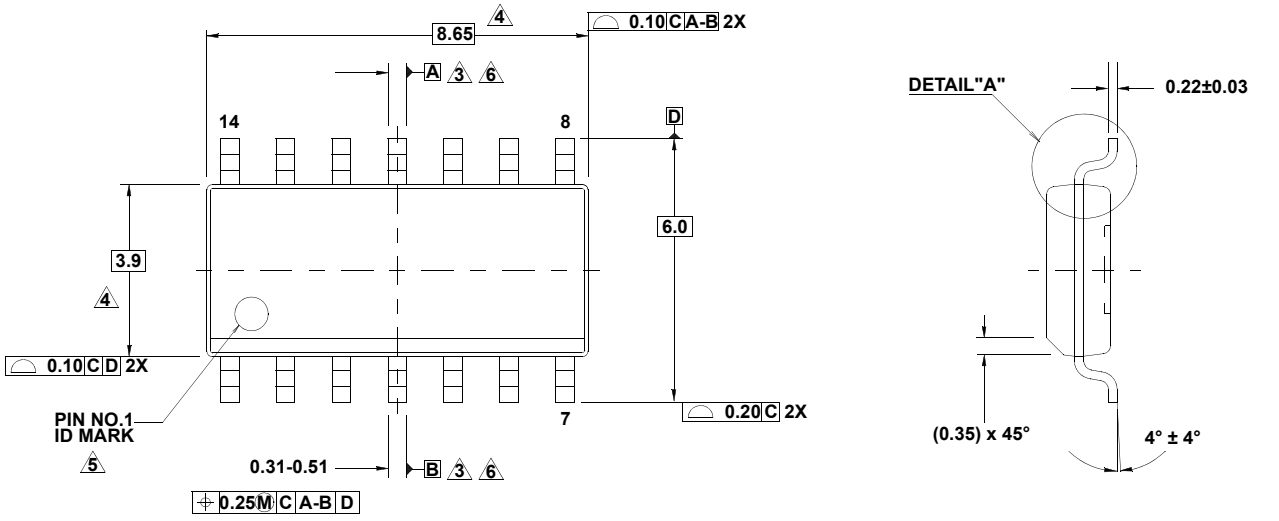
NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

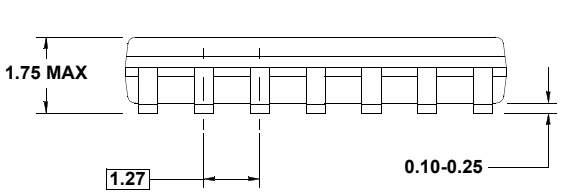
Package Outline Drawing

M14.15

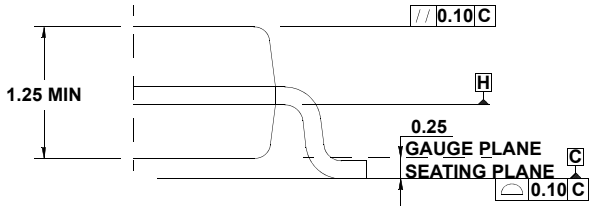
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 1, 10/09



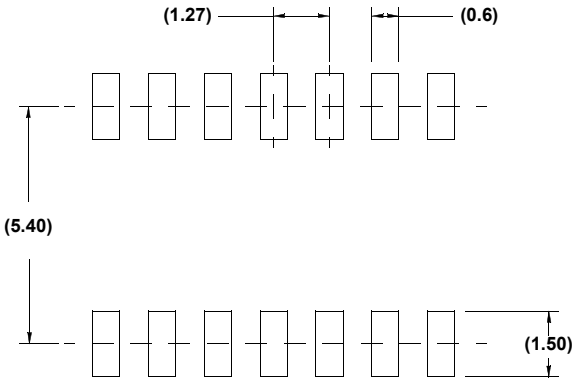
TOP VIEW



SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

Mouser Electronics

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