PRELIMINARY

Am53C94/Am53C96

High Performance SCSI Controller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Pin/function compatible with NCR53C94/53C96**
- **AMD's Patented GLITCH EATER™ Circuitry on $\overline{REQ}$ and $\overline{ACK}$ inputs**
- **5 Mbytes per second synchronous SCSI transfer rate**
- **20 Mbytes per second DMA transfer rate**
- **16-bit DMA Interface plus 2 bits of parity**
- **Flexible three bus architecture**
- **Single ended SCSI bus supported by Am53C94**
- **Single ended and differential SCSI bus supported by Am53C96**
- **Selection of multiplexed or non-multiplexed address and data bus**
- **High current drivers (48 mA) for direct connection to the single ended SCSI bus**
- **Supports Disconnect and Reselect commands**
- **Supports burst mode DMA operation with a threshold of 8**
- **Supports 3-byte-tagged queuing as per the SCSI-2 specification**
- **Supports group 2 and 5 command recognition as per the SCSI-2 specification**
- **Advanced CMOS process for low power consumption**
- **Am53C94 available in 84-pin PLCC package**
- **Am53C96 available in 100-pin PQFP package**

GENERAL DESCRIPTION

The High Performance SCSI Controller (HPSC) has a flexible three bus architecture. The HPSC has a 16-bit DMA interface, an 8 bit host data interface and an 8-bit SCSI data interface. The HPSC is designed to minimize host intervention by implementing common SCSI sequences in hardware. An on-chip state machine reduces protocol overheads by performing the required sequences in response to a single command from the host. Selection, reselection, information transfer and disconnection commands are directly supported.

The 16-byte-internal FIFO further assists in minimizing host involvement. The FIFO provides a temporary storage for all command, data, status and message bytes as they are transferred between the 16 bit host data bus and the 8 bit SCSI data bus. During DMA operations the FIFO acts as a buffer to allow greater latency in the DMA channel. This permits the DMA channel to be suspended for higher priority operations such as DRAM refresh or reception of an ISDN packet.

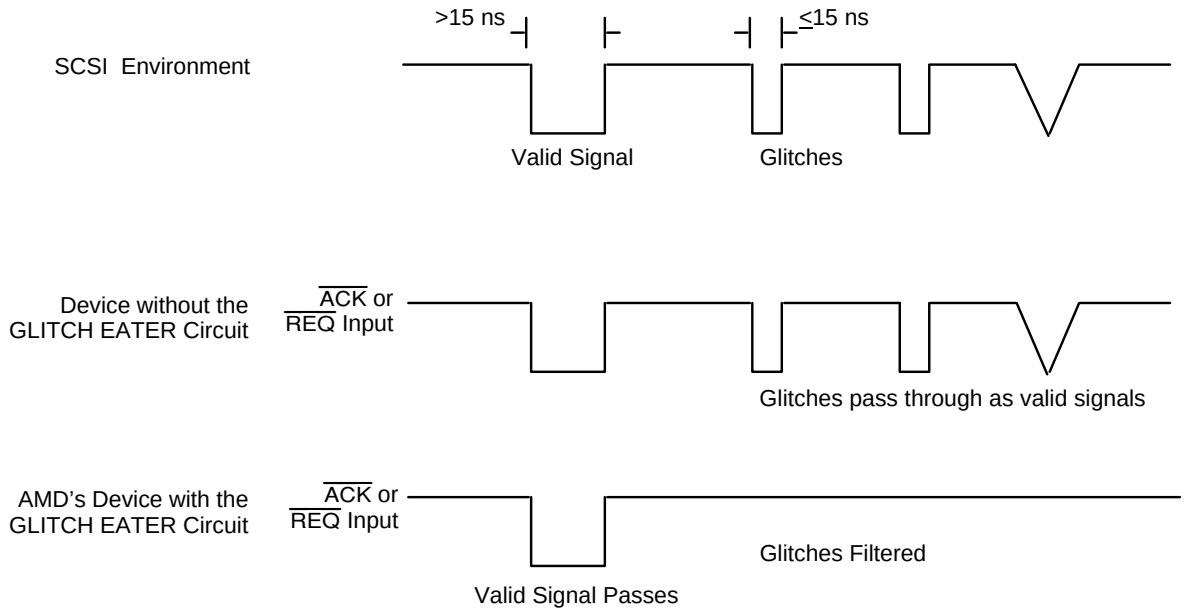
Parity on the DMA bus is optional. Parity can either be generated and checked or it can be simply passed through.

The patented GLITCH EATER Circuitry in the High Performance SCSI Controller detects signal changes that are less than or equal to 15 ns and filters them out. It is designed to dramatically increase system performance and reliability by detecting and filtering glitches that can cause system failure.

The GLITCH EATER Circuitry is implemented on the $\overline{ACK}$ and $\overline{REQ}$ lines only. These lines often encounter many electrical anomalies which degrade system performance and reliability. The two most common are Reflections and Voltage Spikes. Reflections are a result of high current SCSI signals that are mismatched by stubs, cables and terminators. These reflections vary from application to application and can trigger false handshake signals on the $\overline{ACK}$ and $\overline{REQ}$ lines if the voltage amplitude is at the TTL threshold levels. Spikes are generated by high current SCSI signals switching concurrently. On the control signals ($\overline{ACK}$ and $\overline{REQ}$) they can trigger false data transfers which result in loss of data, addition of random data, double clocking and reduced system reliability. AMD's GLITCH EATER Circuitry helps maintain excellent system performance by treating the glitches. Refer to the diagram on the next page.

Publication# **16506** Rev. **C** Amendment **/0**
Issue Date: **May 1993**

GLITCH EATER Circuitry in SCSI Environment



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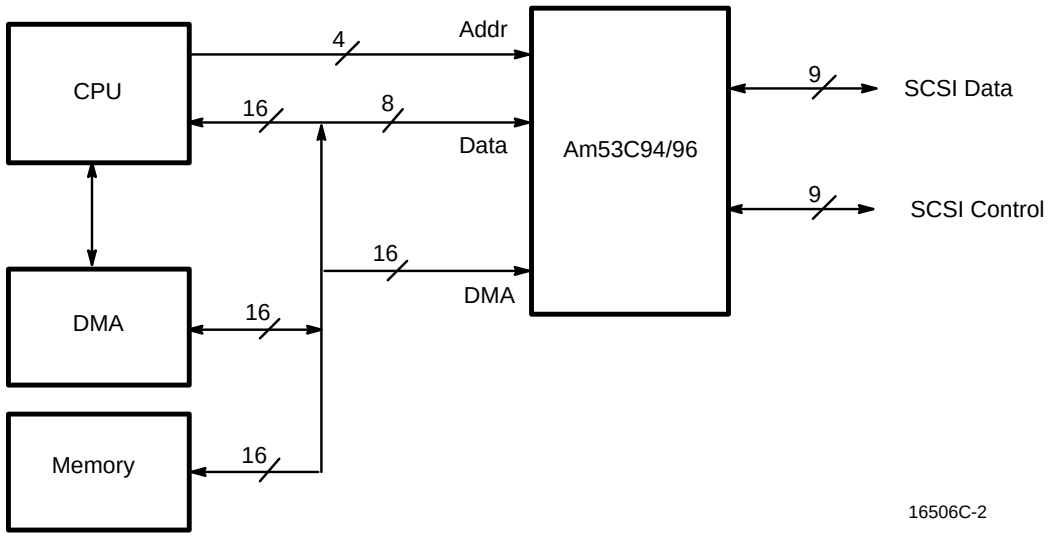
SYSTEM BLOCK DIAGRAM



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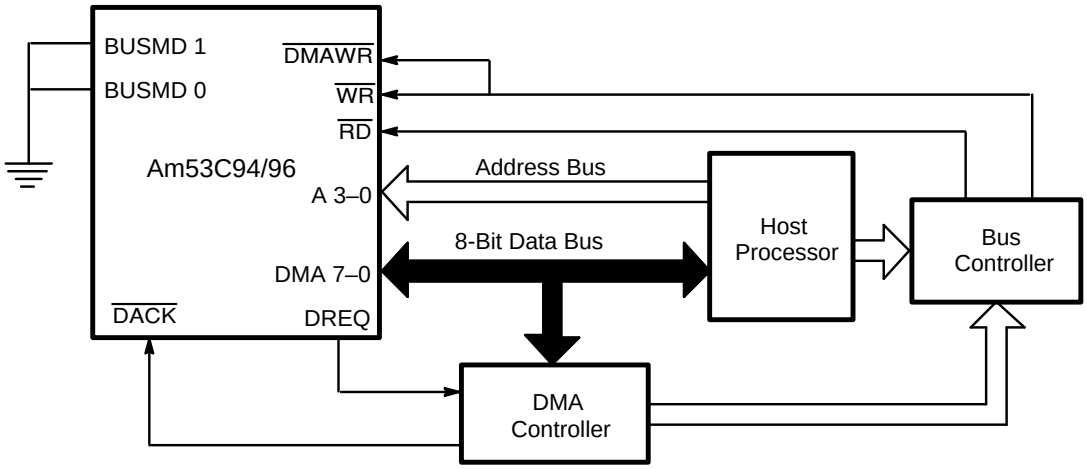
SYSTEM BUS MODE DIAGRAMS



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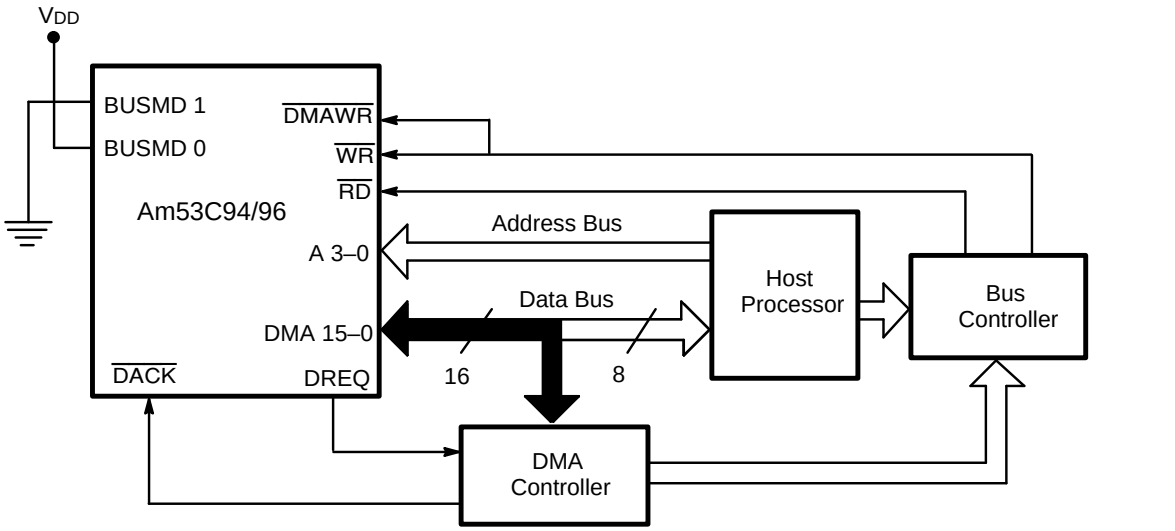
Bus Mode 0



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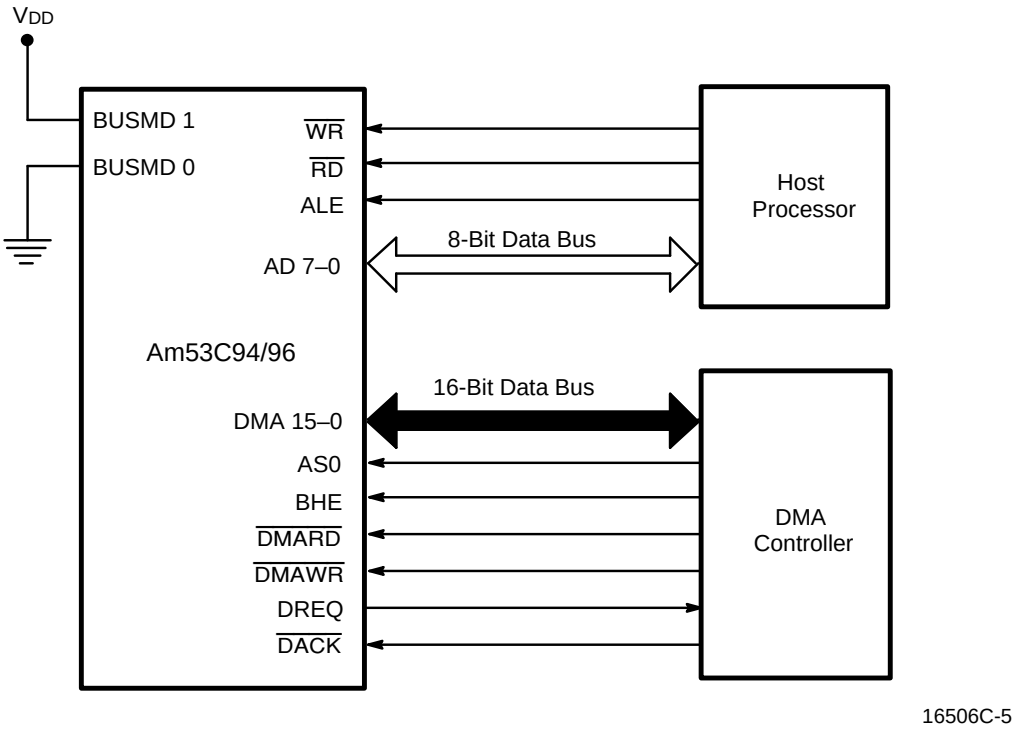
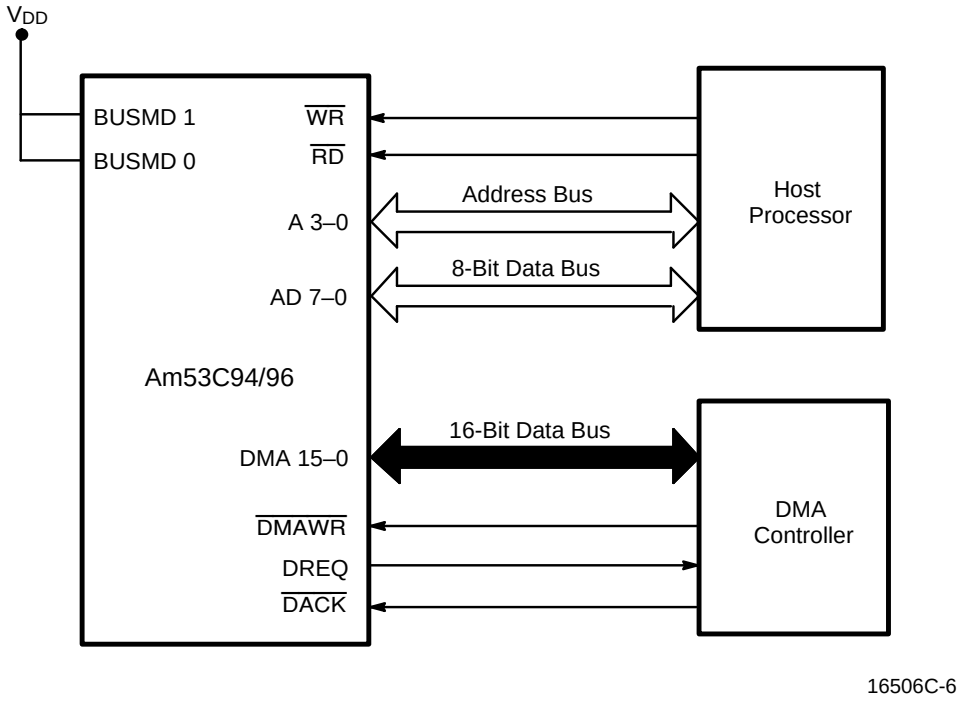
Bus Mode 1

SYSTEM BUS MODE DIAGRAMS

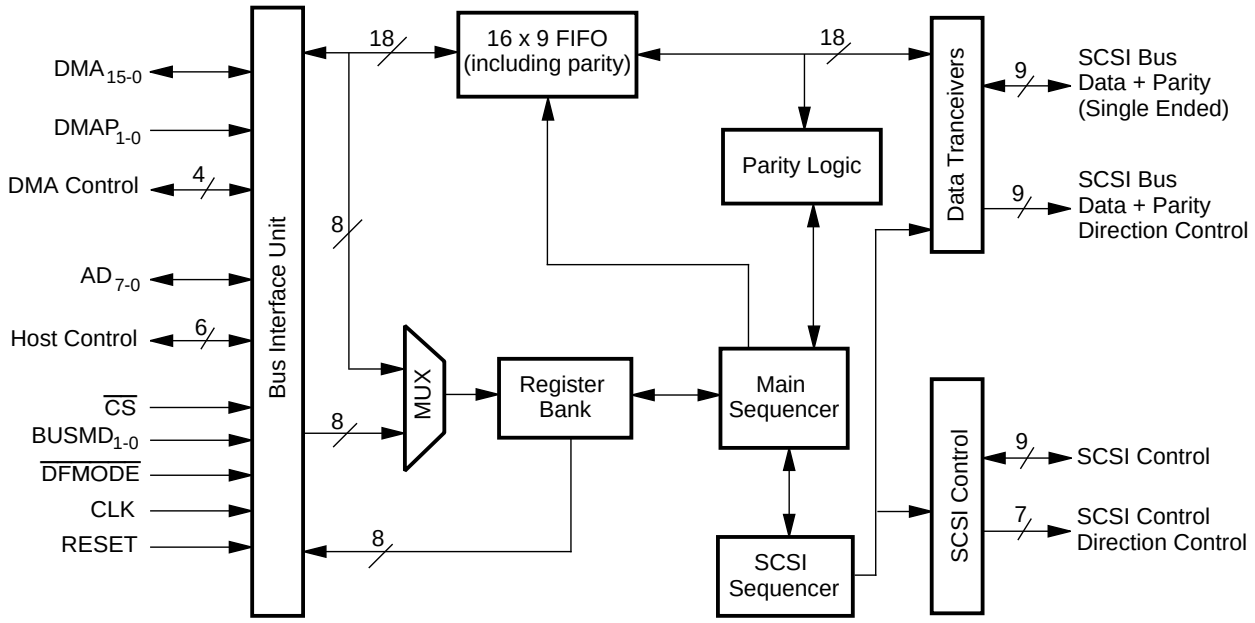


Bus Mode 2



Bus Mode 3

BLOCK DIAGRAM



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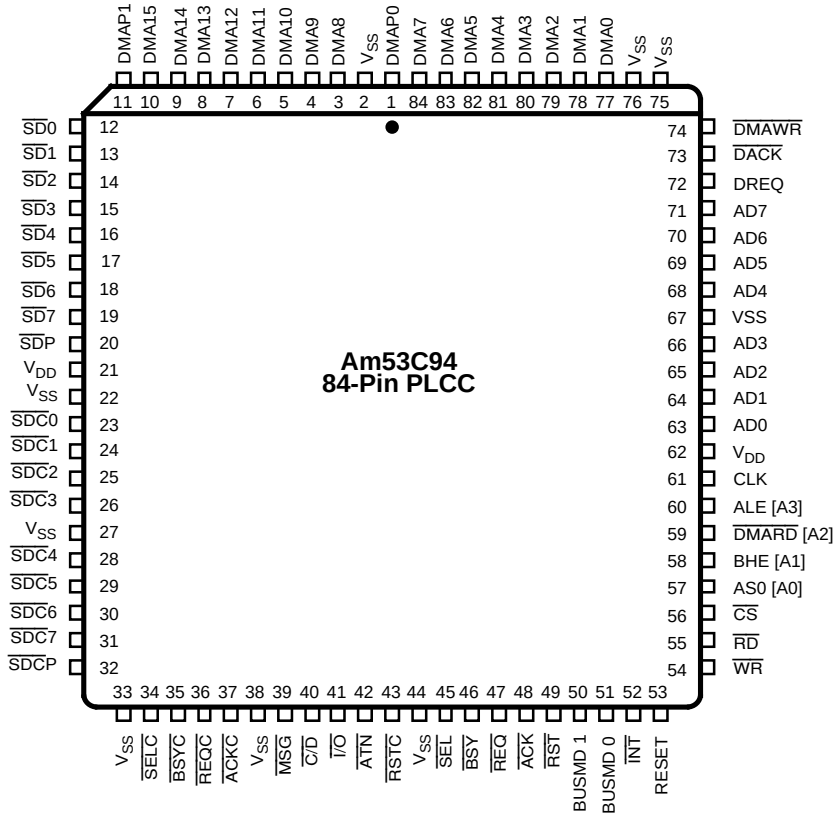
CONNECTION DIAGRAMS

Top View



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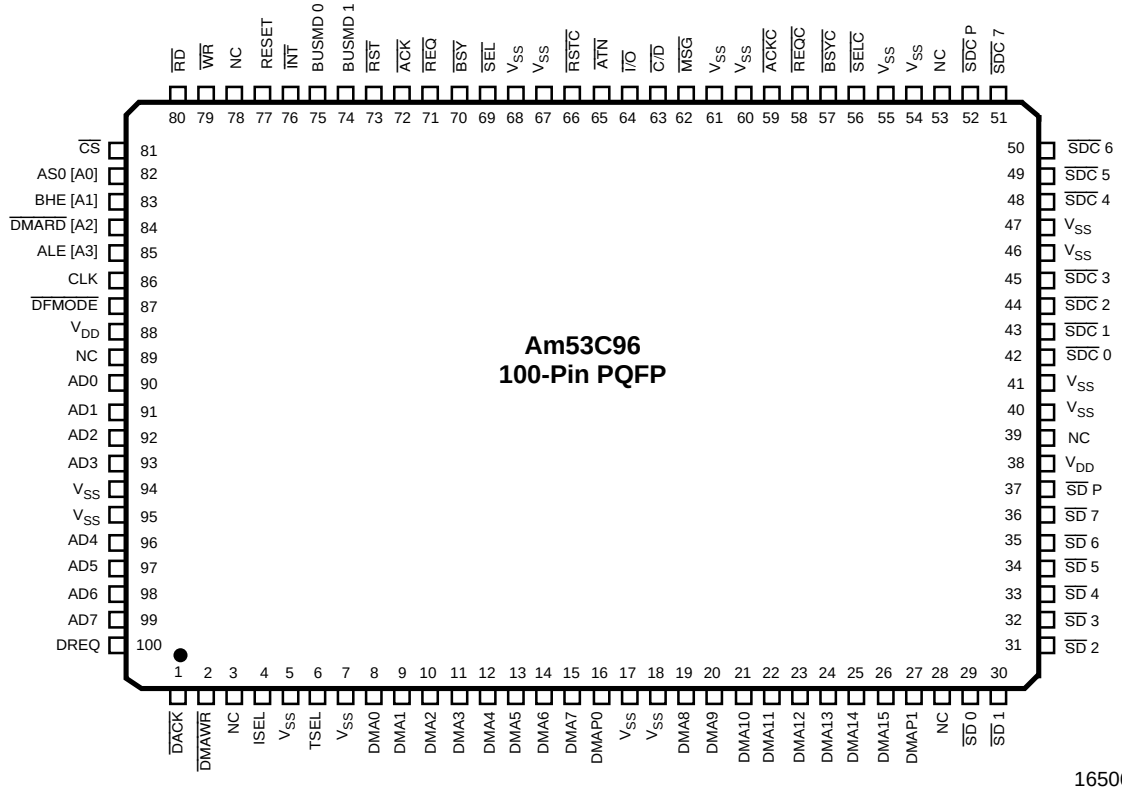

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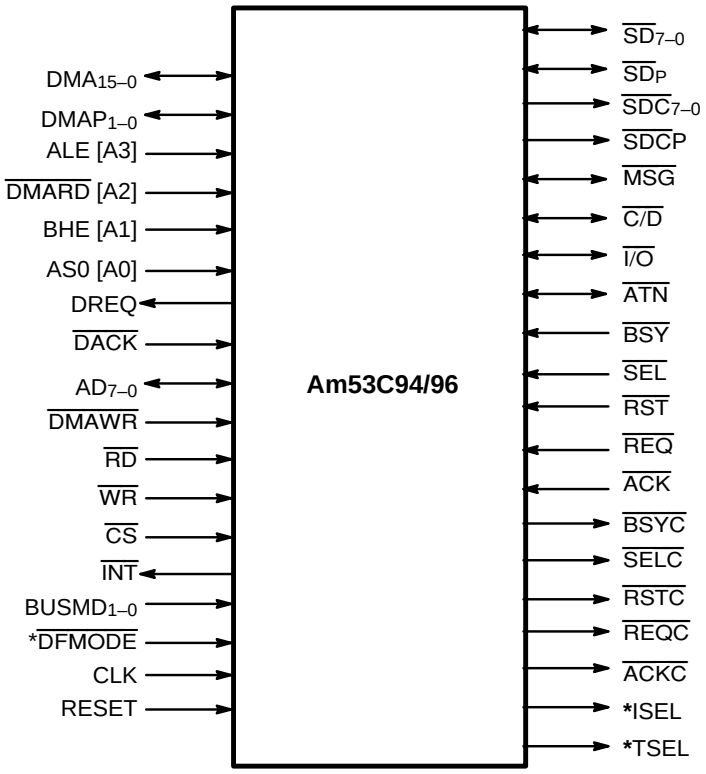
LOGIC SYMBOL



Note:

**Pins available on the Am53C96 only.*

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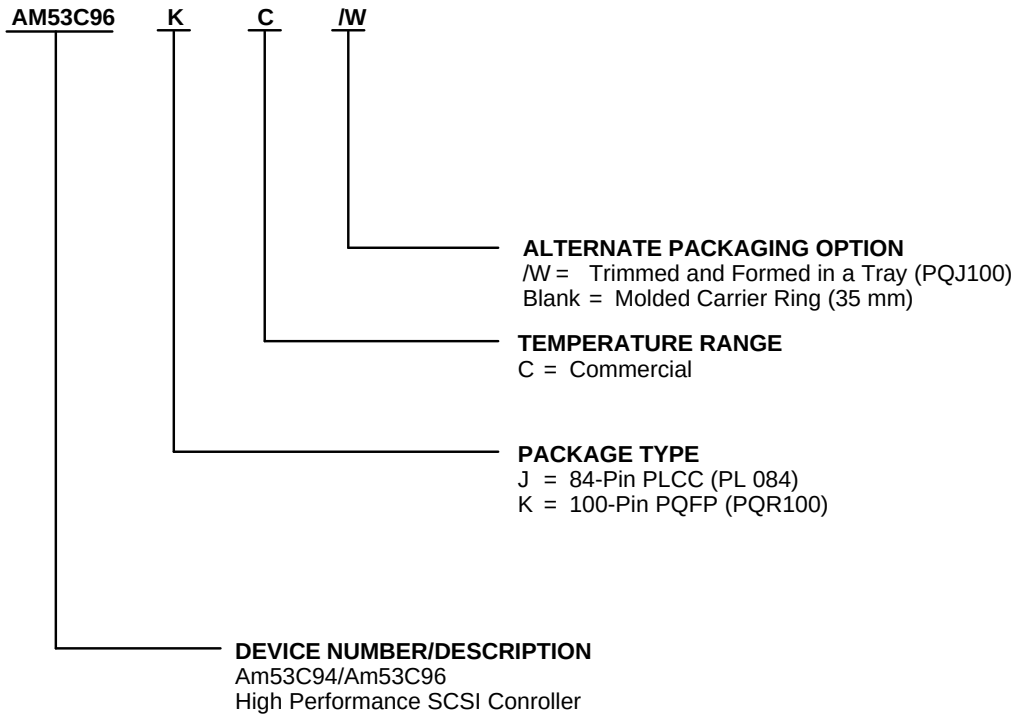
RELATED AMD PRODUCTS

Part Number	Description	Part Number	Description
85C30	Enhanced Serial Communcaiton Controller	Am386™	High-Performance 32-Bit Microprocessor
26LSXX	Line Drivers/Receivers	80188	Highly Integrated 8-Bit Microprocessor
33C93A	Enhanced CMOS SCSI Bus Interface Controller	53C80A	SCSI Bus Controller
80C186	Highly Integrated 16-Bit Microprocessor	85C80	Combination 53C80A SCSI and 85C30 ESCC
80C286 80286	High-Performance 16-Bit Microprocessor	53C94LV	Low Voltage, High Performance SCSI Controller

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

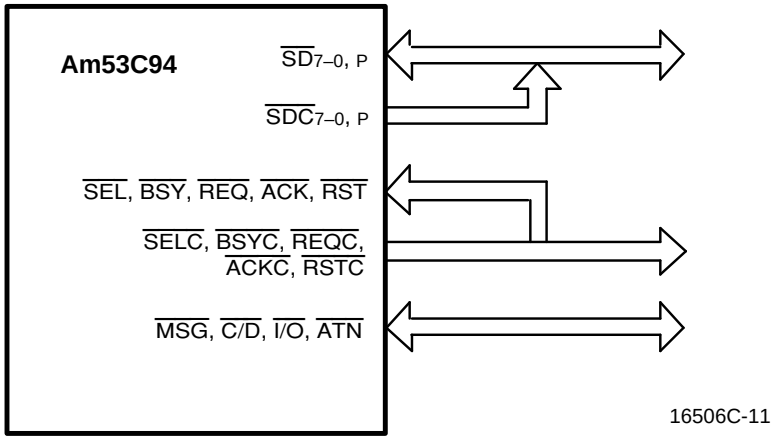


Valid Combinations	
AM53C94	JC
AM53C96	KC, KC/W

Valid Combinations

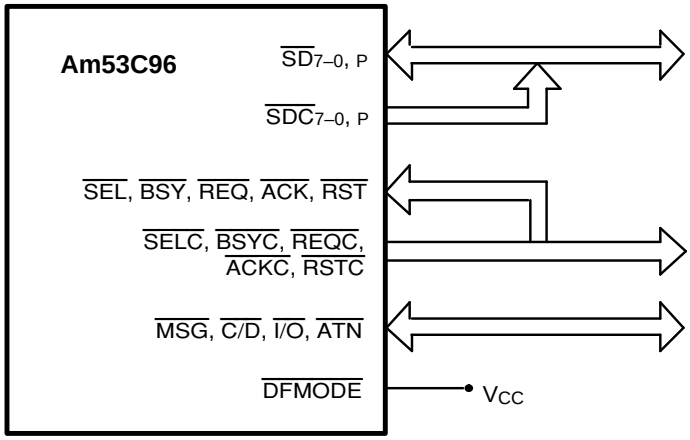
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

SCSI OUTPUT CONNECTIONS



Am53C94 Single Ended SCSI Bus Configuration

SCSI OUTPUT CONNECTIONS



Am53C96 Single Ended SCSI Bus Configuration

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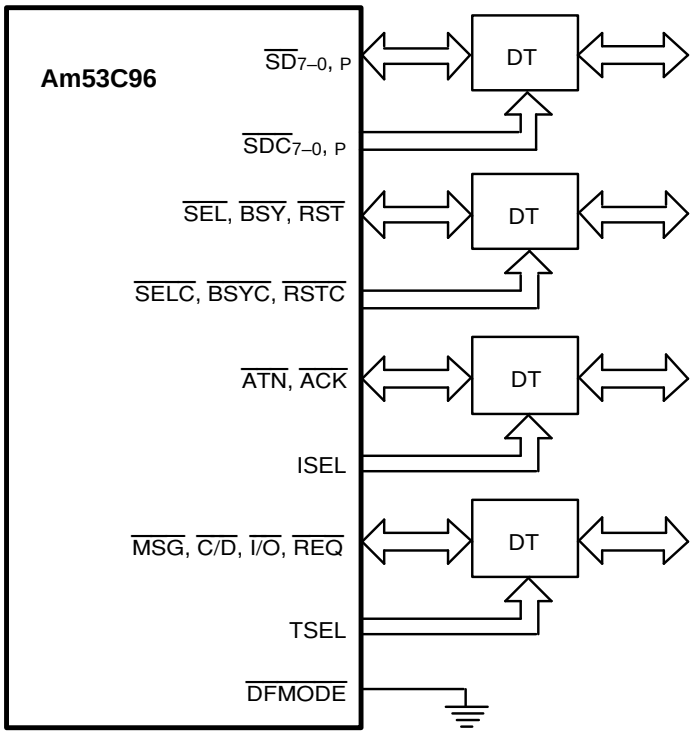

Am53C96 Differential SCSI Bus Configuration

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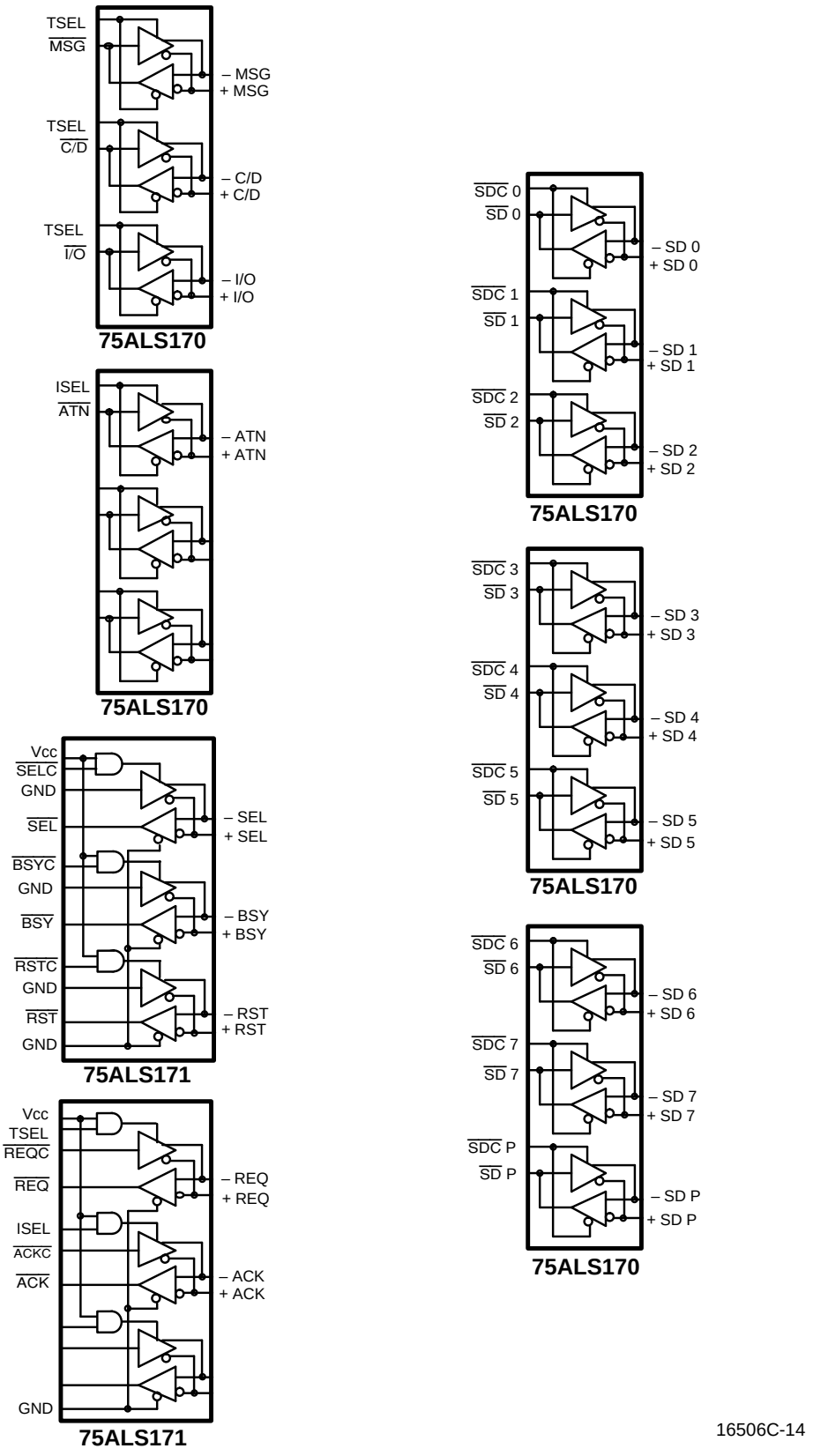
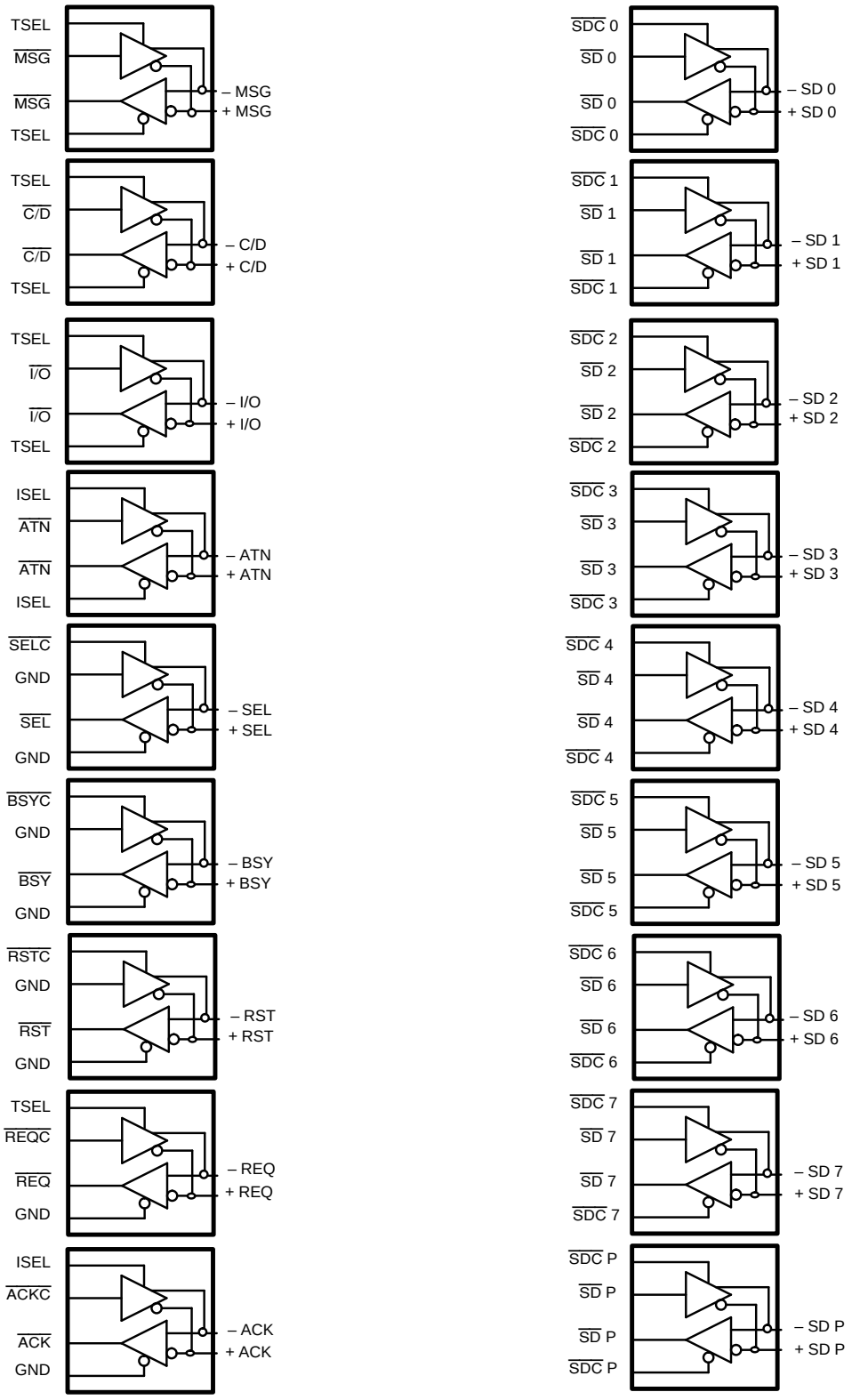


Differential Transceiver Connections for the Differential SCSI Bus Configuration Using 75ALS170 and 75ALS171 Transceivers



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Differential Transceiver Connections for the Differential SCSI Bus Configuration Using 75176A Transceiver

PIN DESCRIPTION

Host Interface Signals

DMA 15–0

Data/DMA Bus
(Input/Output, Active High, Internal Pull-up)

The configuration of this bus depends on the Bus Mode 1–0 (BUSMD 1–0) inputs. When the device is configured for a single bus operation, the host can access the internal register set on the lower eight lines and the DMA accesses can be made to the FIFO using entire bus. When using the Byte Mode via the BHE and A0 inputs the data can be transferred on either the upper or lower half of the DMA 15–0 bus.

DMAP 1–0

Data/DMA Parity Bus
(Input/Output, Active High, Internal Pull-up)

These lines are odd parity for the DMA 15–0 bus. DMAP 1 is the parity for the upper half of the bus DMA 15–8 and DMAP 0 is the parity for the lower half of the bus DMA 7–0.

ALE [A3]

Address Latch Enable [Address 3]
(Input, Active High)

This is a dual function input. When the device is configured for the dual bus mode (two buses, multiplexed and byte control), this input acts as ALE. As ALE, this input latches the address on the AD 7–0 bus on its Low going edge. When the device is configured for all other bus modes, this input acts as A3. As A3, this input is the third bit of the address bus.

$\overline{\text{DMARD}}$ [A2]

DMA Read [Address 2]
(Input, Active Low [Active High])

This is a dual function input. When the device is configured for the dual bus mode (two buses, multiplexed and byte control), this input acts as $\overline{\text{DMARD}}$. As $\overline{\text{DMARD}}$, this input is the read signal for the DMA 15–0 bus. When the device is configured for all other bus modes, this input acts as A2. As A2, this input is the second bit of the address bus.

BHE [A1]

Bus High Enable [Address 1]
(Input, Active High)

This is a dual function input. When the device is configured for the dual bus mode (two buses, multiplexed and byte control), this input acts as BHE. As BHE, this input works in conjunction with AS0 to indicate the lines on which data transfer will take place. When the device is configured for all other bus modes this input acts as A1. As A1, this input is the first bit of the address bus.

AS0 [A0]

Address Status [Address 0]
(Input, Active High)

This is a dual function input. When the device is configured for the dual bus mode (two buses, multiplexed and byte control), this input acts as AS0. As AS0, this input works in conjunction with BHE to indicate the lines on which data transfer will take place. When the device is configured for all other bus modes, this input acts as A0. As A0, this input is the zeroth bit of the address bus.

The following is the decoding for the BHE and AS0 inputs:

BHE	AS0	Bus Used
1	1	Upper Bus – DMA 15–8, DMAP 1
1	0	Full Bus – DMA 15–0, DMAP 1–0
0	1	Reserved
0	0	Lower Bus – DMA 7–0, DMAP 0

DREQ

DMA Request
(Output, Active High, Hi-Z)

This output signal to the DMA controller will be active during DMA read and write cycles. During a DMA read cycle it will be active as long as there is a word (or a byte in the byte mode) in the FIFO to be transferred to memory. During a DMA write cycle it will be active as long as there is an empty space for a word (or a byte in the byte mode) in the FIFO.

$\overline{\text{DACK}}$

DMA Acknowledge
(Input, Active Low)

This input signal from the DMA controller will be active during DMA read and write cycles. The $\overline{\text{DACK}}$ signal is used to access the DMA FIFO only and should never be active simultaneously with the $\overline{\text{CS}}$ signal, which accesses the registers only.

AD 7–0

Host Address Data Bus
(Input/Output, Active High, Internal Pull-up)

This bus is used only in the dual bus mode. This bus allows the host processor to access the device's internal registers while the DMA bus is transferring data. When using multiplexed bus, these lines can be used for address and data. When using non multiplexed bus these lines can be used for the data only.

DMAWR

DMA Write
(Input, Active Low)

This signal writes the data on the DMA 15–0 bus into the internal FIFO when DACK is also active. When in the single bus mode this signal must be tied to the WR signal.

RD

Read
(Input Active Low)

This signal reads the internal device registers and places their contents on the data bus, when either CS signal or DACK signal is active.

WR

Write
(Input Active Low)

This signal writes the internal device registers with the value present on the data bus, when the CS signal is also active.

CS

Chip Select
(Input Active Low)

This signal enables the read and write of the device registers. CS enables access to any register (including the FIFO) while the DACK enables access only to the FIFO. CS and DACK should never be active simultaneously in the single bus mode, they may however be active simultaneously in the dual bus mode provided the CS signal is not enabling access to the FIFO.

INT

Interrupt
(Output, Active Low, Open Drain)

This signal is a non maskable interrupt flag to the host processor. This signal is latched on the output on the high going edge of the clock. This flag may be cleared by reading the Interrupt Status Register (ISTAT) or by performing a device reset (hard or soft). This flag is not cleared by a SCSI reset.

DFMODE

Differential Mode
(Input, Active Low)

This input is available only on the Am53C96. This input configures the SCSI bus to either single ended or differential mode. When this input is active, the device operates in the differential SCSI mode. The SCSI data is available on the SD 7–0 lines and the high active transceiver enables on the SDC 7–0 outputs. When this input is inactive, the device operates in the single ended SCSI mode. The SCSI input data is available on SD 7–0 lines and the output data is available on SDC 7–0 lines. In the single ended SCSI mode, the SD 7–0 and the SDC 7–0 buses can be tied together externally.

BUSMD 1–0

Bus Mode
(Input, Active High)

These inputs configure the device for single bus or dual bus operation and the DMA width.

BUSMD1	BUSMD0	Bus Configuration
1	1	Two buses: 8-bit Host Bus and 16-bit DMA Bus Register Address on A 3–0 and Data on AD Bus
1	0	Two buses: Multiplexed and byte control Register Address on AD 3–0 and Data on AD Bus
0	1	Single bus: 8-bit Host Bus and 16-bit DMA Bus Register Address on A 3–0 and Data on DMA Bus
0	0	Single bus: 8-bit Host Bus and 8-bit DMA Bus Register Address on A 3–0 and Data on DMA Bus

CLK

Clock
(Input)

Clock input used to generate all the internal device timings. The maximum frequency of this input is 25 MHz. and a minimum of 10 MHz to maintain the SCSI bus timings.

RESET

Reset
(Input, Active High)

This input when active resets the device. The RESET input must be active for at least two CLK periods after the voltage on the power inputs have reached Vcc minimum.

SCSI Interface Signals

SD 7–0

SCSI Data
(Input/Output, Active Low, Schmitt Trigger)

When the device is configured in the Single Ended SCSI Mode (DFMODE inactive) these pins are defined as inputs for the SCSI data bus. When the device is configured in the Differential SCSI Mode (DFMODE active) these pins are defined as bidirectional SCSI data bus.

$\overline{SD}_P$

SCSI Data Parity
(Input/Output, Active Low, Schmitt Trigger)

When the device is configured in the Single Ended SCSI Mode ($\overline{DFMODE}$ inactive) this pin is defined as the input for the SCSI data parity. When the device is configured in the Differential SCSI Mode ($\overline{DFMODE}$ active) this pin is defined as bidirectional SCSI data parity.

$\overline{SDC}$ 7–0

SCSI Data Control
(Output, Active Low, Open Drain)

When the device is configured in the Single Ended SCSI Mode ($\overline{DFMODE}$ inactive) these pins are defined as outputs for the SCSI data bus. When the device is configured in the Differential SCSI Mode ($\overline{DFMODE}$ active) these pins are defined as direction controls for the external differential transceivers. In this mode, a signal high state corresponds to an output to the SCSI bus and a low state corresponds to an input from the SCSI bus.

$\overline{SDC}_P$

SCSI Data Control Parity
(Output, Active Low, Open Drain)

When the device is configured in the Single Ended SCSI Mode ($\overline{DFMODE}$ inactive) this pin is defined as an output for the SCSI data parity. When the device is configured in the Differential SCSI Mode ($\overline{DFMODE}$ active) this pin is defined as the direction control for the external differential transceiver. In this mode, a signal high state corresponds to an output to the SCSI bus and a low state corresponds to an input from the SCSI bus.

$\overline{MSG}$

Message
(Input/Output, Active Low, Schmitt Trigger)

This is a bidirectional signal with 48 mA output driver. It is an output in the target mode and a Schmitt trigger input in the initiator mode.

$\overline{C/D}$

Command/Data
(Input/Output, Schmitt Trigger)

This is a bidirectional signal with 48 mA output driver. It is an output in the target mode and a Schmitt trigger input in the initiator mode.

$\overline{I/O}$

Input/Output
(Input/Output, Schmitt Trigger)

This is a bidirectional signal with 48 mA output driver. It is an output in the target mode and a Schmitt trigger input in the initiator mode.

$\overline{ATN}$

Attention
(Input/Output, Active Low, Schmitt Trigger)

This signal is a 48 mA output in the initiator mode and a Schmitt trigger input in the target mode. This signal will be asserted when the initiator detects a parity error or it can be asserted via certain initiator commands.

$\overline{BSY}$

Busy
(Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{SEL}$

Select
(Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{RST}$

Reset
(Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{REQ}$

Request
(Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{ACK}$

Acknowledge
(Input, Active Low, Schmitt Trigger)

This is a SCSI input signal with a Schmitt trigger.

$\overline{BSYC}$

Busy Control
(Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. When the device is configured in the Single Ended SCSI Mode ($\overline{DFMODE}$ inactive) this pin is defined as a BSY output for the SCSI bus. When the device is configured in the Differential SCSI Mode ($\overline{DFMODE}$ active) this pin is defined as the direction control for the external differential transceiver. In this mode, a signal high state corresponds to an output to the SCSI bus and a low state corresponds to an input from the SCSI bus.

SELC

Select Control
(Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. When the device is configured in the Single Ended SCSI Mode (DFMODE inactive) this pin is defined as a SEL output for the SCSI bus. When the device is configured in the Differential SCSI Mode (DFMODE active) this pin is defined as the direction control for the external differential transceiver. In this mode, a signal high state corresponds to an output to the SCSI bus and a low state corresponds to an input from the SCSI bus.

RSTC

Reset Control
(Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. The Reset SCSI command will cause the device to drive RSTC active for 25 ms–40 ms, which will depend on the CLK frequency and the conversion factor. When the device is configured in the Single Ended SCSI Mode (DFMODE inactive) this pin is defined as a RST output for the SCSI bus. When the device is configured in the Differential SCSI Mode (DFMODE active) this pin is defined as the direction control for the external differential transceiver. In this mode, a signal high state corresponds to an output to the SCSI bus and a low state corresponds to an input from the SCSI bus.

REQC

Request Control
(Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. This signal is activated only in the target mode.

ACKC

Acknowledge Control
(Output, Active Low, Open Drain)

This is a SCSI output with 48 mA drive. This signal is activated only in the initiator mode.

ISEL

Initiator Select
(Output, Active High)

This signal is available on the Am53C96 only. This signal is active whenever the device is in the initiator mode. In the differential mode this signal is used to enable the initiator signals ACKC and ATN and the device also drives these signals.

TSEL

Target Select
(Output, Active High)

This signal is available on the Am53C96 only. This signal is active whenever the device is in the target mode. In the differential mode this signal is used to enable the target signals REQC, MSG, C/D and I/O and the device also drives these signals.

FUNCTIONAL DESCRIPTION

Register Map

Address (Hex.)	Operation	Register	Address (Hex.)	Operation	Register
00	Read	Current Transfer Count Register LSB	06	Read	Internal State Register
00	Write	Start Transfer Count Register LSB	06	Write	Synchronous Transfer Period Register
01	Read	Current Transfer Count Register MSB	07	Read	Current FIFO/Internal State Register
01	Write	Start Transfer Count Register MSB	07	Write	Synchronous Offset Register
			08	Read/Write	Control Register 1
02	Read/Write	FIFO Register	09	Write	Clock Factor Register
03	Read/Write	Command Register	0A	Write	Forced Test Mode Register
04	Read	Status Register	0B	Read/Write	Control Register 2
04	Write	SCSI Destination ID Register	0C	Read/Write	Control Register 3
05	Read	Interrupt Status Register			
05	Write	SCSI Timeout Register	0F	Write	Data Alignment Register

Note:

Not all registers in this device are both readable and writable. Some read only registers share the same address with write only registers. The registers can be accessed by asserting the CS signal and then asserting either RD or WR signal depending on the operation to be performed. Only the FIFO Register can be accessed by asserting either CS or DACK in conjunction with RD and WR signals or DMARD and DMAWR signals. The register address inputs are ignored when DACK is used but must be valid when CS is used.

Current Transfer Count Register (00H–01H) Read Only

Current Transfer Count Register
CTCREG

Address: 00H–01H
Type: Read

15	14	13	12	11	10	9	8
CRVL15	CRVL14	CRVL13	CRVL12	CRVL11	CRVL10	CRVL9	CRVL8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
CRVL7	CRVL6	CRVL5	CRVL4	CRVL3	CRVL2	CRVL1	CRVL0
x	x	x	x	x	x	x	x

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CTCREG – Bits 15:0 – CRVL 15:0 – Current Value 15:0

This is a two-byte register. It counts down to keep track of the number of DMA transfers. Reading this registers will return the current value of the counter. The counter will decrement by one for every byte transferred and two for every word transferred over the SCSI bus. The transaction is complete when the count reaches zero. These registers are automatically loaded with the values in the Start Transfer Count Register every time a DMA command is issued.

In the target mode, this counter is decremented by the active edge of $\overline{\text{DACK}}$ during the Data-In phase and by $\overline{\text{REQC}}$ during the Data-Out phase.

In the initiator mode, the counter is decremented by the active edge of $\overline{\text{DACK}}$ during the Synchronous Data-In phase or by $\overline{\text{ACKC}}$ during the Asynchronous Data-In phase and by $\overline{\text{DACK}}$ during the Data-Out phase.

Start Transfer Count Register (00H–01H) Write Only

Start Transfer Count Register
STCREG

Address: 00H–01H
Type: Write

15	14	13	12	11	10	9	8
STVL15	STVL14	STVL13	STVL12	STVL11	STVL10	STVL9	STVL8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
STVL7	STVL6	STVL5	STVL4	STVL3	STVL2	STVL1	STVL0
x	x	x	x	x	x	x	x

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STCREG – Bits 15:0 – STVL 15:0 – Start Value 15:0

This is a two-byte register. It contains the number of bytes to be transferred during a DMA operation. The value of this register is set to the number of bytes to be transferred prior to a DMA transfer command. This register retains its programmed value until it is overwritten and is not affected by hardware or software reset. Therefore, it is not necessary to reprogram the count for subsequent DMA transfers of the same size. Writing a zero to this register sets a maximum transfer count of 65536 bytes. The value in this register is undefined at power-up.

FIFO Register (02H) Read/Write

FIFO Register
FFREG

Address: 02H
Type: Read/Write

7	6	5	4	3	2	1	0
FF7	FF6	FF5	FF4	FF3	FF2	FF1	FF0
0	0	0	0	0	0	0	0

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FFREG – Bits 7:0 – FF 7:0 – FIFO 7:0

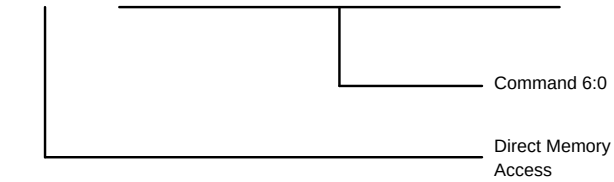
The bottom of the 16x9 FIFO is mapped into the FIFO Register address. By reading and writing this register the bottom of the FIFO can be read or written. This is the only register that can also be accessed by $\overline{\text{DACK}}$ along with $\overline{\text{DMARD}}$ or $\overline{\text{DMAWR}}$. This register is reset to zero by hardware or software reset and also at the start of a selection or reselection sequence.

Command Register (03H) Read/Write

Command Register
CMDREG

Address: 03H
Type: Read/Write

7	6	5	4	3	2	1	0
DMA	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0
x	x	x	x	x	x	x	x



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Commands to the device are issued by writing to this register. This register is two deep which allows for command queuing. The second command can be issued before the first one is completed. The Reset command and the Stop DMA command are not queued and are executed immediately. Reading this register will return the command currently being executed (or the last command executed if there are no pending commands).

CMDREG – Bit 7 – DMA – Direct Memory Access

The DMA bit when set notifies the device that the command is a DMA instruction, when reset it is a non-DMA instruction. For DMA instructions the Current Transfer Count Register (CTCREG) will be loaded with the contents of the Start Transfer Count Register (STCREG). The data is then transferred and the CTCREG is decremented for each byte until it reaches zero.

CMDREG – Bits 6:0 – CMD 6:0 – Command 6:0

These command bits decode the commands that the device needs to perform. There are a total of 29 commands grouped into four categories. The groups are Initiator Commands, Target Commands, Selection/Reselection Commands and General Purpose Commands.

Initiator Commands

CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Command
0	0	1	0	0	0	0	Information Transfer
0	0	1	0	0	0	1	Initiator Command Complete Steps
0	0	1	0	0	1	0	Message Accepted
0	0	1	1	0	0	0	Transfer Pad Bytes
0	0	1	1	0	1	0	Set ATN
0	0	1	1	0	1	1	Reset ATN

Target Commands

CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Command
0	1	0	0	0	0	0	Send Message
0	1	0	0	0	0	1	Send Status
0	1	0	0	0	1	0	Send Data
0	1	0	0	0	1	1	Disconnect Steps
0	1	0	0	1	0	0	Terminate Steps
0	1	0	0	1	0	1	Target Command Complete Steps
0	1	0	0	1	1	1	Disconnect
0	1	0	1	0	0	0	Receive Message Steps
0	1	0	1	0	0	1	Receive Command
0	1	0	1	0	1	0	Receive Data
0	1	0	1	0	1	1	Receive Command Steps
0	0	0	0	1	0	0	DMA Stop

Idle Commands

CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Command
1	0	0	0	0	0	0	Reselect Steps
1	0	0	0	0	0	1	Select without ATN Steps
1	0	0	0	0	1	0	Select with ATN Steps
1	0	0	0	0	1	1	Select with ATN and Stop Steps
1	0	0	0	1	0	0	Enable Selection/Reselection
1	0	0	0	1	0	1	Disable Selection/Reselection
1	0	0	0	1	1	0	Select with ATN3 Steps

General Commands

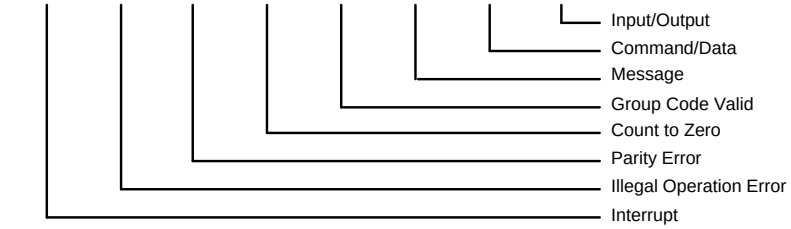
CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Command
0	0	0	0	0	0	0	No Operation
0	0	0	0	0	0	1	Clear FIFO
0	0	0	0	0	1	0	Reset Device
0	0	0	0	0	1	1	Reset SCSI Bus

Status Register (04H) Read

Status Register
STATREG

Address: 04H
Type: Read

7	6	5	4	3	2	1	0
INT	IOE	PE	CTZ	GCV	MSG	C/D	I/O
0	0	0	0	0	x	x	x



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This read only register contains flags to indicate the status and phase of the SCSI transactions. It indicates whether an interrupt or error condition exists. It should be read every time the host is interrupted to determine which device is asserting an interrupt. The data is latched until the Interrupt Status Register is read. The phase bits will be latched only if latching is enabled in the Control Register 2, otherwise, it will indicate the current SCSI phase. If command stacking is used, two interrupts might occur. Reading this register will clear the status information for the first interrupt and update the Status Register for the second interrupt.

STATREG – Bit 7 – INT – Interrupt

The INT bit is set when the device asserts the interrupt output. This bit will be cleared by a hardware or software reset. Reading the Interrupt Status Register will deassert the interrupt output and also clear this bit.

STATREG – Bit 6 – IOE – Illegal Operation Error

The IOE bit is set when an illegal operation is attempted. This condition will not cause an interrupt, it will be detected by reading the status register while servicing another interrupt. The following conditions will cause the IOE bit to be set:

- DMA and SCSI transfer directions are opposite.
- FIFO overflows.
- In initiator mode an unexpected phase change detected during synchronous data transfer.
- Command Register overwritten.

This bit will be cleared by reading the Interrupt Status Register or by a hard or soft reset.

STATREG – Bit 5 – PE – Parity Error

The PE bit is set if the parity checking option is enabled in Control Register 1 and the device detects a parity error on incoming SCSI data, command, status or message bytes. Detection of a parity error condition will not cause an interrupt but will be reported with other interrupt causing conditions. When a parity error is detected in the information phase of the initiator mode $\overline{ATN}$ is asserted on the SCSI bus.

This bit will be cleared by reading the Interrupt Status Register or by a hard or soft reset.

STATREG – Bit 4 – CTZ – Count To Zero

The CTZ bit is set when the Current Transfer Count Register (CTCREG) has counted down to zero. This bit will be reset when the CTCREG is written.

Reading the Interrupt Status Register will not affect this bit. This bit will however be cleared by a hard or soft reset.

Note:

A non-DMA NOP will not reset the CTZ bit since it does not load the CTCREG but a DMA NOP will reset this bit since it loads the CTCREG.

STATREG – Bit 3 – GCV – Group Code Valid

The GCV bit is set if the group code field in the Command Descriptor Block (CDB) is one that is defined by the ANSI Committee in their document X3.131 – 1986. If the SCSI-2 Feature Enable (S2FE) bit in the Control Register 2 (CNTLREG2) is set, Group 2 commands will be treated as ten byte commands and the GCV bit will be set. If S2FE is reset then Group 2 commands will be treated as reserved commands. Group 3 and 4 command will always be considered as reserved commands. The device will treat all reserved commands as six byte commands. Group 6 commands will always be treated as vendor unique six byte commands and Group 7 commands will always be treated as vendor unique ten byte commands.

The GCV bit is cleared by reading the Interrupt Status Register (INSTREG) or by a hard or soft reset.

STATREG – Bit 2 – MSG – Message

STATREG – Bit 1 – C/D – Command/Data

STATREG – Bit 0 – I/O – Input/Output

Bit2 MSG	Bit1 C/D	Bit0 I/O	SCSI Phase
1	1	1	Message In
1	1	0	Message Out
1	0	1	Reserved
1	0	0	Reserved
0	1	1	Status
0	1	0	Command
0	0	1	Data_In
0	0	0	Data_Out

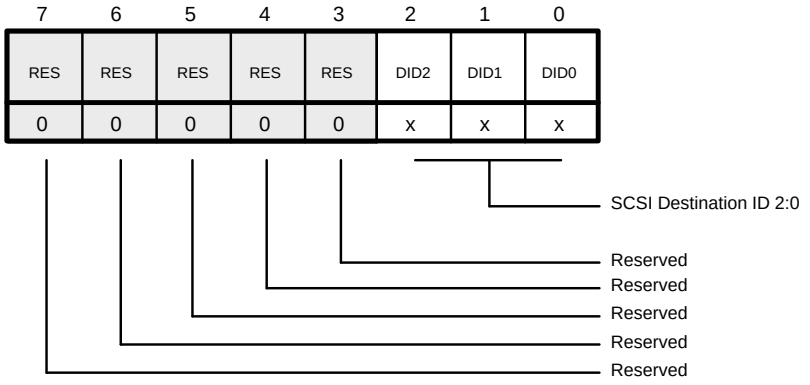
The MSG, C/D and I/O bits together can be referred to as the SCSI Phase bits. They indicate the phase of the SCSI bus. These bits may be latched or unlatched depending on the option selected in Control Register 2 (CNTLREG2) by the Latch SCSI Phase (LSP) bit.

In the latched mode the SCSI phase bits are latched at the end of a command and the latch is opened when the Interrupt Status Register (INSTREG) is read. In the unlatched mode, they indicate the phase of the SCSI bus when this register is read.

SCSI Destination ID Register (04H) Write

SCSI Destination ID Register
SDIDREG

Address: 04H
Type: Write



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SDIDREG – Bits 7:3 – RES – Reserved

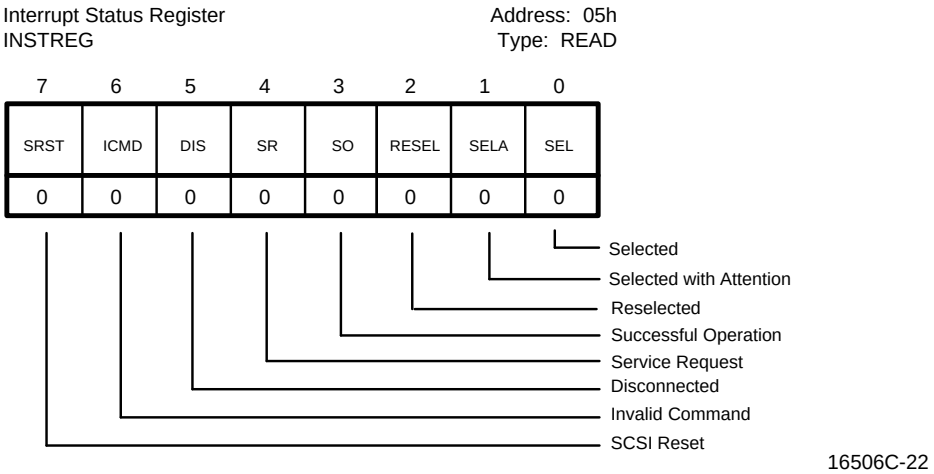
SDIDREG – Bits 2:0 – DID 2:0 – Destination ID 2:0

The DID 2:0 bits are the encoded SCSI ID of the device on the SCSI bus which needs to be selected or reselected.

At power-up the state of these bits is undefined. The DID 2:0 bits are not affected by reset.

DID2	DID1	DID0	SCSI ID
1	1	1	7
1	1	0	6
1	0	1	5
1	0	0	4
0	1	1	3
0	1	0	2
0	0	1	1
0	0	0	0

Interrupt Status Register (05H) Read



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The Interrupt Status Register (INSTREG) will indicate the reason for the interrupt. This register is used with the Status Register (STATREG) and Internal Status Register (ISREG) to determine the reason for the interrupt. Reading the INSTREG will clear all three registers.

INSTREG – Bit 7 – SRST – SCSI Reset

The SRST bit will be set if a SCSI Reset is detected and SCSI reset reporting is enabled via the DISR (bit 6) of the CNTLREG1.

INSTREG – Bit 6 – ICMD – Invalid Command

The ICMD bit will be set if the device detects an illegal command code. This bit is also set if a command code from a different mode is detected than the mode the device is currently in.

INSTREG – Bit 5 – DIS – Disconnected

The DIS bit can be set in the target or the initiator mode when the device disconnects from the SCSI bus. In the target mode this bit will be set if a terminate or a command complete sequence causes the device to disconnect from the SCSI bus. In the Initiator mode this bit will be set if the target disconnects or a selection or reselection timeout occurs.

INSTREG – Bit 4 – SR – Service Request

The SR bit can be set in the target or the initiator mode when another device on the SCSI bus has a service request. In the target mode this bit will be set when the initiator asserts the $\overline{\text{ATN}}$ signal. In the Initiator mode this bit is set whenever the target requests an information transfer phase.

INSTREG – Bit 3 – SO – Successful Operation

The SO bit can be set in the target or the initiator mode when an operation is successfully complete. In the target mode this bit will be set when any target mode command is completed. In the initiator mode this bit is set after a target has been successfully selected, after a command is successfully completed and after an information transfer command when the target requests a message in phase.

INSTREG – Bit 2 – RESEL – Reselected

The RESEL bit is set at the end of the reselection phase indicating that the device has been reselected as an initiator.

INSTREG – Bit 1 – SELA – Selected with Attention

The SELA bit is set at the end of the selection phase indicating that the device has been selected and that the $\overline{\text{ATN}}$ signal was active during the selection.

INSTREG – Bit 0 – SEL – Selected

The SEL bit is set at the end of the selection phase indicating that the device has been selected and that the $\overline{\text{ATN}}$ signal was inactive during the selection.

SCSI Timeout Register (05H) Write

SCSI Timeout Register
STIMREG

Address: 05H
Type: Write

7	6	5	4	3	2	1	0
STIM7	STIM6	STIM5	STIM4	STIM3	STIM2	STIM1	STIM0
x	x	x	x	x	x	x	x

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This register determines how long the initiator (target) will wait for a target to respond to a selection (reselection) before timing out. It should be set to yield 250 ms to comply with ANSI standards for SCSI.

STIMREG – Bits 7:0 – STIM 7:0 – SCSI Timer 7:0

The value loaded in STIM 7:0 can be calculated from the following formula:

STIM 7:0 =

[(SCSI Time Out) (Clock Frequency) / (8192 (Clock Factor))]

Example:

SCSI Time Out (in seconds): 250 ms. (Recommended by the ANSI Standard) = 250 x 10^{-3} s.

Clock Frequency: 20 MHz. (assume) = 20 x 10^{6} Hz.

Clock Factor: CLKF 2:0 from Clock Conversion Register (09H) = 5

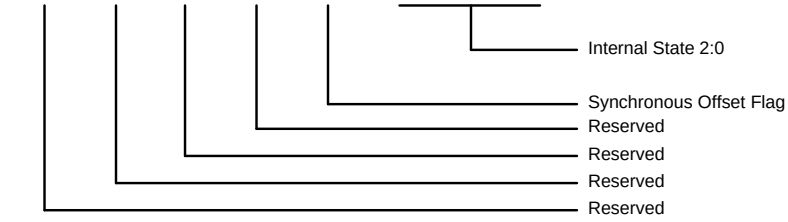
STIM 7:0 = (250 x 10^{-3}) X (20 x 10^{6}) / (8192 (5)) = 122 decimal

Internal State Register (06H) Read

Internal State Register
ISREG

Address: 06H
Type: Read

7	6	5	4	3	2	1	0
RES	RES	RES	RES	$\overline{SOF}$	IS2	IS1	IS0
x	x	x	x	0	0	0	0



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The Internal State Register (ISREG) tracks the progress of a sequence-type command. It is updated after each successful completion of an intermediate operation. If an error occurs, the host can read this register to determined at where the command failed and take the necessary procedure for recovery. Reading the Interrupt Status Register will clear this register.

ISREG – Bits 7:4 – RES – Reserved

ISREG – Bit 3 – $\overline{SOF}$ – Synchronous Offset Flag

The SOF is reset when the Synchronous Offset Register (SOFREG) has reached its maximum value.

Note:

The SOF bit is active Low.

ISREG – Bits 2:0 – IS 2:0 – Internal State 2:0

The IS 2:0 bits along with the Interrupt Status Register (INSTREG) indicates the status of the successfully completed intermediate operation. Refer to the Status Decode section for more details.

Initiator Select without ATN Steps

Internal State Register (06H) Bits 2:0 (Hex)	Interrupt Status Register (05H) Bits 7:0 (Hex)	Explanation
0	20	Arbitration steps completed or disconnected or selection time–out
4	18	Selection with ATN steps fully executed
3	18	Sequence halted during command transfer due to premature phase change (target)
2	18	Arbitration and selection completed; sequence halted because target failed to assert command phase

Initiator Select with ATN Steps

Internal State Register (06H) Bits 2:0 (Hex)	Interrupt Status Register (05H) Bits 7:0 (Hex)	Explanation
4	18	Selection with ATN steps fully executed
3	18	Sequence halted during command transfer due to premature phase change; some CDB bytes may not have been sent; check FIFO flags
2	18	Message out completed; sent one message byte with ATN true, then released ATN; sequence halted because target failed to assert command phase after message byte was sent
0	18	Arbitration and selection completed; sequence halted because target did not assert message out phase; ATN still driven by HPSC

Initiator Select with ATN3 Steps

Internal State Register (06H) Bits 2:0 (Hex)	Interrupt Status Register (05H) Bits 7:0 (Hex)	Explanation
0	20	Arbitration steps completed or disconnected or selection time–out
4	18	Selection with ATN3 steps fully executed
3	18	Sequence halted during command transfer due to premature phase change; some CDB bytes may not have been sent; check FIFO flags
2	18	One, two, or three message bytes sent; sequence halted because target failed to assert command phase after third message byte, or prematurely released message out phase; ATN released only if third message byte was sent
0	18	Arbitration and selection completed; sequence halted because target failed to assert message out phase; ATN still driven by HPSC

Initiator Select with ATN and Stop Steps

Internal State Register (06H) Bits 2:0 (Hex)	Interrupt Status Register (05H) Bits 7:0 (Hex)	Explanation
0	20	Arbitration steps completed or disconnected or selection time–out
0	18	Arbitration and selection completed; sequence halted because target failed to assert message out phase; ATN still asserted by HPSC
1	18	Message out completed; one message byte sent; ATN on

Target Selected without ATN Steps

Internal State Register (06H) Bits 2:0 (Hex)	Interrupt Status Register (05H) Bits 7:0 (Hex)	Explanation
2	11	Selected; received entire CDB; check group code valid bit; initiator asserted ATN in command phase
1	11	Sequence halted in command phase due to parity error; some CDB bytes may not have been received; check FIFO flags; initiator asserted ATN in command phase
2	01	Selected; received entire CDB; check group code valid bit
1	01	Sequence halted in command phase because of parity error; some CDB bytes may not have been received; check FIFO flags
0	01	Selected; loaded bus ID into FIFO; null–byte message loaded into FIFO

Target Select with ATN Steps, SCSI–2 Bit NOT SET

Internal State Register (06H) Bits 2:0 (Hex)	Interrupt Status Register (05H) Bits 7:0 (Hex)	Explanation
2	12	Selection complete; received one message byte and entire CDB; initiator asserted ATN during command phase
1	12	Halted in command phase; parity error and ATN true
0	12	Selected with ATN; stored bus ID and one message byte; sequence halted because ATN remained true after first message byte
2	02	Selection completed; received one message byte and the entire CDB
1	02	Sequence halted in command phase because of parity error; some CDB bytes not received; check group code valid bit and FIFO flags
0	02	Selected with ATN; stored bus ID and one message byte; sequence halted because of parity error or invalid ID message

Target Select with ATN Steps, SCSI–2 Bit SET

Internal State Register (06H) Bits 2:0 (Hex)	Interrupt Status Register (05H) Bits 7:0 (Hex)	Explanation
5	12	Halted in command phase; parity error and ATN true
4	12	ATN remained true after third message byte
0	02	Selected with ATN; stored bus ID and one message byte; sequence halted because of parity error or invalid ID message
6	02	Selection completed; received three message bytes and the entire CDB
5	02	Received three message bytes then halted in command phase because of parity error; some CDB bytes not received; check group code valid bit and FIFO flags
402	Parity error during second or third message byte	

Target Receive Command Steps

Internal State Register (06H) Bits 2:0 (Hex)	Interrupt Status Register (05H) Bits 7:0 (Hex)	Explanation
2	18	Received entire CDB; initiator asserted ATN
1	18	Sequence halted during command transfer due to parity error; ATN asserted by initiator
2	08	Received entire CDB
1	08	Sequence halted during command transfer due to parity error; check FIFO flags

Target Disconnect Steps

Internal State Register (06H) Bits 2:0 (Hex)	Interrupt Status Register (05H) Bits 7:0 (Hex)	Explanation
2	28	Disconnect steps fully executed; disconnected; bus is free
1	18	Two message bytes sent; sequence halted because initiator asserted ATN
0	18	One message byte sent; sequence halted because initiator asserted ATN

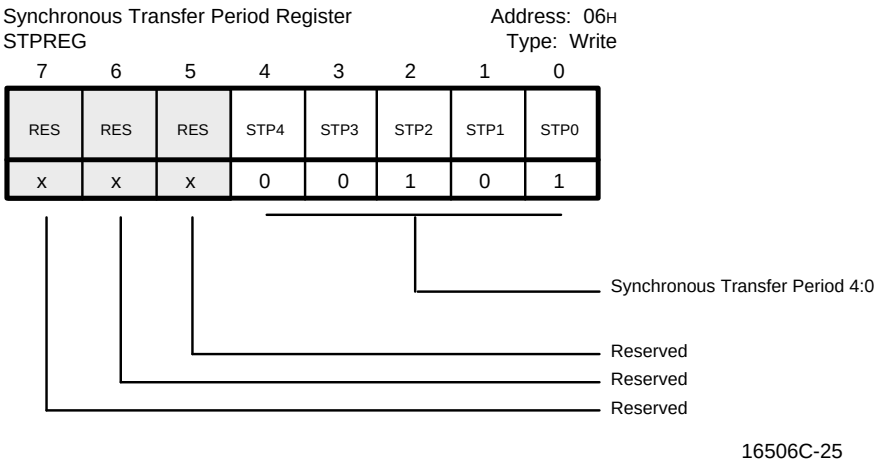
Target Terminate Steps

Internal State Register (06H)	Interrupt Status Register (05H)	Explanation
Bits 2:0 (Hex)	Bits 7:0 (Hex)	
2	28	Terminate steps fully executed; disconnected; bus is free
1	18	Status and message bytes sent; sequence halted because initiator asserted ATN
0	18	Status byte sent; sequence halted because initiator asserted ATN

Target Command Complete Steps

Internal State Register (06H)	Interrupt Status Register (05H)	Explanation
Bits 2:0 (Hex)	Bits 7:0 (Hex)	
1	18	Status and message bytes sent; sequence halted because initiator set ATN
0	18	Status byte sent; sequence halted because initiator set ATN
2	08	Command complete steps fully executed

Synchronous Transfer Period Register (06H) Write



The Synchronous Transfer Period Register (STPREG) contains a 5-bit value indicating the number of clock cycles each byte will take to be transferred over the SCSI bus in synchronous mode. The minimum value allowed is 5. The STPREG defaults to five after a hard or soft reset.

STPREG – Bits 7:5 – RES – Reserved

STPREG – Bits 4:0 – STP 4:0 – Synchronous Transfer Period 4:0

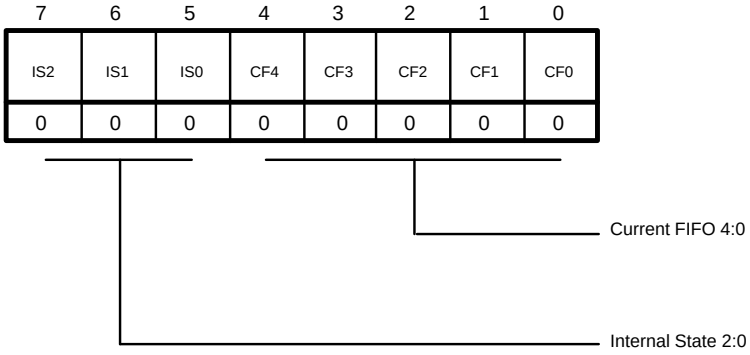
The STP 4:0 bits are programmed to specify the synchronous transfer period or the number of clock cycles for each byte transfer in the synchronous mode. The minimum value for STP 4:0 is five. Missing table entries follow the binary code.

STP4	STP3	STP2	STP1	STP0	Clocks/ Byte
0	0	1	0	0	5
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
•	•	•	•	•	•
•	•	•	•	•	•
1	1	1	1	1	31
0	0	0	0	0	32
0	0	0	0	1	33
0	0	0	1	0	34
0	0	0	1	1	35

Current FIFO/Internal State Register (07H) Read

Current FIFO/Internal State Register
CFISREG

Address: 07H
Type: Read



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This register has two fields, the Current FIFO field and the Internal State field.

CFISREG – Bits 7:5 – IS 2:0 – Internal State 2:0

The Internal State Register (ISREG) tracks the progress of a sequence-type command.

The IS 2:0 bits are duplicated from the IS 2:0 field in the Internal State Register (ISREG) in the normal mode. If the device is in the test mode, IS 0 is set to indicate that the offset value is non zero. A non zero value indicates that synchronous data transfer can continue. A zero value indicates that the synchronous offset count has been reached and no more data can be transferred until an acknowledge is received.

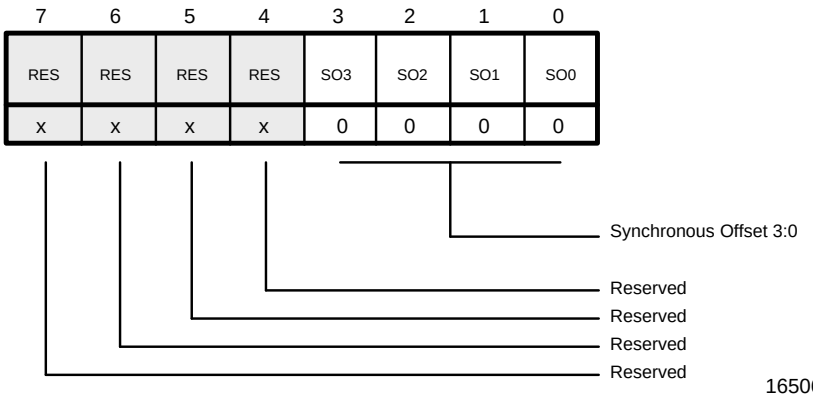
CFISREG – Bits 4:0 – CF 4:0 – Current FIFO 4:0

The CF 4:0 bits are the binary coded value of the number of bytes in the FIFO. These bits should not be read when the device is transferring data since this count may not be stable.

Synchronous Offset Register (07H) Write

Synchronous Offset Register
SOFREG

Address: 07H
Type: Write



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The Synchronous Offset Register (SOFREG) contains a 4-bit count of the number of bytes that can be sent to (or received from) the SCSI bus without an $\overline{ACK}$ (or $\overline{REQ}$). Bytes exceeding the threshold will be sent one byte at a time (asynchronously). That is, each byte will require an $\overline{ACK}$/$\overline{REQ}$ handshake. To set up an asynchronous transfer, the SOFREG is set to zero. The SOFREG is set to zero after a hard or soft reset.

SOFREG – Bits 7:4 – RES – Reserved

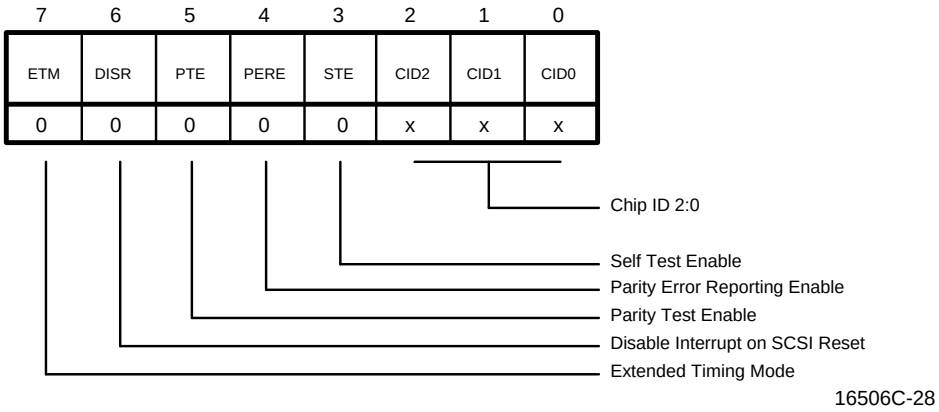
SOFREG – Bits 3:0 – SO 3:0 – Synchronous Offset 3:0

The SO 4:0 bits are the binary coded value of the number of bytes that can be sent to (or received from) the SCSI bus without an $\overline{ACK}$ (or $\overline{REQ}$) signal.

Control Register One (08H) Read/Write

Control Register One
CNTLREG1

Address: 08H
Type: Read/Write



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The Control Register 1 (CNTLREG1) sets up the device with various operating parameters.

CNTLREG1 – Bit 7 – ETM – Extended Timing Mode

The ETM bit is set if an extra clock period is required between the data being driven on the bus and the $\overline{REQ}$ or $\overline{ACK}$ being asserted. This is some times necessary in high capacitive loading environments. The ETM bit is reset to zero by a hard or soft reset.

CNTLREG1 – Bit 6 – DISR – Disable Interrupt on SCSI Reset

The DISR bit masks the reporting of the SCSI reset. When the DISR bit is set and a SCSI reset is asserted, the device will disconnect from the SCSI bus and remain idle without interrupting the host processor. When the DISR bit is reset and a SCSI reset is asserted the device will respond by interrupting the host processor. The DISR bit is reset to zero by a hard or soft reset.

CNTLREG1 – Bit 5 – PTE – Parity Test Enable

The PTE bit is for test use only. When the PTE bit is set the parity on the output (SCSI or host processor) bus is forced to the value of the MSB (bit 7) of the output data from the internal FIFO. This allows parity errors to be created to test the hardware and software. The PTE bit is reset to zero by a hard or soft reset.

CNTLREG1 – Bit 4 – PERE – Parity Error Reporting Enable

The PERE bit enables the checking and reporting of parity errors on incoming SCSI bytes during the information transfer phase. When the PERE bit set and a bad parity is detected, the PE bit in the STATREG is will be set but an interrupt will not be generated. In the initiator mode the $\overline{ATN}$ signal will also be asserted on the SCSI bus. When the PERE bit is reset and a bad parity occurs it is not detected and no action is taken.

CNTLREG1 – Bit 3 – STE – Self Test Enable

The STE bit is for test use only. When the STE bit is set the device is placed in a test mode which enables the device to access the test register at address 0AH. To reset this bit and to resume normal operation the device must be issued a hard or soft reset.

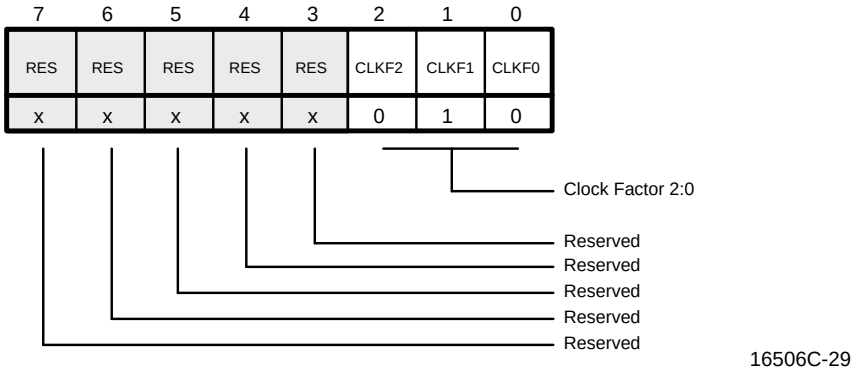
CNTLREG1 – Bit 2:0 – CID 2:0 – Chip ID 2:0

The Chip ID 2:0 bits specify the binary coded value of the device ID on the SCSI bus. The device will arbitrate with this ID and will respond to selection or reselection to this ID. At power-up the state of these bit are undefined. These bits are not affected by hard or soft reset.

Clock Factor Register (09H) Write

Clock Factor Register
CLKFREG

Address: 09H
Type: Write



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The Clock Factor Register (CLKFREG) must be set to indicate the input frequency range of the device. This value is crucial for controlling various timings to meet the SCSI specification. The selector can be calculated by rounding off the quotient of (Input Clock Frequency in MHz)/(5 MHz). The device has a frequency range of 10 to 25 MHz.

CLKF2	CLKF1	CLKF0	Input Clock Frequency in MHz
0	1	0	10
0	1	1	10.01 to 15
1	0	0	15.01 to 20
1	0	1	20.01 to 25

CLKFREG – Bits 7:3 – RES – Reserved

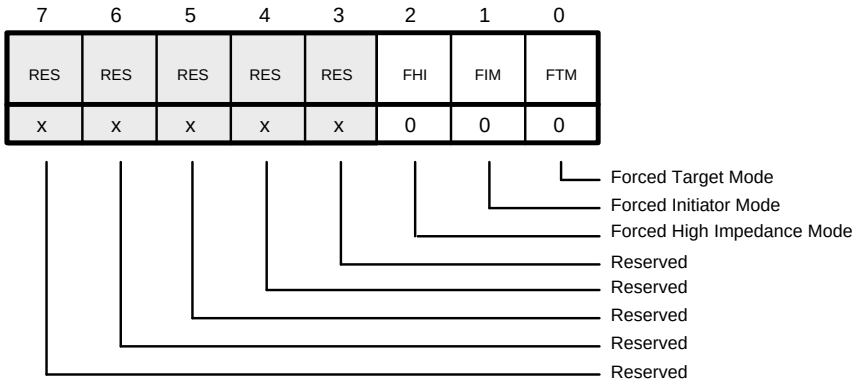
CLKFREG – Bits 2:0 – CLKF 2:0 – Clock Factor 2:0

The CLKF 2:0 bits specify the binary coded value of the clock factor. The CLKF 2:0 bits will default to a value of 2 by a hard or soft reset.

Forced Test Mode Register (0AH) Write

Forced Test Mode Register
FTMREG

Address: 0AH
Type: Write



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The Forced Test Mode Register (FTMREG) is for test use only. The STE bit in the CNTLREG1 must be set for the FTMREG to operate.

FTMREG – Bits 7:3 – RES – Reserved

FTMREG – Bit 2 – FHI – Forced High Impedance Mode

The FHI bit when set places all the output and bidirectional pins into a high impedance state.

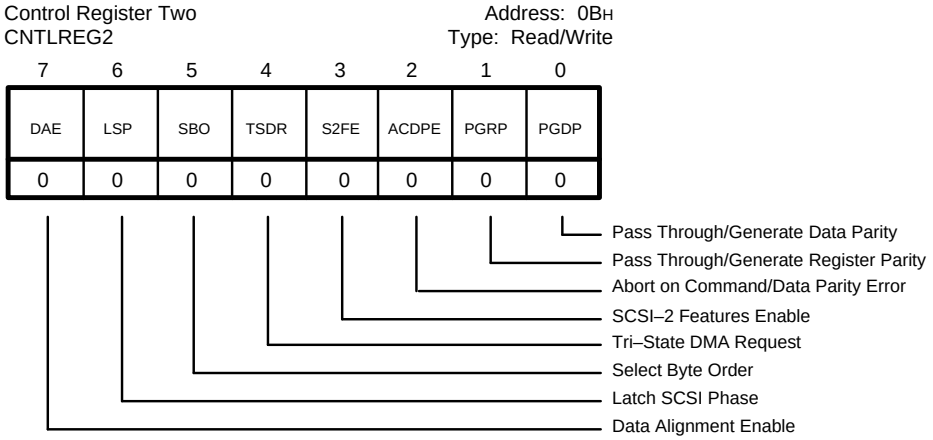
FTMREG – Bit 1 – FIM – Forced Initiator Mode

The FIM bit when set forces the device into the initiator mode. The device will then execute all initiator commands irrespective of the SCSI bus status.

FTMREG – Bit 0 – FTM – Forced Target Mode

The FTM bit when set forces the device into the target mode. The device will then execute all target commands irrespective of the SCSI bus status.

Control Register Two (0BH) Read/Write



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The Control Register 2 (CNTLREG2) sets up the device with various operating parameters.

CNTLREG2 – Bit 7 – DAE – Data Alignment Enable

The DAE bit is used in the initiator Synchronous Data-In phase only. When the DAE bit is set one byte is reserved at the end of the FIFO when the phase changes to the Synchronous Data-In phase. The contents of this byte will become the lower byte of the DMA word (16-bit) transfer to the memory, the upper byte being the first byte of the first word received from the SCSI bus.

Note:

If an interrupt is received for a misaligned boundary on a phase change to synchronous data the following recovery procedure may be followed. The host processor should copy the byte at the start address in the host memory to the Data Alignment Register 0FH (DALREG) and then issue an information transfer command. The first word the device will write to the memory (via DMA) will consists of the lower byte from the DALREG and the upper byte from the first byte received from the SCSI bus.

The DAE bit must be set before the phase changes to the Synchronous Data-In. The DAE bit is reset to zero by a hard or soft reset or by writing the DALREG when interrupted in the Synchronous Data-In phase.

CNTLREG2 – Bit 6 – LSP – Latch SCSI Phase

The LSP bit is used to enable or disable the latching of the SCSI phase bits (MSG, C/D and I/O) in the Status Register (STATREG) 04H.

When the LSP bit is set the phase bits STSTREG – Bits 2:0 are latched at the end of each command. This simplifies software for stacked commands. When the LSP bit is reset the phase bits STATREG – Bits 2:0 reflect the actual state of the SCSI phase lines at any instant of time. The LSP bit is reset by a hard or soft reset.

CNTLREG2 – Bit 5 – SBO – Select Byte Order

The SBO bit is used only when the BUSMD 1:0 = 10 to enable or disable the byte control on the DMA interface. When SBO is set and the BUSMD 1:0 = 10, the byte control inputs BHE and AS0 control the byte positions. When SBO is reset the byte control inputs BHE and AS0 are ignored.

CNTLREG2 – Bit 4 – TSDR – Tri-State DMA Request

The TSDR bit when set sends the DREQ output signal to high impedance state and the device ignores all activity on the DMA request (DREQ) input. This is useful for wiring-OR several devices that share a common DMA request line. When the TSDR bit is reset the DREQ output is driven to TTL levels.

CNTLREG2 – Bit 3 – S2FE – SCSI–2 Features Enable

The S2FE bit allows the device to recognize two SCSI-2 features. The two features are extended message feature and the Group 2 command recognition.

Extended Message Feature: When the S2FE bit is set and the device is selected with attention, the device will monitor the $\overline{ATN}$ signal at the end of the first message byte. If the $\overline{ATN}$ signal is active, the device will request two more message bytes before switching to the command phase. If the $\overline{ATN}$ signal is inactive the device will switch to the command phase. When the S2FE bit is reset the device as a target will request a single message byte. As an initiator, the device will abort the selection sequence if the target does not switch to the command phase after receiving a single message byte.

Group 2 Command Recognition: When the S2FE bit is set the group 2 commands are recognized as 10 byte commands. The GCV (Group Code Valid) bit in the STATREG (04H) is set. When the S2FE bit is reset, the device will interpret the group 2 commands as reserved commands and will request 6 byte commands. The GCV bit in the STATREG will not be set in this case.

CNTLREG2 – Bit 2 – ACDPE – Abort on Command/ Data Parity Error

The ACDPE bit when set allows the device to abort a command or data transfer when a parity error is detected. When the ACDPE bit is reset parity error is ignored.

CNTLREG2 – Bit 1 – PGRP – Pass Through/Generate Register Parity

The PGRP bit when set causes the data along with the parity from the host to pass through to the FIFO under the control of the $\overline{CS}$ and the $\overline{WR}$ signals. When the PGRP bit is reset, the device generates the parity on the data from the host before writing it to the FIFO.

When the device is placing the data on the SCSI bus, it will check for an outgoing parity error if either the PGRP bit is set or the PGDP (Pass Through/Generate Data Parity) bit is set.

CNTLREG2 – Bit 0 – PGDP – Pass Through/Generate Data Parity

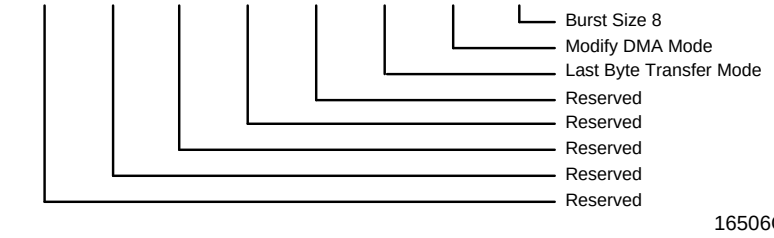
The PGDP bit when set causes the data along with the parity from the host to pass through to the FIFO under the control of the $\overline{DACK}$ and the $\overline{WR}$ signals. When the PGDP bit is reset, the device generates the parity on the data from the host before writing it to the FIFO.

When the device is placing the data on the SCSI bus, it will check for an outgoing parity error if either the PGDP bit is set or the PGRP (Pass Through/Generate Register Parity) bit is set.

Control Register Three (0CH) Read/Write

Control Register Three — Address: 0CH
CNTLREG3 — Type: Read/Write

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	LBTM	MDM	BS8
0	0	0	0	0	0	0	0



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CNTLREG3 – Bits 7:3 – RES – Reserved

CNTLREG3 – Bit 2 – LBTM – Last Byte Transfer Mode

The LBTM bit specifies how the last byte in an odd byte transfer is handled during 16-bit DMA transfers. This mode is not used if byte control is selected via BUSMD 1:0 inputs and BSO (Byte Select Order) bit in the CNTLREG2. This mode has no affect during 8-bit DMA transfers and on transfers on the SCSI bus.

When the LBTM bit is set the DREQ signal will not be asserted for the last byte, instead the host will read or write the last byte from or to the FIFO. When the LBTM bit is reset the DREQ signal will be asserted for the last byte and the following 16-bit DMA transfer will contain the last byte on the lower bus. If the transfer is a DMA read the upper bus will be all ones.

The LBTM bit is reset by hard or soft reset.

CNTLREG3 – Bit 1 – MDM – Modify DMA Mode

The MDM bit is used to modify the timing of the $\overline{DACK}$ signal with respect to the $\overline{DMARD}$ and $\overline{DMAWR}$ signals. The MDM bit is used in conjunction with the Burst Size 8 (BS8) bit in the CNTLREG3. Both bits have to be set for proper operation.

When the MDM bit is set and the device is in a DMA read or write mode the $\overline{DACK}$ signal will remain asserted while the data is strobed by the $\overline{DMARD}$ or $\overline{DMAWR}$ signals. In the DMA read mode when BUSMD 1:0 = 11 the $\overline{DACK}$ signal will toggle for every DMA read.

When the MDM bit is reset and the device is in a DMA read or write mode the $\overline{DACK}$ signal will toggle every time the data is strobed by the $\overline{DMARD}$ or $\overline{DMAWR}$ signals.

CNTLREG3 – Bit 0 – BS8 – Burst Size 8

The BS8 bit is used to modify the timing of the DREQ signal with respect to the $\overline{\text{DMARD}}$ and $\overline{\text{DMAWR}}$ signals. The BS8 bit is used in conjunction with the Modify DMA Mode (MDM) bit in the CNTLREG3. Both bits have to be set for proper operation.

When the BS8 bit is set the device delays the assertion of the DREQ signal until 8 bytes or 4 words transfer is possible.

When the BS8 bit is set and the device is in a DMA write mode the DREQ signal will be asserted only when 8 byte locations are available for writing. In the DMA read mode the DREQ signal will go active under the following circumstances:

At the end of a transfer,

- In the target mode,
  - when the transfer is complete

  or
  - when the $\overline{\text{ATN}}$ signal is active
- In the initiator mode,
  - when the Current Transfer Register is decremented to zero

  or
  - after any phase change

In the middle of a transfer

- In the initiator mode,
  - when the last 8 bytes of the FIFO are full
  - during Synchronous Data-In transfer when the Event Transfer Count Register is greater than 7 and the last 8 bytes of the FIFO are full.

When the BS8 bit is reset and the device is in a DMA read or write mode the DREQ signal will toggle every time the data is strobed by the $\overline{\text{DMARD}}$ or $\overline{\text{DMAWR}}$ signals.

Using Bit 0 (BS8) and Bit 1 (MDM) of Control Register 3, one can enable the different combination modes shown in the table below.

(MDM) Bit 1	(BS8) Bit 0	Function	Maximum Synchronous Offset
0	0	Normal DMA Mode	15
0	1	Burst Size 8 Mode	7
1	0	Reserved	–
1	1	Modified DMA Mode	15

Data Alignment Register (0FH) Write

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The Data Alignment Register (DALREG) is used if the first byte of a 16-bit DMA transfer from the SCSI bus to the host processor is misaligned. Prior to issuing an information transfer command, the host processor must set the Data Alignment Enable (DAE) bit in the CNTLREG2.

DALREG – Bits 7:0 – DA 7:0 – Data Alignment 7:0

COMMANDS

The device commands can be broadly divided into two categories, DMA commands and non-DMA commands. DMA commands are those which cause data movement between the host memory and the SCSI bus while non-DMA commands are those that cause data movement between the device FIFO and the SCSI bus. The MSB of the command byte differentiate the DMA from the non-DMA commands.

Summary of Commands

Command	Command Code (Hex.)	
	Non-DMA Mode	DMA Mode
Initiator Commands		
Information Transfer	10	90
Initiator Command Complete Steps	11	91
Message Accepted	12	–
Transfer Pad Bytes	18	98
Set $\overline{\text{ATN}}$	1A	–
Reset $\overline{\text{ATN}}$	1B	–
Target Commands		
Send Message	20	A0
Send Status	21	A1
Send Data	22	A2
Disconnect Steps	23	A3
Terminate Steps	24	A4
Target Command Complete Steps	25	A5
Disconnect	27	A7
Receive Message	28	A8
Receive Command Steps	29	A9
Receive Data	2A	AA
Receive Command Steps	2B	AB
Target Abort DMA	04	84

Command	Command Code (Hex.)	
	Non-DMA Mode	DMA Mode
Idle State Commands		
Reselect Steps	40	C0
Select without $\overline{\text{ATN}}$ Steps	41	C1
Select with $\overline{\text{ATN}}$ Steps	42	C2
Select with $\overline{\text{ATN}}$ and Stop Steps	43	C3
Enable Selection/Reselection	44	C4
Disable Selection/Reselection	45	C5
Select With $\overline{\text{ATN3}}$	46	C6
General Commands		
No Operation	00	80
Clear FIFO	01	81
Reset Device	02	82
Reset SCSI bus	03	83

COMMAND DESCRIPTION

Initiator Commands

Initiator commands are executed by the device when it is in the initiator mode. If the device is not in the initiator mode and an initiator command is received the device will ignore the command, generate an illegal command interrupt and clear the Command Register (CMDREG) 03H.

Information Transfer Command (Command Code 10H/90H)

The Information Transfer command is used to transfer information bytes over the SCSI bus. This command may be issued during any SCSI Information Transfer phase. Information transfer for synchronous data must use the DMA mode.

The device will continue to transfer information until it is terminated by any one of the following conditions:

- The target changes the SCSI bus phase before the expected number of bytes are transferred. The device clears the Command Register (CMDREG) 03H, and generates a service interrupt when the target asserts $\overline{REQ}$.
- Transfer is successfully complete. If the phase is Message Out, the device deasserts $\overline{ATN}$ before asserting $\overline{ACK}$ for the last byte of the message. When the target asserts $\overline{REQ}$, a service interrupt is generated.
- In the Message In phase when the device receives the last byte. The device keeps the $\overline{ACK}$ signal asserted and generates a Successful Operation interrupt.

During synchronous data transfers the target may send up to the maximum synchronous threshold number of $\overline{REQ}$ pulses to the initiator. If it is the Synchronous Data-In phase then the target sends the data and the $\overline{REQ}$ pulses. These bytes are stored by the initiator in the FIFO as they are received.

Information Transfer Command when issued during the following SCSI phases and terminating in synchronous data phases, is handled as described below:

- Message In/Status Phase – When a phase change to Synchronous Data-In or Synchronous Data-Out is detected by the device, the Command Register (CMDREG) 03H is cleared and the DMA interface is disabled to disallow any transfer of data phase bytes. If the phase change is to Synchronous Data-In and bad parity is detected on the data bytes coming in, it is not reported since the Status Register (STATREG) 04H will report the status of the command just completed. The parity error flag and the $\overline{ATN}$ signal will be asserted when the Transfer Information command begins execution.
- Message Out/Command Phase – When a phase change to Synchronous Data-In or Synchronous Data-Out is detected by the device, the Command Register (CMDREG) 03H is cleared and the DMA interface is disabled to allow any transfer of data phase bytes. If the phase change is to Synchronous Data-In and bad parity is detected on the data bytes coming in, it is not reported since the Status Register (STATREG) 04H will report the status of the command just completed. The parity error flag and the ATN signal will be asserted when the Transfer Information command begins execution. The FIFO Register29 (FFREG) 02H will be latched and will remain in that condition until the next command begins execution. The value in the FFREG indicates the number of bytes in the FIFO when the phase changed to Synchronous Data-In. These bytes are cleared from the FIFO, which now contains only the incoming data bytes.
- In the Synchronous Data-Out phase, the threshold counter is incremented as $\overline{REQ}$ pulses are received. The transfer is completed when the FIFO is empty and the Current Transfer Count Register (CTCREG) 00H–01H is zero. The threshold counter will not be zero.
- In the Synchronous Data-In phase, the Current Transfer Count Register (CTCREG) is decremented as bytes are read from the FIFO rather than being decremented when the bytes are being written to the FIFO. The transfer is completed when Current Transfer Count Register (CTCREG) is zero but the FIFO may not be empty.

Initiator Command Complete Steps (Command Code 11H/91H)

The Initiator Command Complete Steps command is normally issued when the SCSI bus is in the Status In phase. One Status byte followed by one Message byte is transferred if this command completes normally. After receiving the message byte the device will keep the $\overline{ACK}$ signal asserted to allow the initiator to examine the message and assert the $\overline{ATN}$ signal if it is unacceptable. The command terminates early if the target does not switch to the Message In phase or if the target disconnects from the SCSI bus.

Message Accepted Command (Command Code 12H)

The Message Accepted Command is used to release the $\overline{ACK}$ signal. This command is normally used to complete a Message In handshake. Upon execution of this command the device generates a service request interrupt after $\overline{REQ}$ is asserted by the target.

After the device has received the last byte of message, it keeps the $\overline{ACK}$ signal asserted. This allows the device to either accept or reject the message. To accept the message, Message Accepted Command is issued. To reject the message the $\overline{ATN}$ signal must be asserted (with the help of the Set $\overline{ATN}$ Command) before issuing the Message Accepted Command. In either case the Message Accepted Command has to be issued to release the $\overline{ACK}$ signal.

Transfer Pad Bytes Command (Command Code 18H/98H)

The Transfer Pad Bytes Command is used to recover from an error condition. This command is similar to the Information Transfer Command, only the information bytes consists of null data. It is used when the target expects more data bytes than the initiator has to send. It is also used when the initiator receives more information than it expected from the target.

When sending data to the SCSI bus, the FIFO is loaded with null bytes and these bytes are sent out to the SCSI bus. DMA has to be enabled when pad bytes are transferred to the SCSI bus. No actual DMA requests are made but the device uses the Current Transfer Count Register (CTCREG) 00H–01H to terminate the transfer.

When receiving data from the SCSI bus, the device will receive the pad bytes and place them on the top of the FIFO and unload them from the bottom of the FIFO.

The command terminates under the same condition as the Information Transfer Command, only the device does not keep the $\overline{ACK}$ signal asserted during the last byte of the Message In phase. If this command terminates prematurely, due to a disconnect or a phase change, before the CTCREG decrements to zero, the FIFO may contain residual pad bytes.

Set $\overline{ATN}$ Command (Command Code 1AH)

The Set $\overline{ATN}$ Command is used to drive the $\overline{ATN}$ signal active on the SCSI bus. An interrupt is not generated at the end of this command. The $\overline{ATN}$ signal is deasserted before asserting the $\overline{ACK}$ signal during the last byte of the Message Out phase.

Note:
The $\overline{ATN}$ *signal is asserted by the device without this command in the following cases:*

- If any select with $\overline{ATN}$ command is issued and the arbitration is won.
- An initiator needs the target's attention to send a message. The $\overline{ATN}$ signal is asserted before deasserting the $\overline{ACK}$ signal.

Reset $\overline{ATN}$ Command (Command Code 1BH)

The Reset $\overline{ATN}$ Command is used to deassert the $\overline{ATN}$ signal on the SCSI bus. An interrupt is not generated at the end of this command. This command is used only when interfacing with devices that do not support the Common Command Set (CCS). These older devices do not deassert their $\overline{ATN}$ signal automatically on the last byte of the Message Out phase. This device does deassert its $\overline{ATN}$ signal automatically on the last byte of the Message Out phase.

Target Commands

Target commands are executed by the device when it is in the target mode. If the device is not in the target mode and a target command is received the device will ignore the command, generate an illegal command interrupt and clear the Command Register (CMDREG) 03H.

A SCSI bus reset during any target command will cause the device to abort the command sequence , flag a SCSI bus reset interrupt (if the interrupt is enabled) and disconnect from the SCSI bus.

Normal or successful completion of a target command will cause a Successful Operation interrupt to be flagged. If the $\overline{ATN}$ signal is asserted during a target command sequence the Service Request bit is asserted in the Interrupt Status Register (INSTREG) 05H. If the $\overline{ATN}$ signal is asserted when the device is in an idle state a Service Request interrupt will be generated, the Successful Operation bit in the INSTREG will be reset and the CMDREG cleared.

Send Message Command (Command Code 20H/A0H)

The Send Message Command is used by the target to inform the initiator to receive a message. The SCSI bus phase lines are set to the Message In Phase and message bytes are transferred from the device FIFO to the buffer memory.

Send Status Command (Command Code 21H/A1H)

The Send Status Command is used by the target to inform the initiator to receive status information. The SCSI bus phase lines are set to the Status Phase and status bytes are transferred from the target device to the initiator device.

Send Data Command (Command Code 22H/A2H)

The Send Data Command is used by the target to inform the initiator to receive data bytes. The SCSI bus phase lines are set to the Data-In Phase and data bytes are transferred from the target device to the initiator device.

Disconnect Steps Command (Command Code 23H/A3H)

The Disconnect Steps Command is used by the target to disconnect from the SCSI bus. This command consists of two steps. The first step consists of sending two bytes of the Save Data Pointers commands by the target in the Message In Phase. In the second step the target disconnects from the SCSI bus. Successful Operation and Disconnected bits are set in the Interrupt Status Register (INSTREG) 05H upon command completion. If $\overline{ATN}$ signal is asserted by the initiator then Successful Operation and Service Request bits are set in the INSTREG, the CMDREG is cleared and Disconnect Steps Command terminates without disconnecting.

Terminate Steps Command (Command Code 24H/A4H)

The Terminate Steps Command is used by the target to disconnect from the SCSI bus. This command consists of three steps. The first step consists of sending one status byte by the target in the Status Phase. The second step consists of sending one message byte by the target in the Message In Phase. As the third step the target disconnects from the SCSI bus. Successful Operation and Disconnected bits are set in the Interrupt Status Register (INSTREG) 05H upon command completion. If $\overline{ATN}$ signal is asserted by the initiator then Successful Operation and Service Request bits are set in the INSTREG, the CMDREG is cleared and Terminate Steps Command terminates without disconnecting.

Target Command Complete Steps Command (Command Code 25H/A5H)

The Target Command Complete Steps Command is used by the target to inform the initiator of a linked command completion. This command consists of two steps. The first step consists of sending one status byte by the target in the Status Phase. The second step consists of sending one message byte by the target in the Message In Phase. The Successful Operation bit is set in the Interrupt Status Register (INSTREG) 05H upon command completion. If $\overline{ATN}$ signal is asserted by the initiator then Successful Operation and Service Request bits are set in the INSTREG, the CMDREG is cleared and Target Command Complete Steps Command terminates prematurely.

Disconnect Command (Command Code 27H/A7H)

The Disconnect Command is used by the target to disconnect from the SCSI bus. All SCSI bus signals except $\overline{RSTC}$ are released and the device returns to the Disconnected state. The $\overline{RSTC}$ signal is driven active for about 25 micro seconds (depending on clock frequency and clock factor). Interrupt is not generated to the microprocessor.

Receive Message Steps Command (Command Code 28H A8H)

The Receive Message Steps Command is used by the target to request message bytes from the initiator. During this command the target receives the message bytes from the initiator while the SCSI bus is in the Message Out Phase. The Successful Operation bit is set in the Interrupt Status Register (INSTREG) 05H upon command completion. If $\overline{ATN}$ signal is asserted by the initiator then Successful Operation and Service Request bits are set in the INSTREG, the CMDREG is cleared. If a parity error is detected, the device ignores the received message bytes until $\overline{ATN}$ signal is asserted, the Successful Operation bit is set in the INSTREG, and the CMDREG is cleared.

Receive Commands Command (Command Code 29H/A9H)

The Receive Commands Command is used by the target to request the initiator for command bytes. During this command the target receives the command bytes from the initiator while the SCSI bus is in the Command Phase. The Successful Operation bit is set in the Interrupt Status Register (INSTREG) 05H upon command completion. If $\overline{ATN}$ signal is asserted by the initiator then Successful Operation and Service Request bits are set in the INSTREG, the CMDREG is cleared and the command terminates prematurely. If a parity error is detected, the device continues to receive command bytes until the transfer is complete if the Abort on Command/Data Parity Error (ACDPE) bit in the Control Register (CNTLREG2) 0BH is reset. If the ACDPE bit is set, the command is terminated immediately. The Parity Error (PE) bit in the Status Register (STATREG) 04H is set and CMDREG is cleared.

Receive Data Command (Command Code 2AH/AAH)

The Receive Data Command is used by the target to request the initiator for data bytes. During this command the target receives the data bytes from the initiator while the SCSI bus is in the Data-Out Phase. The Successful Operation bit is set in the Interrupt Status Register (INSTREG) 05H upon command completion. If $\overline{ATN}$ signal is asserted by the initiator then Successful Operation and Service Request bits are set in the INSTREG, the CMDREG is cleared and the command terminates prematurely. If a parity error is detected, the device continues to receive data bytes until the transfer is complete if the Abort on Command/Data Parity Error (ACDPE) bit in the Control Register (CNTLREG2) 0BH is reset. If the ACDPE bit is set, the command is terminated immediately. The Parity Error (PE) bit in the Status Register (STATREG) 04H is set and CMDREG is cleared.

Receive Command Steps Command (Command Code 2BH/ABH)

The Receive Command Steps Command is used by the target to request the initiator for command information bytes. During this command the target receives the command information bytes from the initiator while the SCSI bus is in the Command Phase.

The target device determines the command byte length from the first command byte. If an unknown length is received, the Start Transfer Count Register (STCREG) 00H–01H is loaded with 5 and the Group Code Valid (GCV) bit in the Status Register (STATREG) 04H is reset. If a valid length is received, the STCREG is loaded with the appropriate value and the GCV bit in the STATREG is set. If $\overline{ATN}$ signal is asserted by the initiator then the Service Request bit is set in the INSTREG, and the CMDREG is cleared If a parity error is detected, the command is terminated prematurely and the CMDREG is cleared.

DMA Stop Command (Command Code 04H/84H)

The DMA Stop Command is used by the target to allow the microprocessor to discontinue data transfers due to a lack of activity on the DMA channel. This command is executed from the top of the command queue. If there is a queued command waiting execution, it will be overwritten and the Illegal Operation Error (IOE) bit in the

Status Register (STATREG) 04H will be set. This command is cleared from the command queue once it is decoded.

Caution must be exercised when using this command.

The DMA Stop Command can be used only during a DMA Target Send Data Command or DMA Target Receive Data Command execution. In both cases the DMA controller has to be in the idle state.

During a DMA Target Send Data Command the FIFO has to be empty or the Current FIFO (CF 4:0) bits in the Current FIFO/Internal State Register (CFISREG) 07H are zero.

During a DMA Synchronous Target Receive Data Command the Current Transfer Count Register (CTCREG) 00–01H is zero, which is indicated by the Count to Zero (CTZ) bit of the Status Register (STATREG) 04H. or when the Synchronous Offset Register (SOFREG) 07H has reached its maximum value which is indicated by the Synchronous Offset Flag (SOF) bit of the Internal State Register (ISREG) 06H.

During a DMA Asynchronous Target Receive Data Command the FIFO is full which is indicated by the Current FIFO (CF 4:0) bits in the Current FIFO/Internal State Register (CFISREG) 07H being all high or Current Transfer Count Register (CTCREG) 00–01H is zero, which is indicated by the Count to Zero (CTZ) bit of the Status Register (STATREG) 04H.

Idle State Commands

The Idle State Commands can be issued to the device only when the device is disconnected from the SCSI bus. If these commands are issued to the device when it is logically connected to the SCSI bus, the commands are ignored, and the device will generate an illegal command interrupt and clear the Command Register (CMDREG) 03H.

Reselect Steps Command (Command Code 40H/C0H)

The Reselect Steps Command is used by the target device to reselect an initiator device. When this command is issued the device arbitrates for the control of the SCSI bus. If the device wins arbitration, it reselects the initiator device and transfers a single byte identify message. Before issuing this command the SCSI Timeout Register (STIMREG) 05H, the Control Register One (CNTLREG1) 08H and the SCSI Destination ID Register (SDIDREG) 04H must be set to the proper values. If DMA is enabled, the Start Transfer Count Register (STCREG) 00H–01H must be set to one. If DMA is not enabled, the single byte identify message must be loaded into the FIFO before issuing this command. This command will be terminated early if the SCSI Timeout Register times out. This command also resets the Internal State Register (ISREG) 06H.

Select without ATN Steps Command (Command Code 41H/C1H)

The Select without ATN Steps Command is used by the initiator to select a target. When this command is issued the device arbitrates for the control of the SCSI bus. When the device wins arbitration, it selects the target device and transfers the Command Descriptor Block (CDB). Before issuing this command the SCSI Timeout Register (STIMREG) 05H, the Control Register One (CNTLREG1) 08H and the SCSI Destination ID Register (SDIDREG) 04H must be set to the proper values. If DMA is enabled, the Start Transfer Count Register (STCREG) 00H–01H must be set to the total length of the command. If DMA is not enabled, the data must be loaded into the FIFO before issuing this command. This command will be terminated early if the SCSI Timeout Register times out or if the target does not go to the Command Phase following the Selection Phase or if the target exits the Command Phase early.

Select with ATN Steps Command (Command Code 42H/C2H)

The Select with ATN Steps Command is used by the initiator to select a target. When this command is issued the device arbitrates for the control of the SCSI bus. When the device wins arbitration, it selects the target device with the $\overline{\text{ATN}}$ signal asserted and transfers the Command Descriptor Block (CDB) and a one byte message. Before issuing this command the SCSI Timeout Register (STIMREG) 05H, the Control Register One (CNTLREG1) 08H and the SCSI Destination ID Register (SDIDREG) 04H must be set to the proper values. If DMA is enabled, the Start Transfer Count Register (STCREG) 00H–01H must be set to the total length of the command. If DMA is not enabled, the data must be loaded into the FIFO before issuing this command. This command will be terminated early in the following situations:

- The SCSI Timeout Register times out
- The target does not go to the Message Out Phase following the Selection Phase
- The target exits the Message Phase early
- The target does not go to the Command Phase following the Selection Phase
- The target exits the Command Phase early.

Select with ANT and Stop Steps Command (Command Code 43H/C3H)

The Select with ATN and Stop Steps Command is used by the initiator to select a target. When this command is issued the device arbitrates for the control of the SCSI bus. When the device wins arbitration, it selects the target device with the $\overline{\text{ATN}}$ signal asserted and transfers the Command Descriptor Block (CDB) and stops after one message byte is sent, but the $\overline{\text{ATN}}$ signal is not

deasserted at the end of the command which allows the initiator to send other messages after the ID message is sent out. Before issuing this command the SCSI Timeout Register (STIMREG) 05H, the Control Register One (CNTLREG1) 08H and the SCSI Destination ID Register (SDIDREG) 04H must be set to the proper values. This command will be terminated early if the SCSI Timeout Register times out or if the target does not go to the Message Out Phase following the Selection Phase.

Enable Selection/Reselection Command (Command Code 44H/C4H)

The Enable Selection/Reselection Command is used by the target to respond to a bus-initiated reselection. Upon disconnecting from the bus the Selection/Reselection circuit is automatically disabled by device. This circuit has to be enabled for the device to respond to subsequent reselection attempts and the Enable Selection/ Reselection Command is issued to do that. This command is normally issued within 250 ms (select/reselect timeout) after the device disconnects from the bus. If DMA is enabled the device loads the received data to the buffer memory, but if the DMA is disabled, the received data stays in the FIFO.

Disable Selection/Reselection Command (Command Code 45H/C5H)

The Disable Selection/Reselection Command is used by the target to disable response to a bus-initiated reselection. When this command is issued before a bus initiated selection or reselection is initiated, it resets the internal mode bits previously set by the Enable Selection/Reselection Command. The device also generates a function complete interrupt to the processor. If however, this command is issued after a bus initiated selection/reselection has already begun the command is ignored since the Command Register is held reset and all incoming commands are ignored. The device generates a selected or reselected interrupt when the sequence is complete.

Select with ATN3 Steps Command (Command Code 46H/C6H)

The Select with ATN3 Steps Command is used by the initiator to select a target. This command is similar to the Select with ATN Steps Command, except that it sends exactly three message bytes. When this command is issued the device arbitrates for the control of the SCSI bus. When the device wins arbitration, it selects the target device with the $\overline{\text{ATN}}$ signal asserted and transfers the Command Descriptor Block (CDB) and three message bytes. Before issuing this command the SCSI Timeout Register (STIMREG) 05H, the Control Register One (CNTLREG1) 08H and the SCSI Destination ID Register (SDIDREG) 04H must be set to the proper values. If DMA is enabled, the Start Transfer Count Register (STCREG) 00H–01H must be set to the total length of the command. If DMA is not enabled, the data must be loaded into the FIFO before issuing this command. This command will be terminated early in the following situations:

- The SCSI Timeout Register times out
- The target does not go to the Message Out Phase following the Selection Phase
- The target exits the Message Phase early
- The target does not go to the Command Phase following the Selection Phase
- The target exits the Command Phase early.

General Commands

No Operation Command (Command Code 00H/80H)

The No Operation Command is used to perform no operation and no interrupt is generated at the end of this command. This command is issued after the Reset Device Command to enable the Command Register. A No Operation Command in the DMA mode may be used to verify the contents of the Start Transfer Count Register (STCREG) 00H – 01H. After the STCREG is loaded with the transfer count and a No Operation Command is issued, reading the Current Transfer Count Register (CTCREG) 00H–01H will give the transfer count value.

Clear FIFO Command (Command Code 01H/81H)

The Clear FIFO Command is used to initialize the FIFO to the empty condition. The Current FIFO Register (CFISREG) 07H reflects the empty FIFO status and the bottom of the FIFO is set to zero. No interrupt is generated at the end of this command.

Reset Device Command (Command Code 02H/82H)

The Reset Device Command immediately stops any device operation and resets all the functions of the device. It returns the device to the disconnected state and it also generates a hard reset. The Reset Device Command remains on the top of the Command Register FIFO holding the device in the reset state until the No Operation Command is loaded. The No Operation command serves to enable the Command Register.

Reset SCSI Bus Command (Command Code 03H/83H)

The Reset SCSI Bus Command is used to assert the $\overline{\text{RSTC}}$ signal for approximately 25 ms. This command causes the device to go to the disconnected state. No interrupt is generated upon command completion. A SCSI reset interrupt is however generated upon command completion if the interrupt is not disabled in the Control Register One (CNTLREG1) 08H.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature Under Bias . –55°C to +125°C

V_{DD} . . . . . –0.5 V to +7.0 V

DC Voltage Applied to Any Pin . –0.5 to (V_{DD} +0.5) V

Input Static Discharge Protection . . 4000 V pin to pin (Human body model: 100 pF at 1.5K Ω)

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Supply Voltage (V_{DD}) . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

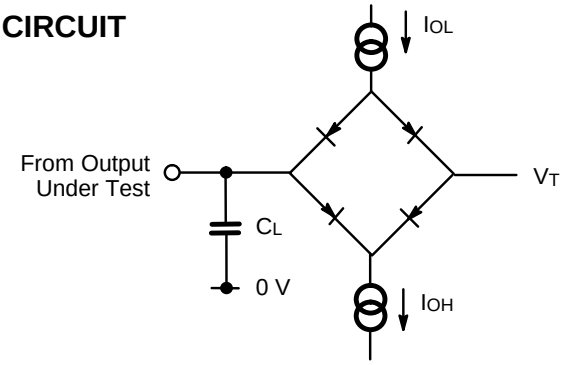
DC OPERATING CHARACTERISTICS

Parameter Symbol	Parameter Description	Pin Names	Test Conditions	Min	Max	Unit
I_{DDS}	Static Supply Current		$V_{DD\ MAX}$		4.0	mA
I_{DDD}	Dynamic Supply Current		$V_{DD\ MAX}$		35	mA
I_{LU}	Latch Up Current	All I/O	$V_{LU} \le 10$ V	– 100	+100	mA
C	Capacitance	All Pins			10	pF
SCSI Pins						
V_{IH}	Input High Voltage	All SCSI Inputs		2.0	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	All SCSI Inputs		V_{SS} – 0.5	0.8	V
V_{IHST}	Input Hysterisis	All SCSI Inputs	4.75 V < V_{DD} < 5.25 V	300		mV
V_{OH}	Output High Voltage	$\overline{SD}_{7–0}$, $\overline{SD}_P$	I_{OH} = – 2 mA	2.4	V_{DD}	V
V_{SOL1}	SCSI Output Low Voltage	$\overline{SD}_{7–0}$, $\overline{SD}_P$	I_{OL}= 4 mA	V_{SS}	0.4	V
V_{SOL2}	SCSI Output Low Voltage	$\overline{SDC}_{7–0}$, $\overline{SDC}_P$, $\overline{MSG}$, $\overline{C/D}$, $\overline{I/O}$, $\overline{ATN}$, $\overline{RSTC}$, $\overline{SELC}$, $\overline{BSYC}$, $\overline{ACKC}$ and $\overline{REQC}$	I_{OL}= 48 mA	V_{SS}	0.5	V
I_{IL}	Input Low Leakage		0.0 V < V_{IN} < 2.7 V	–10	+10	µA
I_{IH}	Input High Leakage		2.7 V < V_{IN} < V_{DD}	–10	+10	µA
I_{OZ}	High Impedance Leakage		0 V < V_{OUT} < V_{DD}	–10	+10	µA
Bidirectional Pins						
V_{IH}	Input High Voltage			2.0	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output High Voltage	DMA 15–0, DMAP 1–0 and AD 7–0	I_{OH} = – 2 mA	2.4	V_{DD}	V
V_{OL}	Output Low Voltage	DMA 15–0, DMAP 1–0 and AD 7–0	I_{OL}= 4 mA	V_{SS}	0.4	V
I_{IL}	Input Low Leakage	DMA 15–0, DMAP 1–0 and AD 7–0	V_{IN} = V_{IL}	– 400	+10	µA
I_{IH}	Input High Leakage	DMA 15–0, DMAP 1–0 and AD 7–0	V_{IN} = V_{IH}	–10	+10	µA
I_{OZ}	High Impedance Leakage		0 V < V_{OUT} < V_{DD}	–100	400	µA
Output Pins						
V_{OH}	Output High Voltage	DREQ, ISEL, TSEL	I_{OH} = – 2 mA	2.4	V_{DD}	V
V_{OL}	Output Low Voltage	DREQ, ISEL, TSEL	I_{OL}= 4 mA	V_{SS}	0.4	V
I_{OZ}	High Impedance Leakage		0 V < V_{OUT} < V_{DD}	–10	+10	µA

DC OPERATING CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description	Pin Names	Test Conditions	Min	Max	Unit
Input Pins						
V_{IH}	Input High Voltage	A 3-0, $\overline{CS}$, $\overline{RD}$. $\overline{WR}$, $\overline{DMAWR}$, CLK, BUSMD 1-0, $\overline{DACK}$, $\overline{RESET}$, and $\overline{DFMODE}$		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	A 3-0, $\overline{CS}$, $\overline{RD}$. $\overline{WR}$, $\overline{DMAWR}$, CLK, BUSMD 1-0, $\overline{DACK}$, $\overline{RESET}$, and $\overline{DFMODE}$		V_{SS} + 0.5	0.8	V
I_{IL}	Input Low Leakage	A 3-0, $\overline{CS}$, $\overline{RD}$. $\overline{WR}$, $\overline{DMAWR}$, CLK, BUSMD 1-0, $\overline{DACK}$, $\overline{RESET}$, and $\overline{DFMODE}$	$V_{IN} = V_{IL}$	–10	+10	µA
I_{IH}	Input High Voltage	A 3-0, $\overline{CS}$, $\overline{RD}$. $\overline{WR}$, $\overline{DMAWR}$, CLK, BUSMD 1-0, $\overline{DACK}$, $\overline{RESET}$, and $\overline{DFMODE}$	$V_{IN} = V_{IH}$	–10	+10	µA

SWITCHING TEST CIRCUIT



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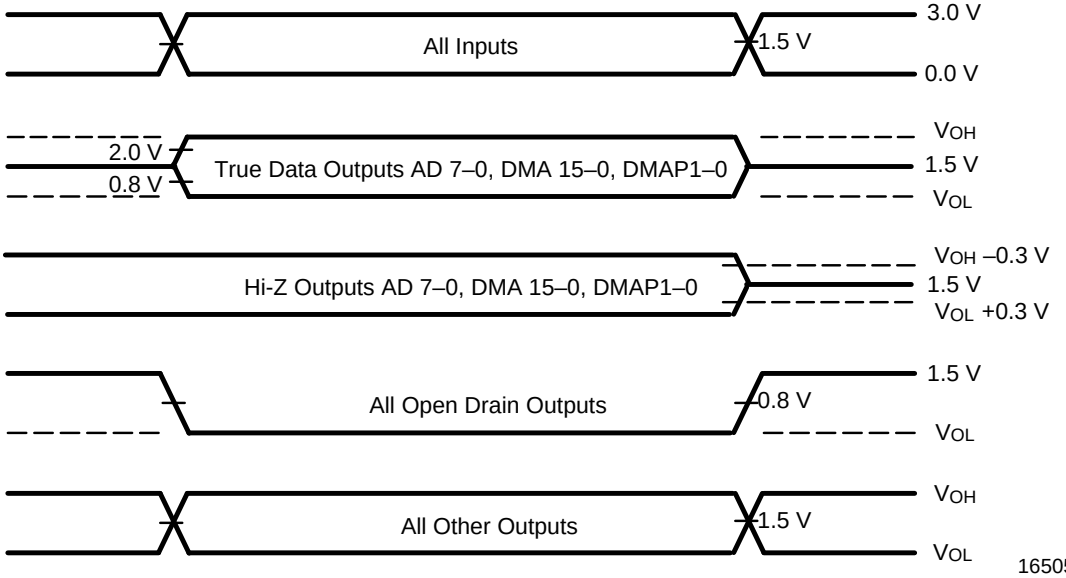
SWITCHING TEST WAVEFORMS



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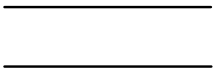
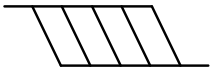
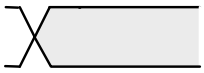
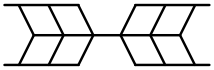
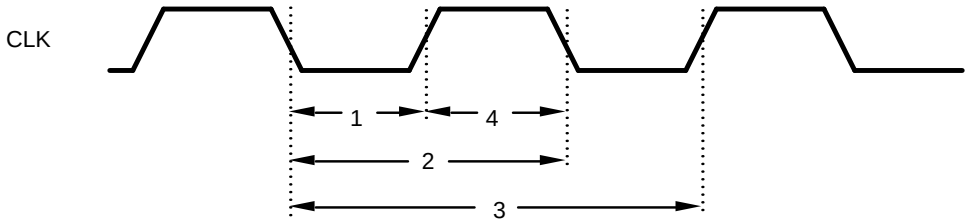
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance “Off” State

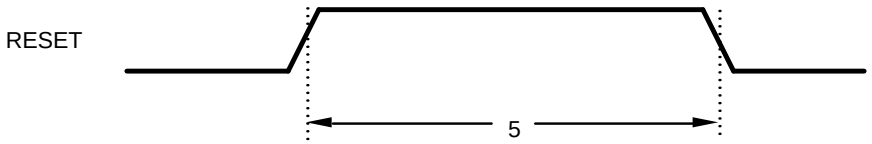
KS000010



Clock Input 16505C-36

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
1	t_{PWL}	Clock Pulse Width Low		14.58		ns
2	t_{CP}	Clock period		40	100	ns
3	t_L	Synchronization latency (parameter 2 + parameter 1)		54.58	185.42	ns
4	t_{PWH}	Clock Pulse Width High		14.58		ns

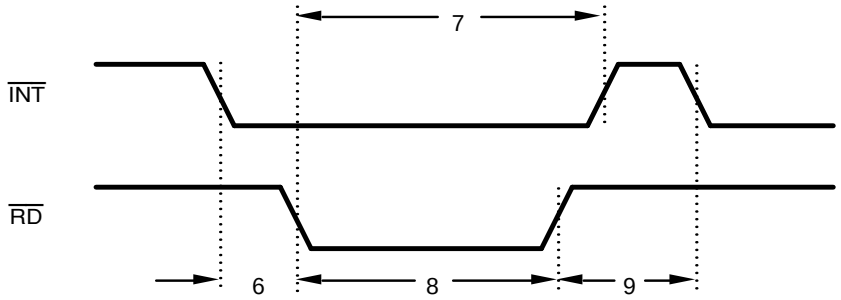
Note:
Clock Frequency Range = 10 to 25 MHz for Asynchronous SCSI Bus
= 12 to 25 MHz for Synchronous SCSI Bus



Reset Input 16505C-37

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
5	t_{PWH}	Reset Pulse Width High		500		ns

Note:
There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).

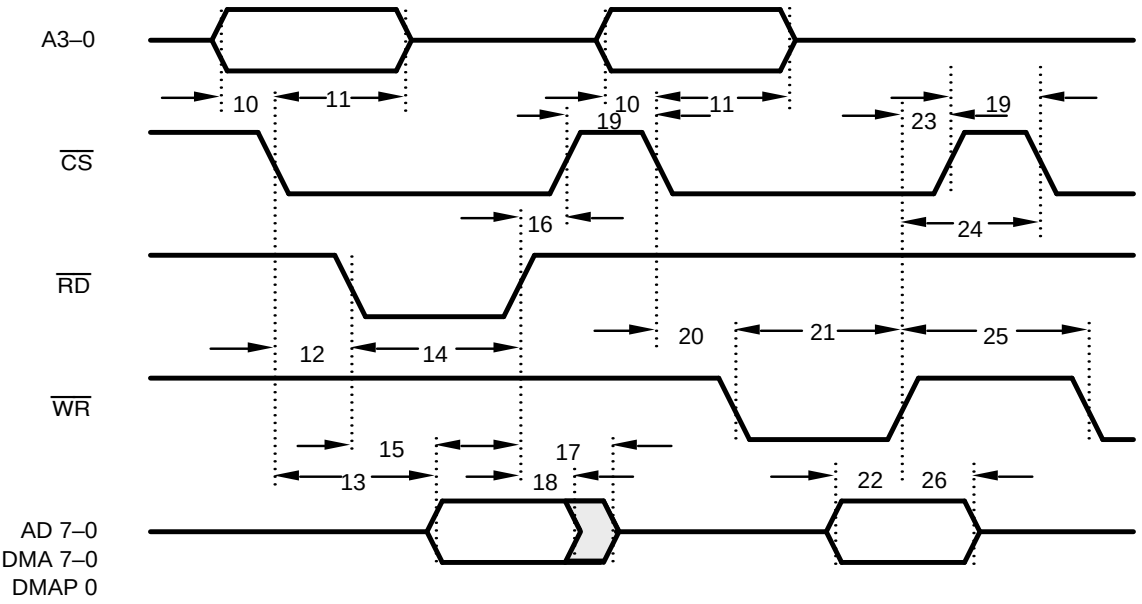


16505C-38

Interrupt Output

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
6	t_S	$\overline{INT}$ ↓ to $\overline{RD}$ ↓ Set Up Time		0		ns
7	t_{PD}	$\overline{RD}$ ↓ to $\overline{INT}$ ↑ Delay		0	100	ns
8	t_{PWL}	$\overline{RD}$ Pulse Width Low		50		ns
9	t_{PD}	$\overline{RD}$ ↑ to $\overline{INT}$ ↓ Delay		$t_L - t_{PD}$		ns

Note:
There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).

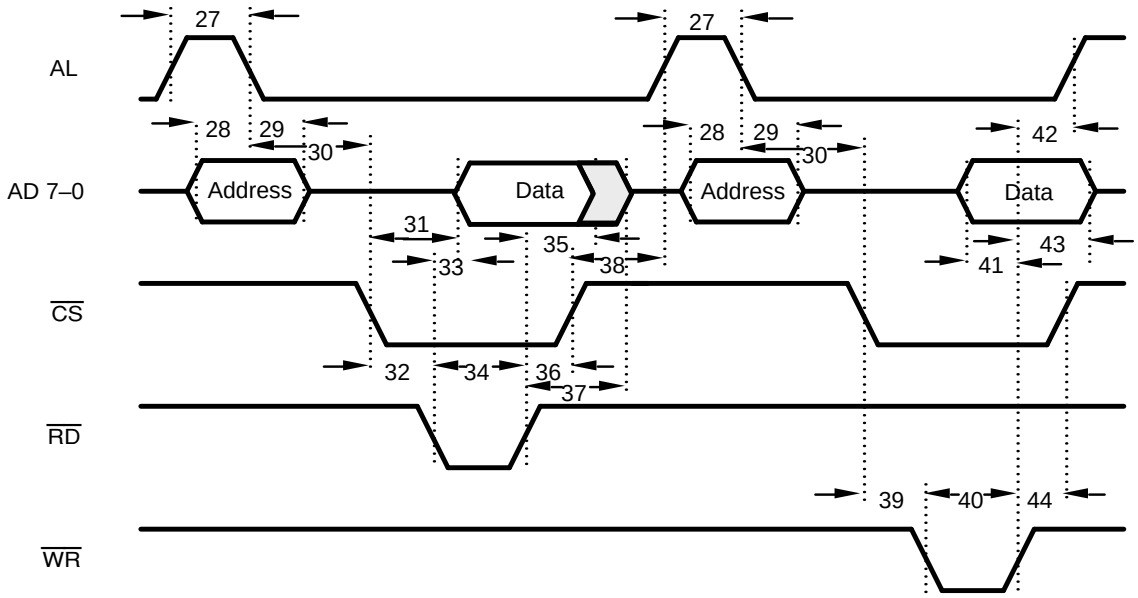


Register Read/Write with Non-Multiplexed Address Data Bus

16505C-39

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
10	t_S	Address to $\overline{CS}$ ↓ Set Up Time		0		ns
11	t_H	Address to $\overline{CS}$ ↓ Hold Time		50		ns
12	t_S	$\overline{CS}$ ↓ to $\overline{RD}$ ↓ Set Up Time		0		ns
13	t_{PD}	$\overline{CS}$ ↓ to Data Valid Delay			90	ns
14	t_{PWL}	$\overline{RD}$ Pulse Width Low		50		ns
15	t_{PD}	$\overline{RD}$ ↓ to Data Valid Delay			50	ns
16	t_H	$\overline{RD}$ ↑ to $\overline{CS}$ ↑ Hold Time		0		ns
17	t_Z	$\overline{RD}$ ↑ to Data High Impedance			40	ns
18	t_H	$\overline{RD}$ ↑ to Data Hold Time		2		ns
19	t_{PWH}	$\overline{CS}$ Pulse Width High		40		ns
20	t_S	$\overline{CS}$ ↓ to $\overline{WR}$ ↓ Set Up Time		0		ns
21	t_{PWL}	$\overline{WR}$ Pulse Width Low		40		ns
22	t_S	Data to $\overline{WR}$ ↑ Set Up Time		15		ns
23	t_H	$\overline{WR}$ ↑ to $\overline{CS}$ ↑ Hold Time		0		ns
24	t_S	$\overline{WR}$ ↑ to $\overline{CS}$ ↓ Set Up Time		60		ns
25	t_{PWH}	$\overline{WR}$ Pulse Width High		60		ns
26	t_H	Data to $\overline{WR}$ ↑ Hold Time		0		ns

Note:
There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).

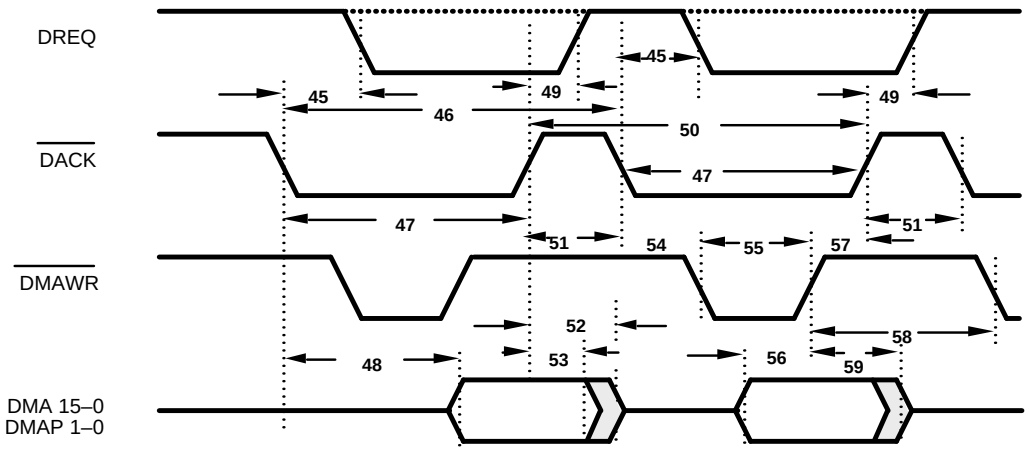


16506C-40

Register Read/Write with Multiplexed Address Data Bus

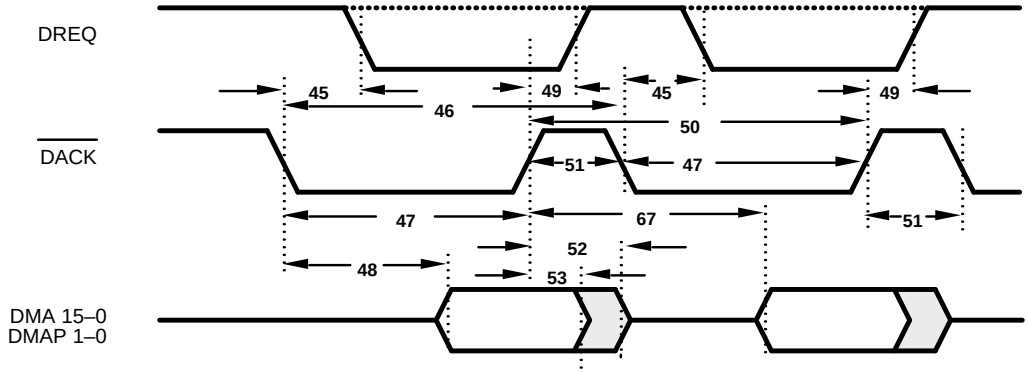
No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
27	t_{PWH}	ALE Pulse Width High		20		ns
28	t_S	Address to ALE ↓ Set Up Time		10		ns
29	t_H	Address to ALE ↓ Hold Time		10		ns
30	t_S	ALE ↓ to $\overline{CS}$ ↓ Set Up Time		10		ns
31	t_{PD}	$\overline{CS}$ ↓ to Data Valid Delay			90	ns
32	t_S	$\overline{CS}$ ↓ to $\overline{RD}$ ↓ Set Up Time		0		ns
33	t_{PD}	$\overline{RD}$ ↓ to Data Valid Delay			50	ns
34	t_{PWL}	$\overline{RD}$ Pulse Width Low		50		ns
35	t_H	$\overline{RD}$ ↑ to Data Hold Time		2		ns
36	t_H	$\overline{RD}$ ↑ to $\overline{CS}$ ↑ Hold Time		0		ns
37	t_Z	$\overline{RD}$ ↑ to Data High Impedance			40	ns
38	t_S	$\overline{CS}$ ↑ to ALE ↑ Set Up Time		50		ns
39	t_S	$\overline{CS}$ ↓ to $\overline{WR}$ ↓ Set Up Time		0		ns
40	t_{PWL}	$\overline{WR}$ Pulse Width Low		40		ns
41	t_S	Data to $\overline{WR}$ ↑ Set Up Time		15		ns
42	t_S	$\overline{WR}$ ↑ to ALE ↑ Set Up Time		50		ns
43	t_H	Data to $\overline{WR}$ ↑ Hold Time		0		ns
44	t_H	$\overline{WR}$ ↑ to $\overline{CS}$ ↑ Hold Time		0		ns

Note:
There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).



16506C-41

DMA Write without Byte Control



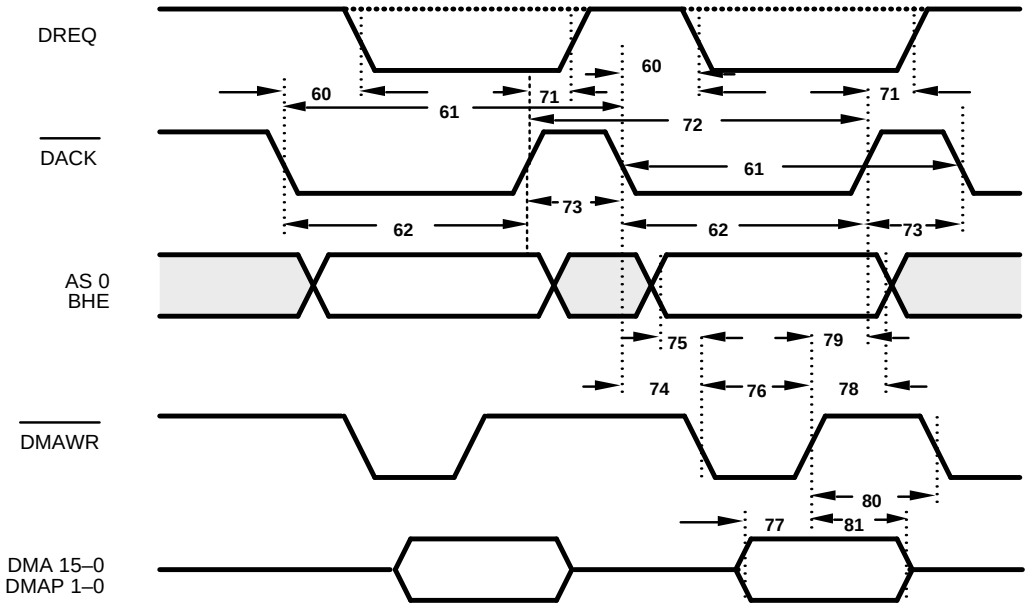
16506C-42

DMA Read without Byte Control

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
45	t_{PD}	$\overline{DACK}$ ↓ to DREQ ↓ Valid Delay			38	ns
46	t_P	$\overline{DACK}$ ↓ to $\overline{DACK}$ ↓ period		100		ns
47	t_{PWL}	$\overline{DACK}$ Pulse Width Low		60		ns
48	t_{PD}	$\overline{DACK}$ ↓ to Data Valid Delay			41	ns
49	t_{PD}	$\overline{DACK}$ ↑ to DREQ ↑ Valid Delay			40	ns
50	t_P	$\overline{DACK}$ ↑ to $\overline{DACK}$ ↑ period		t_3+50–t_{51}		ns
51	t_{PWH}	$\overline{DACK}$ Pulse Width High		12		ns
52	t_Z	$\overline{DACK}$ ↑ to Data High Impedance			40	ns
53	t_H	$\overline{DACK}$ ↑ to Data Hold Time		2		ns
54	t_S	$\overline{DACK}$ ↓ to $\overline{DMAWR}$ ↓ Set Up Time		0		ns
55	t_{PWL}	$\overline{DMAWR}$ Pulse Width Low		50		ns
56	t_S	Data to $\overline{DMAWR}$ ↑ Set Up Time		15		ns
57	t_H	$\overline{DMAWR}$ ↑ to $\overline{DACK}$ ↑ Hold Time		0		ns
58	t_{PWH}	$\overline{DMAWR}$ Pulse Width High		40		ns
59	t_H	Data to $\overline{DMAWR}$ ↑ Hold Time		0		ns

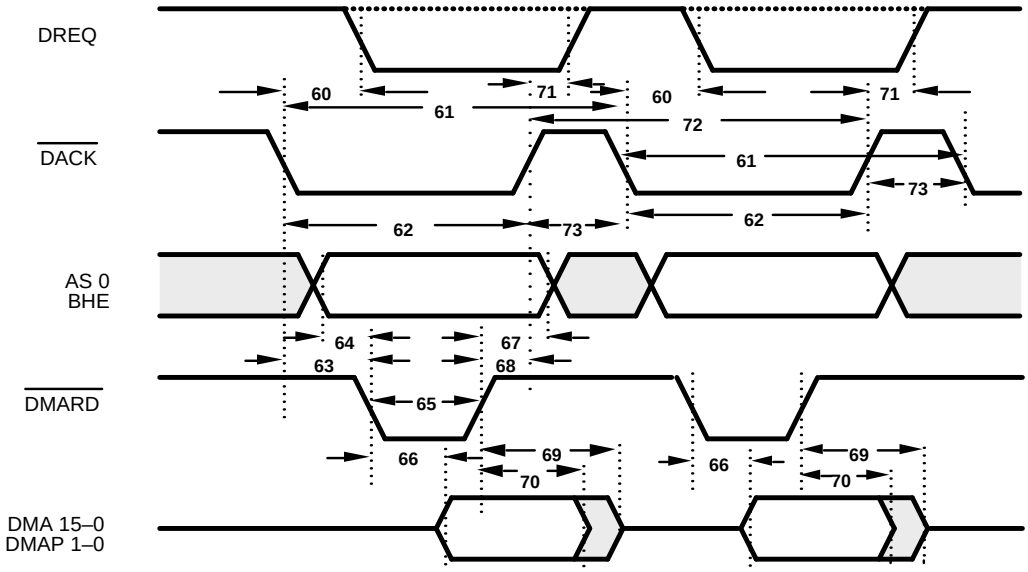
Note:

There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).



16506C-52

DMA Write with Byte Control



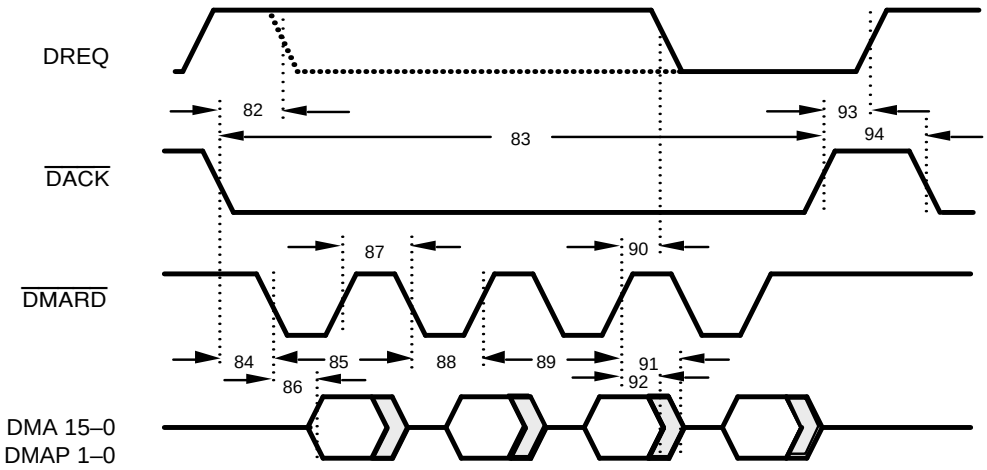
16506C-53

DMA Read with Byte Control

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
60	t_{PD}	$\overline{DACK}$ ↓ to DREQ ↓ Valid Delay			38	ns
61	t_P	$\overline{DACK}$ ↓ to $\overline{DACK}$ ↓ period		100		ns
62	t_{PWL}	$\overline{DACK}$ Pulse Width Low		60		ns
63	t_S	$\overline{DACK}$ ↓ to $\overline{DMARD}$ ↓ Set Up Time		0		ns
64	t_S	BHE, AS0 to $\overline{DMARD}$ ↓ Set Up Time		20		ns
65	t_{PWL}	$\overline{DMARD}$ Pulse Width Low		60		ns
66	t_{PD}	$\overline{DMARD}$ ↓ to Data Valid Delay			51	ns
67	t_H	BHE, AS0 to $\overline{DMARD}$ ↑ Hold Time		20		ns
68	t_H	$\overline{DMARD}$ ↑ to $\overline{DACK}$ ↑ Hold Time		0		ns
69	t_Z	$\overline{DMARD}$ ↑ to Data High Impedance			40	ns
70	t_H	$\overline{DMARD}$ ↑ to Data Hold Time		2		ns
71	t_{PD}	$\overline{DACK}$ ↑ to DREQ ↑ Valid Delay			40	ns
72	t_P	$\overline{DACK}$ ↑ to $\overline{DACK}$ ↑ period		100		ns
73	t_{PWH}	$\overline{DACK}$ Pulse Width High		12		ns
74	t_S	$\overline{DACK}$ ↓ to $\overline{DMAWR}$ ↓ Set Up Time		0		ns
75	t_S	BHE, AS0 to $\overline{DMAWR}$ ↓ Set Up Time		20		ns
76	t_{PWL}	$\overline{DMAWR}$ Pulse Width Low		50		ns
77	t_S	Data to $\overline{DMAWR}$ ↑ Set Up Time		15		ns
78	t_H	BHE, AS0 to $\overline{DMAWR}$ ↑ Hold Time		20		ns
79	t_H	$\overline{DMAWR}$ ↑ to $\overline{DACK}$ ↑ Hold Time		0		ns
80	t_{PWH}	$\overline{DMAWR}$ Pulse Width High		40		ns
81	t_H	Data to $\overline{DMAWR}$ ↑ Hold Time		0		ns

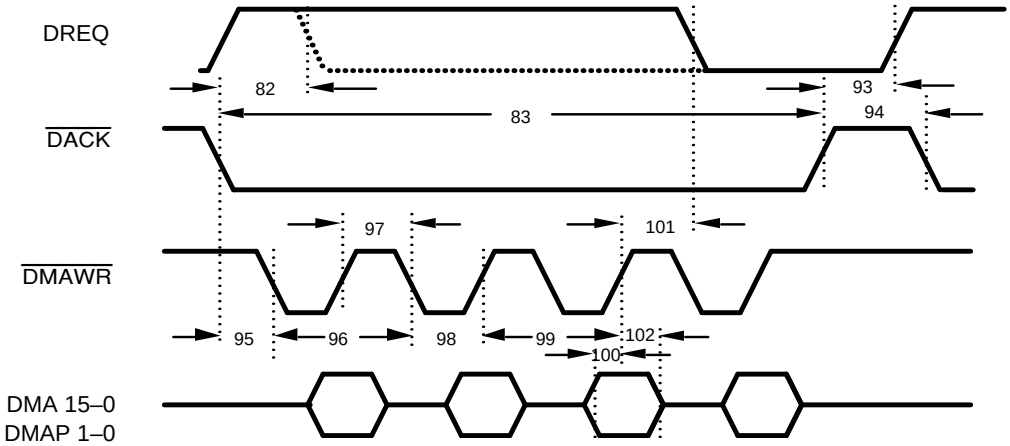
Note:

There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).



16506C-43

Burst DMA Read without Byte Control

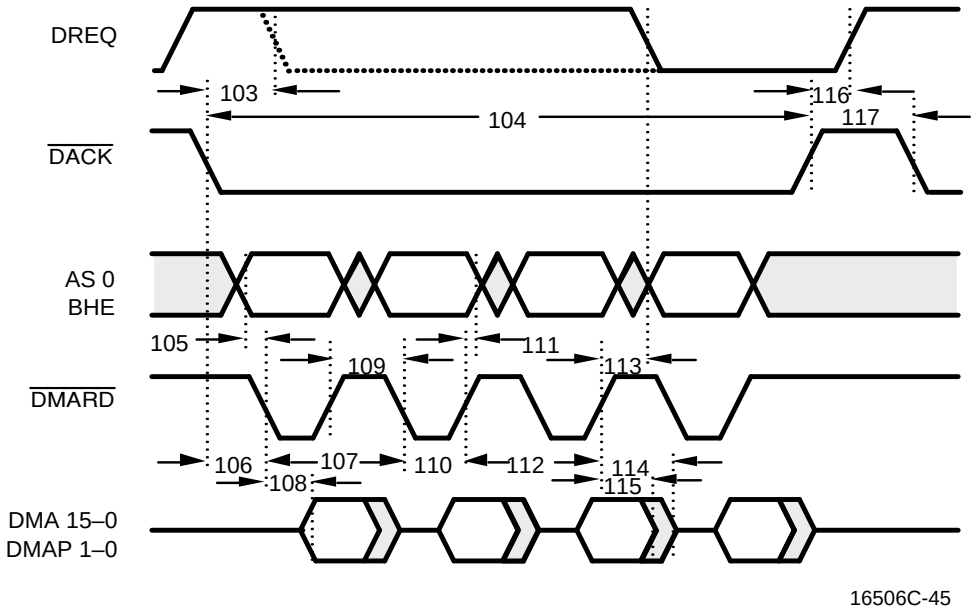


16506C-44

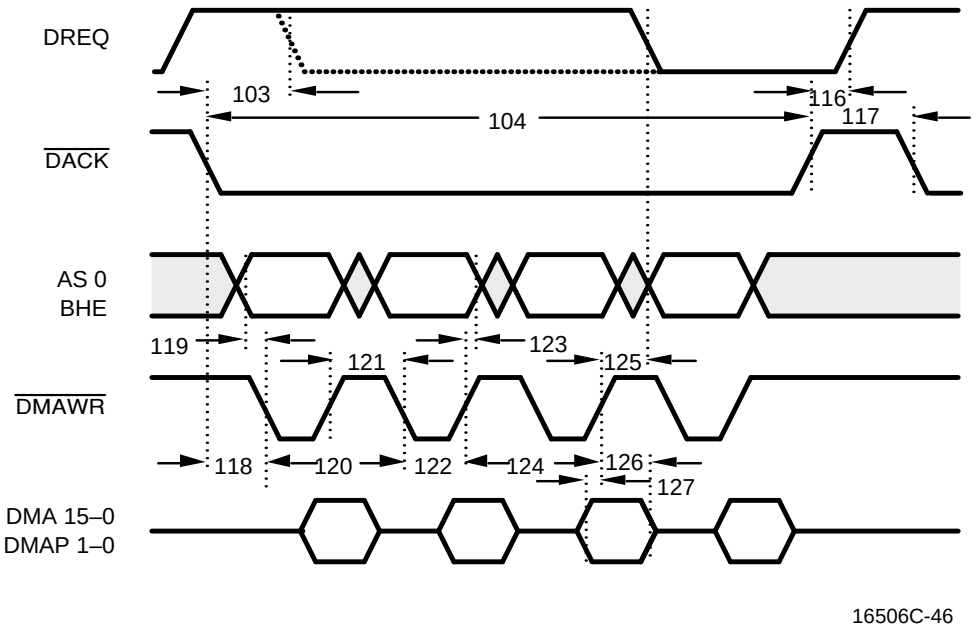
Burst DMA Write without Byte Control

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
82	t_{PD}	$\overline{DACK}$ ↓ to DREQ ↓ Valid Delay			45	ns
83	t_{PWL}	$\overline{DACK}$ Pulse Width Low		100		ns
84	t_S	$\overline{DACK}$ ↓ to $\overline{DMARD}$ ↓ Set Up Time		0		ns
85	t_P	$\overline{DMARD}$ ↓ to $\overline{DMARD}$ ↓ period		130		ns
86	t_{PD}	$\overline{DMARD}$ ↓ to Data Valid Delay			70	ns
87	t_{PWH}	$\overline{DMARD}$ Pulse Width High		60		ns
88	t_{PWL}	$\overline{DMARD}$ Pulse Width Low		70		ns
89	t_P	$\overline{DMARD}$ ↑ to $\overline{DMARD}$ ↑ period		$t_3 + 50$		ns
90	t_{PD}	$\overline{DMARD}$ ↑ to DREQ ↓ Valid Delay			140	ns
91	t_Z	$\overline{DMARD}$ ↑ to Data High Impedance			50	ns
92	t_H	$\overline{DMARD}$ ↑ to Data Hold Time		2		ns
93	t_{PD}	$\overline{DACK}$ ↑ to DREQ ↑ Valid Delay			40	ns
94	t_{PWH}	$\overline{DACK}$ Pulse Width High		60		ns
95	t_S	$\overline{DACK}$ ↓ to $\overline{DMAWR}$ ↓ Set Up Time		0		ns
96	t_P	$\overline{DMAWR}$ ↓ to $\overline{DMAWR}$ ↓ period		160		ns
97	t_{PWH}	$\overline{DMAWR}$ Pulse Width High		60		ns
98	t_{PWL}	$\overline{DMAWR}$ Pulse Width Low		100		ns
99	t_P	$\overline{DMAWR}$ ↑ to $\overline{DMAWR}$ ↑ period		$t_3 + 50$		ns
100	t_S	Data to $\overline{DMAWR}$ ↑ Set Up Time		15		ns
101	t_{PD}	$\overline{DMAWR}$ ↑ to DREQ ↓ Valid Delay			140	ns
102	t_H	Data to $\overline{DMAWR}$ ↑ Hold Time		0		ns

Note:
There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).



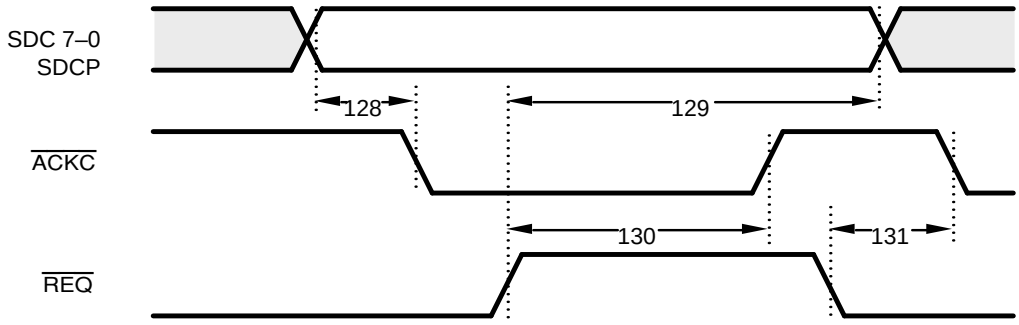
Burst DMA Read with Byte Control



Burst DMA Write with Byte Control

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
103	t_{PD}	$\overline{DACK}$ ↓ to DREQ ↓ Valid Delay			45	ns
104	t_{PWL}	$\overline{DACK}$ Pulse Width Low		100		ns
105	t_S	BHE, AS0 to $\overline{DMARD}$ ↓ Set Up Time		20		ns
106	t_S	$\overline{DACK}$ ↓ to $\overline{DMARD}$ ↓ Set Up Time		0		ns
107	t_P	$\overline{DMARD}$ ↓ to $\overline{DMARD}$ ↓ period		130		ns
108	t_{PD}	$\overline{DMARD}$ ↓ to Data Valid Delay			70	ns
109	t_{PWH}	$\overline{DMARD}$ Pulse Width High		60		ns
110	t_{PWL}	$\overline{DMARD}$ Pulse Width Low		70		ns
111	t_H	BHE, AS0 to $\overline{DMARD}$ ↑ Hold Time		20		ns
112	t_P	$\overline{DMARD}$ ↑ to $\overline{DMARD}$ ↑ period		$t_3 + 50$		ns
113	t_{PD}	$\overline{DMARD}$ ↑ to DREQ ↓ Valid Delay			140	ns
114	t_Z	$\overline{DMARD}$ ↑ to Data High Impedance			50	ns
115	t_H	$\overline{DMARD}$ ↑ to Data Hold Time		2		ns
116	t_{PD}	$\overline{DACK}$ ↑ to DREQ ↑ Valid Delay			50	ns
117	t_{PWH}	$\overline{DACK}$ Pulse Width High		60		ns
118	t_S	$\overline{DACK}$ ↓ to $\overline{DMAWR}$ ↓ Set Up Time		0		ns
119	t_S	BHE, AS0 to $\overline{DMAWR}$ ↓ Set Up Time		20		ns
120	t_P	$\overline{DMAWR}$ ↓ to $\overline{DMAWR}$ ↓ period		160		ns
121	t_{PWH}	$\overline{DMAWR}$ Pulse Width High		60		ns
122	t_{PWL}	$\overline{DMAWR}$ Pulse Width Low		100		ns
123	t_H	BHE, AS0 to $\overline{DMAWR}$ ↑ Hold Time		20		ns
124	t_P	$\overline{DMAWR}$ ↑ to $\overline{DMAWR}$ ↑ period		$t_3 + 50$		ns
125	t_{PD}	$\overline{DMAWR}$ ↑ to DREQ ↓ Valid Delay			140	ns
126	t_H	Data to $\overline{DMAWR}$ ↑ Hold Time		0		ns
127	t_S	Data to $\overline{DMAWR}$ ↑ Set Up Time		15		ns

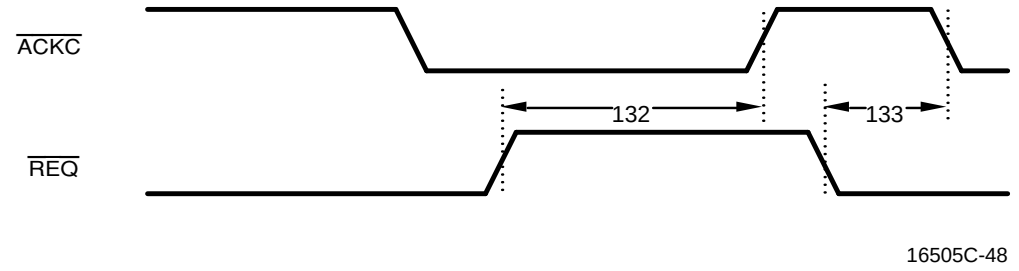
Note:
There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).



16505C-47

Asynchronous Initiator Send

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
128	t_S	Data to $\overline{ACKC}$ ↓ Set Up Time		55		ns
129	t_{PD}	$\overline{REQ}$ ↑ to Data Delay			80	ns
130	t_{PD}	$\overline{REQ}$ ↑ to $\overline{ACKC}$ ↑ Delay			46	ns
131	t_{PD}	$\overline{REQ}$ ↓ to $\overline{ACKC}$ ↓ Delay			55	ns

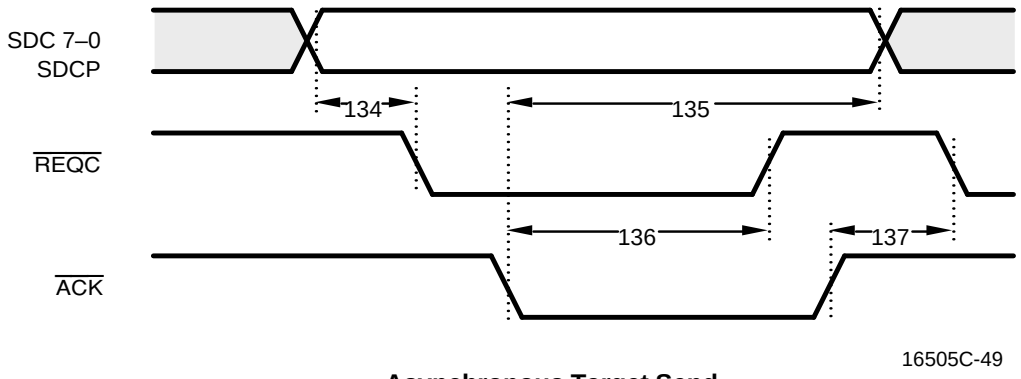


16505C-48

Asynchronous Initiator Receive

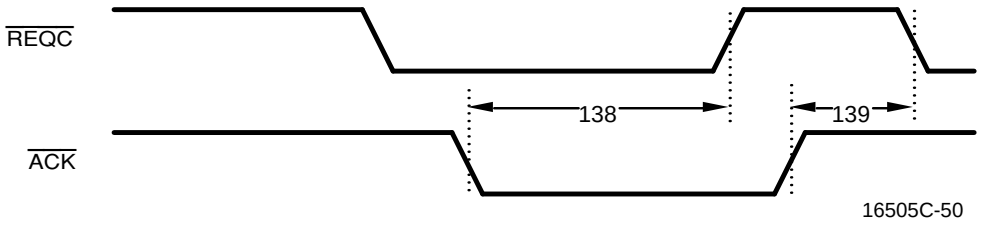
No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
132	t_{PD}	$\overline{REQ}$ ↑ to $\overline{ACKC}$ ↑ Delay			43	ns
133	t_{PD}	$\overline{REQ}$ ↓ to $\overline{ACKC}$ ↓ Delay			47	ns

Note:
There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).



Asynchronous Target Send

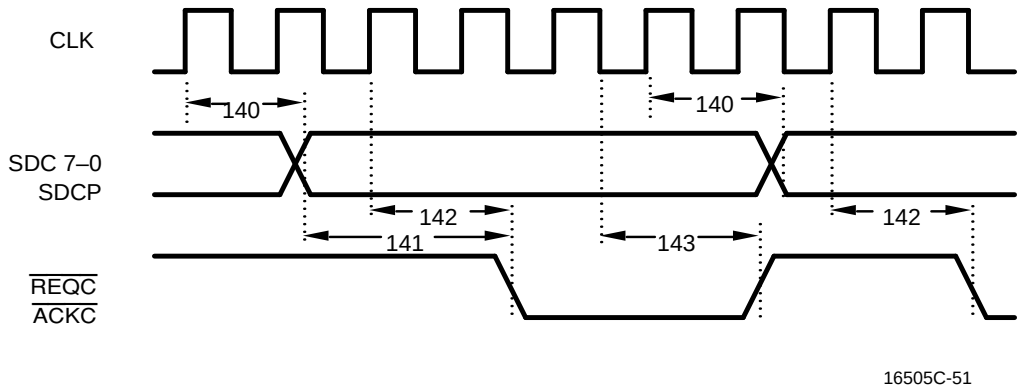
No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
134	t_S	Data to $\overline{REQC}$ ↓ Set Up Time		55		ns
135	t_{PD}	$\overline{ACK}$ ↓ to Data Delay			78	ns
136	t_{PD}	$\overline{ACK}$ ↓ to $\overline{REQC}$ ↑ Delay			60	ns
137	t_{PD}	$\overline{ACK}$ ↑ to $\overline{REQC}$ ↓ Delay			45	ns



Asynchronous Target Receive

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
138	t_{PD}	$\overline{ACK}$ ↓ to $\overline{REQC}$ ↑ Delay			60	ns
139	t_{PD}	$\overline{ACK}$ ↑ to $\overline{REQC}$ ↓ Delay			45	ns

Note:
There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).



Synchronous Initiator Target Transmit

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
140	t_{PD}	CLK ↑ to Data Delay		15*	90	ns
141	t_S	$\overline{ACKC}$ or $\overline{REQC}$ ↓ to Data Set Up Time		55		ns
142	t_{PD}	CLK ↑ to $\overline{ACKC}$ or $\overline{REQC}$ ↓ Delay		13*	68	ns
143	t_{PD}	CLK ↓ to $\overline{ACKC}$ or $\overline{REQC}$ ↑ Delay		17	70	ns

** The minimum values have a wide range since they depend on the Synchronization latency. The synchronization latency, in turn, depends on the operating frequency of the device.*

Note:
There is a one-to-one relationship between every AMD and NCR Parameter (refer to Appendix B).

APPENDIX A
Pin Connection Cross Reference for Am53C94

Pin#	AMD	NCR
1	DMAP0	DBP0
2	V_{SS}	V_{SS}
3	DMA8	DB8
4	DMA9	DB9
5	DMA10	DB10
6	DMA11	DB11
7	DMA12	DB12
8	DMA13	DB13
9	DMA14	DB14
10	DMA15	DB15
11	DMAP1	DBP1
12	$\overline{SD}$0	SDI0/
13	$\overline{SD}$1	SDI1/
14	$\overline{SD}$2	SDI2/
15	$\overline{SD}$3	SDI3/
16	$\overline{SD}$4	SDI4/
17	$\overline{SD}$5	SDI5/
18	$\overline{SD}$6	SDI6/
19	$\overline{SD}$7	SDI7/
20	$\overline{SDP}$	SDIP/
21	V_{DD}	V_{DD}
22	V_{SS}	V_{SS}
23	$\overline{SDC}$0	SDO0/
24	$\overline{SDC}$1	SDO1/
25	$\overline{SDC}$2	SDO2/
26	$\overline{SDC}$3	SDO3/
27	V_{SS}	V_{SS}
28	$\overline{SDC}$4	SDO4/
29	$\overline{SDC}$5	SDO5/
30	$\overline{SDC}$6	SDO6/
31	$\overline{SDC}$7	SDO7/
32	$\overline{SDC}$P	SDOP/
33	V_{SS}	V_{SS}
34	$\overline{SELC}$	SELO/
35	$\overline{BSYC}$	BSYO/
36	$\overline{REQC}$	REQO/
37	$\overline{ACKC}$	ACKO/
38	V_{SS}	V_{SS}
39	$\overline{MSG}$	MSGIO/
40	$\overline{C/D}$	C/DIO
41	$\overline{I/O}$	I/OIO
42	$\overline{ATN}$	ATNIO/

Pin#	AMD	NCR
43	$\overline{RSTC}$	RSTO/
44	V_{SS}	V_{SS}
45	$\overline{SEL}$	SELI/
46	$\overline{BSY}$	BSYI/
47	$\overline{REQ}$	REQI/
48	$\overline{ACK}$	ACKI/
49	$\overline{RST}$	RSTI/
50	BUSMD 1	MODE 1
51	BUSMD 0	MODE 0
52	$\overline{INT}$	INT/
53	RESET	RESET
54	$\overline{WR}$	WR/
55	$\overline{RD}$	RD/
56	$\overline{CS}$	CS/
57	ASO [AO]	A0–SA0
58	BHE [A1]	A1–BHE
59	$\overline{DMARD}$ [A2]	A2–DBRD/
60	ALE [A3]	A3–ALE
61	CLK	CLK
62	V_{DD}	V_{DD}
63	AD0	PAD0
64	AD1	PAD1
65	AD2	PAD2
66	AD3	PAD3
67	V_{SS}	V_{SS}
68	AD4	PAD4
69	AD5	PAD5
70	AD6	PAD6
71	AD7	PAD7
72	DREQ	DREQ
73	$\overline{DACK}$	DACK/
74	$\overline{DMAWR}$	DBWR/
75	V_{SS}	V_{SS}
76	V_{SS}	V_{SS}
77	DMA0	DB0
78	DMA1	DB1
79	DMA2	DB2
80	DMA3	DB3
81	DMA4	DB4
82	DMA5	DB5
83	DMA6	DB6
84	DMA7	DB7

APPENDIX A
Pin Connection Cross Reference for Am53C96

Pin#	AMD	NCR
1	$\overline{\text{DACK}}$	DACK
2	$\overline{\text{DMAWR}}$	DBWR/
3	NC	NC
4	ISEL	IGS
5	V_{SS}	V_{SS}
6	TSEL	TGS
7	V_{SS}	V_{SS}
8	DMA0	DB0
9	DMA1	DB1
10	DMA2	DB2
11	DMA3	DB3
12	DMA4	DB4
13	DMA5	DB5
14	DMA6	DB6
15	DMA7	DB7
16	DMAP0	DBP0
17	V_{SS}	V_{SS}
18	V_{SS}	V_{SS}
19	DMA8	DB8
20	DMA9	DB9
21	DMA10	DB10
22	DMA11	DB11
23	DMA12	DB12
24	DMA13	DB13
25	DMA14	DB14
26	DMA15	DB15
27	DMAP1	DBPI
28	NC	NC
29	$\overline{\text{SD}}0$	SDI0/
30	$\overline{\text{SD}}1$	SDI1/
31	$\overline{\text{SD}}2$	SDI2/
32	$\overline{\text{SD}}3$	SDI3/
33	$\overline{\text{SD}}4$	SDI4/
34	$\overline{\text{SD}}5$	SDI5/
35	$\overline{\text{SD}}6$	SDI6/
36	$\overline{\text{SD}}7$	SDI7/
37	$\overline{\text{SD}}P$	SDIP/
38	V_{DD}	V_{DD}
39	NC	NC
40	V_{SS}	V_{SS}
41	V_{SS}	V_{SS}
42	$\overline{\text{SDC}}0$	SDO0/
43	$\overline{\text{SDC}}1$	SDO1/
44	$\overline{\text{SDC}}2$	SDO2/
45	$\overline{\text{SDC}}3$	SDO3/
46	V_{SS}	V_{SS}
47	V_{SS}	V_{SS}
48	$\overline{\text{SDC}}4$	SDO4/
49	$\overline{\text{SDC}}5$	SDO5/
50	$\overline{\text{SDC}}6$	SDO6/

Pin#	AMD	NCR
51	$\overline{\text{SDC}}$ 7	SDO7/
52	$\overline{\text{SDC}}$ P	SDOP/
53	NC	NC
54	V_{SS}	V_{SS}
55	V_{SS}	V_{SS}
56	$\overline{\text{SELC}}$	SELO/
57	$\overline{\text{BSYC}}$	BSYO/
58	$\overline{\text{REQC}}$	REQO/
59	$\overline{\text{ACKC}}$	ACKO/
60	V_{SS}	V_{SS}
61	V_{SS}	V_{SS}
62	$\overline{\text{MSG}}$	MSGIO/
63	$\overline{\text{C/D}}$	C/DIO
64	$\overline{\text{I/O}}$	I/OIO
65	$\overline{\text{ATN}}$	ATNIO/
66	$\overline{\text{RSTC}}$	RSTO/
67	V_{SS}	V_{SS}
68	V_{SS}	V_{SS}
69	$\overline{\text{SEL}}$	SELI/
70	$\overline{\text{BSY}}$	BSYI/
71	$\overline{\text{REQ}}$	REQI/
72	$\overline{\text{ACK}}$	ACKI/
73	$\overline{\text{RST}}$	RSTI/
74	BUSMD 1	MODE 1
75	BUSMD 0	MODE 0
76	$\overline{\text{INT}}$	INT/
77	RESET	RESET
78	NC	NC
79	$\overline{\text{WR}}$	WR/
80	$\overline{\text{RD}}$	RD/
81	$\overline{\text{CS}}$	CS/
82	ASO [A0]	A0–SAO
83	BHE [A1]	A1–BHE
84	$\overline{\text{DMARD}}$ [A2]	A2–DBRD/
85	ALE [A3]	A3–ALE
86	CLK	CLK
87	$\overline{\text{DFMODE}}$	DIFFM/
88	V_{DD}	V_{DD}
89	NC	NC
90	AD0	PAD0
91	AD1	PAD1
92	AD2	PAD2
93	AD3	PAD3
94	V_{SS}	V_{SS}
95	V_{SS}	V_{SS}
96	AD4	PAD4
97	AD5	PAD5
98	AD6	PAD6
99	AD7	PAD7
100	DREQ	DREQ

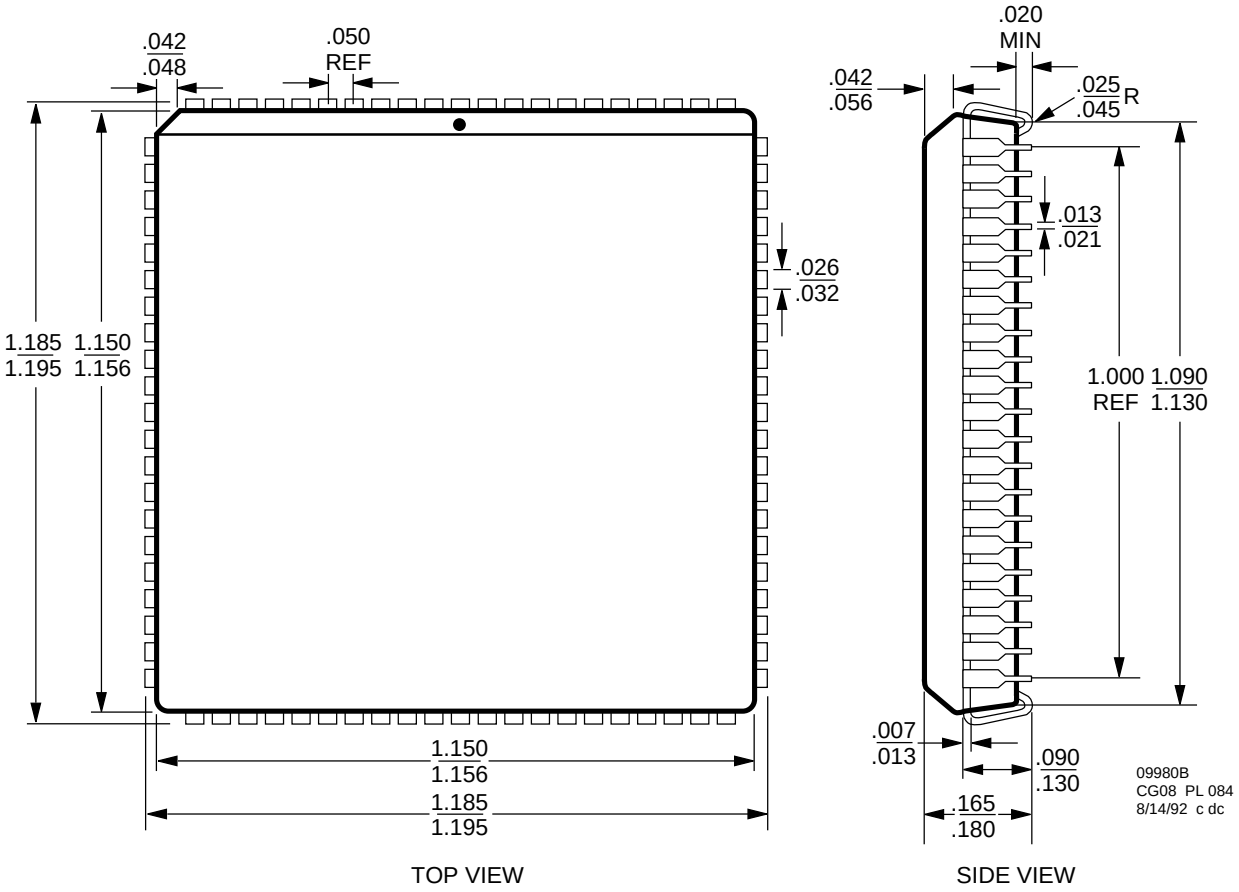
APPENDIX B
AMD/NCR Timing Parameters Cross Reference

NCR Symbol	AMD Parameter #
t_{CH}	4
t_{CL}	1
t_{CP}	2
t_{CS}	3
t_{RST}	5
t_{IR}	6
t_{RD}	8
t_{RI}	7
t_{ICY}	9
t_{RDP1}	10
t_{RDP2}	11
t_{RDP3}	19
t_{RDP4}	13
t_{RDP5}	12
t_{RDP6}	14
t_{RDP7}	16
t_{RDP8}	15
t_{RDP9} (max)	17
t_{RDP9} (min)	18
t_{RDP10}	20
t_{RDP11}	21
t_{RDP12}	23
t_{RDP13}	22
t_{RDP14}	26
t_{RDP15}	24
t_{RDP16}	25
t_{RMP1}	28
t_{RMP2}	29
t_{RMP3}	27
t_{RMP4}	30
t_{RMP5}	31
t_{RMP6}	38
t_{RMP7}	32
t_{RMP8}	34
t_{RMP9}	36
t_{RMP10}	33
t_{RMP11} (max)	37
t_{RMP11} (min)	35
t_{RMP12}	39
t_{RMP13}	40
t_{RMP14}	44
t_{RMP15}	41
t_{RMP16}	43
t_{RMP17}	42
t_{DNB1}	45
t_{DNB2}	49
t_{DNB3}	51
t_{DNB4}	47

NCR Symbol	AMD Parameter #
t_{DNB5}	46
t_{DNB6}	50
t_{DNB7}	48
t_{DNB8} (max)	52
t_{DNB8} (min)	53
t_{DNB9}	54
t_{DNB10}	55
t_{DNB11}	57
t_{DNB12}	56
t_{DNB13}	59
t_{DNB14}	58
t_{DBC1}	60
t_{DBC2}	71
t_{DBC3}	73
t_{DBC4}	62
t_{DBC5}	61
t_{DBC6}	72
t_{DBC7}	64
t_{DBC8}	67
t_{DBC9}	63
t_{DBC10}	65
t_{DBC11}	68
t_{DBC12}	66
t_{DBC13} (max)	69
t_{DBC13} (min)	70
t_{DBC14}	75
t_{DBC15}	78
t_{DBC16}	74
t_{DBC17}	76
t_{DBC18}	79
t_{DBC19}	77
t_{DBC20}	81
t_{DBC21}	80
t_{DAN1}	93
t_{DAN2}	82
t_{DAN3}	94
t_{DAN4}	83
t_{DAN5}	90
t_{DAN6}	84
t_{DAN7}	88
t_{DAN8}	87
t_{DAN9}	86
t_{DAN10} (max)	91
t_{DAN10} (min)	92
t_{DAN11}	85
t_{DAN12}	89
t_{DAN13}	101
t_{DAN14}	95

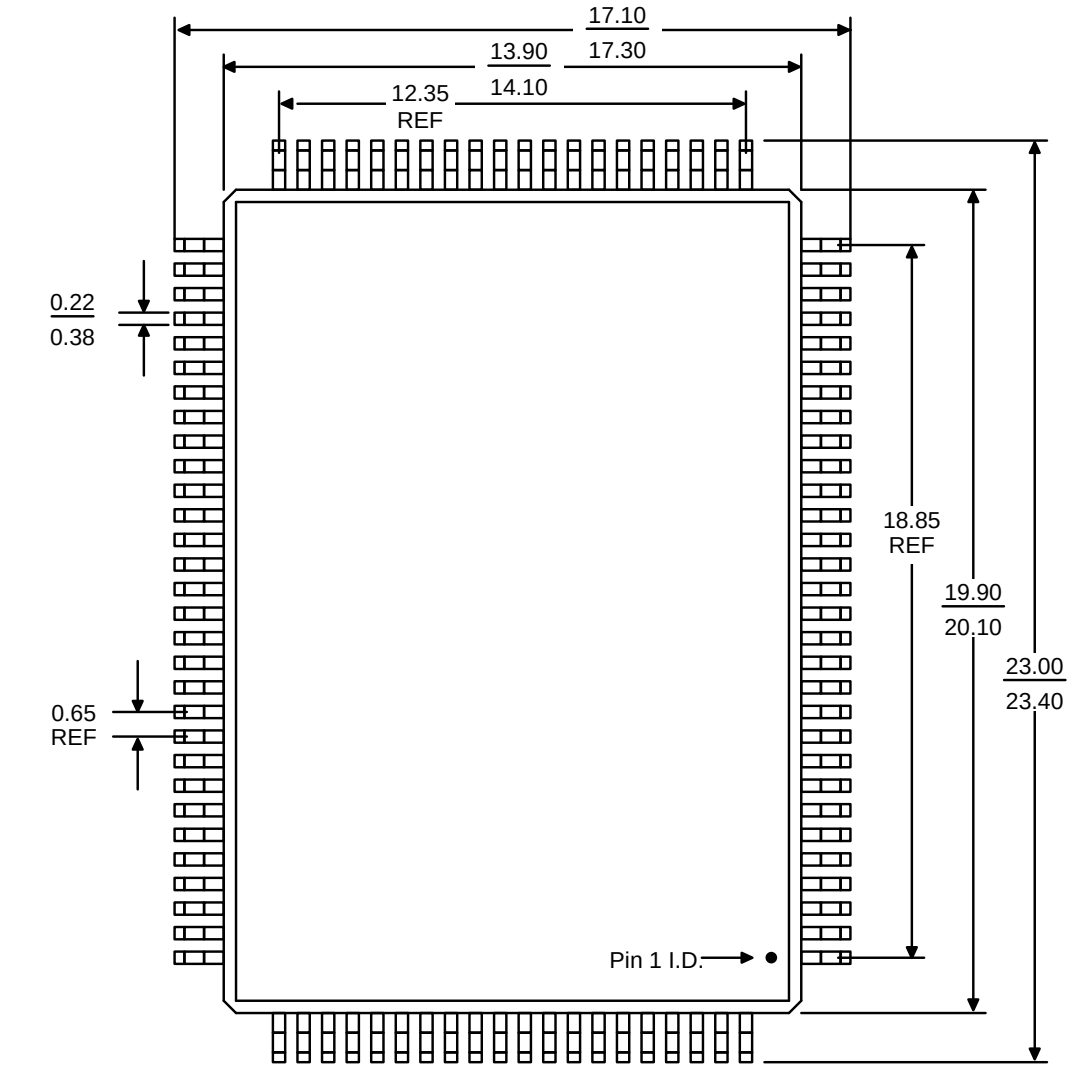
NCR Symbol	AMD Parameter #
t_{DAN15}	98
t_{DAN16}	97
t_{DAN17}	100
t_{DAN18}	102
t_{DAN19}	96
t_{DAN20}	99
t_{DAB1}	116
t_{DAB2}	103
t_{DAB3}	117
t_{DAB4}	104
t_{DAB5}	113
t_{DAB6}	105
t_{DAB7}	111
t_{DAB8}	106
t_{DAB9}	110
t_{DAB10}	109
t_{DAB11}	108
t_{DAB12} (max)	114
t_{DAB12} (min)	115
t_{DAB13}	107
t_{DAB14}	112
t_{DAB15}	125
t_{DAB16}	119
t_{DAB17}	123
t_{DAB18}	118
t_{DAB19}	122
t_{DAB20}	121
t_{DAB21}	127
t_{DAB22}	126
t_{DAB23}	120
t_{DAB24}	124
t_{LAXDA}	128
t_{LAXAH}	130
t_{LAXRD}	129
t_{LAXAL}	131
t_{LARAH}	132
t_{LARAL}	133
t_{TAXDR}	134
t_{TAXRH}	136
t_{TAXAD}	135
t_{TAXRL}	137
t_{TARRH}	138
t_{TARRL}	139
t_{SXD}	140
t_{SXRAL}	142
t_{SXRAH}	143
t_{SXDSU}	141

PHYSICAL DIMENSIONS*
PL 084
Plastic Leaded Chip Carrier (measured in inches)

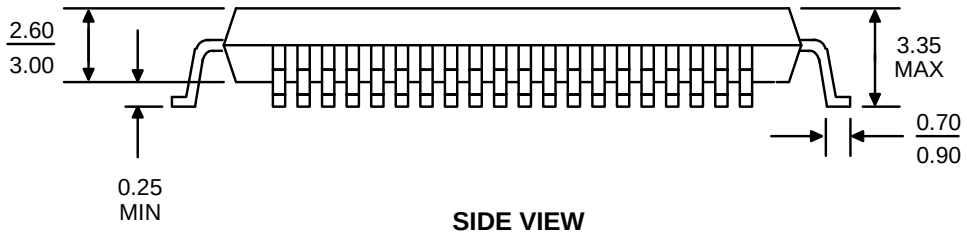


** For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS*
PQR100
Plastic Quad Flatpack Trimmed and Formed (measured in millimeters)



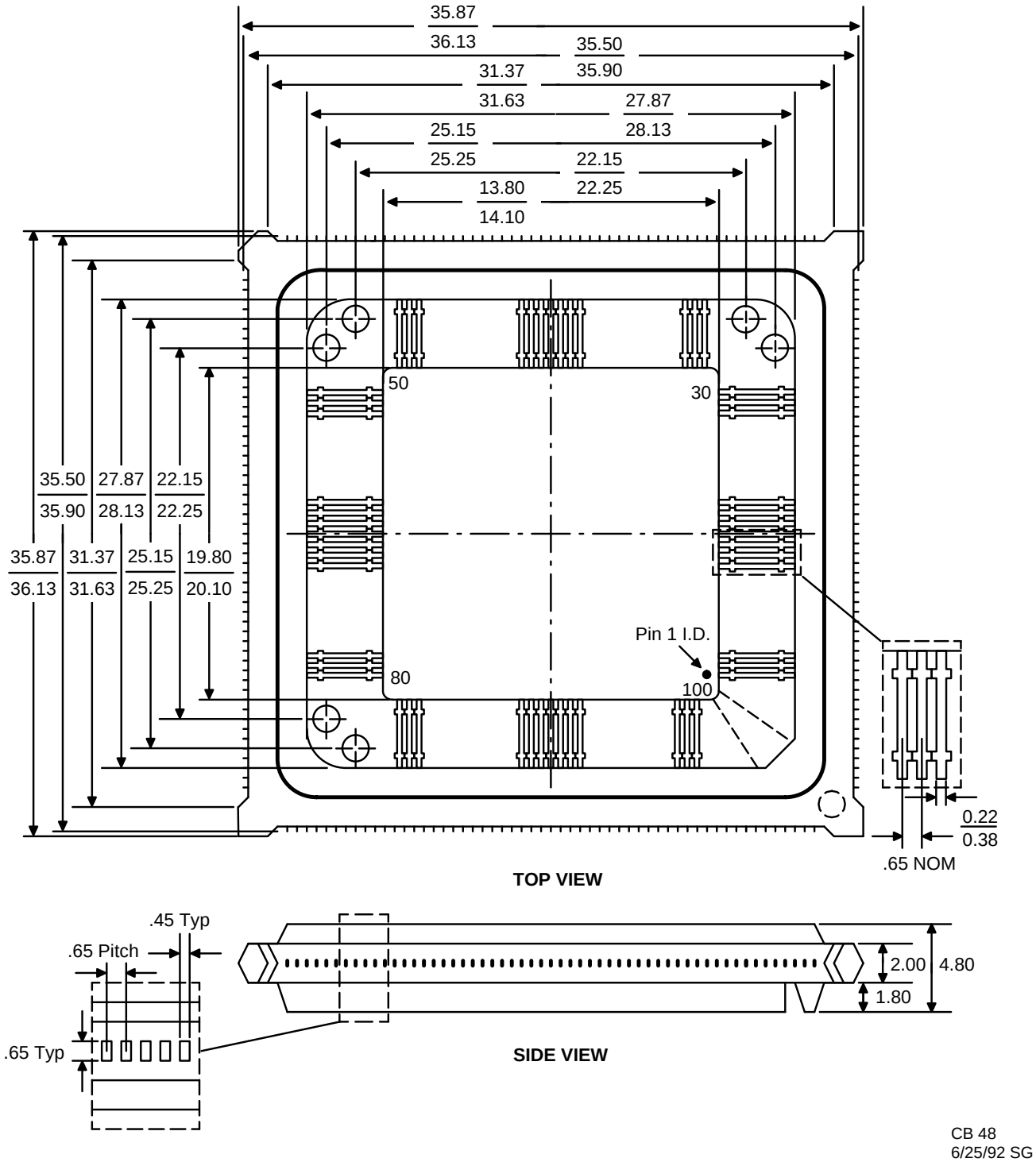
TOP VIEW



SIDE VIEW

15590D
BX 45
9/6/91 SG

PHYSICAL DIMENSIONS*
PQR100
Molded Carrier Ring Plastic Quad Flatpack (measured in millimeters)



CB 48
6/25/92 SG

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