VITESSE

VSC7145
Datasheet

Dual Speed 10-Bit Serializer/Deserializer for Fibre Channel, Gigabit Ethernet, and InfiniBand™

FEATURES

- Dual Speed Operation
  - 1.0625Gb/s / 2.125Gb/s for Fibre Channel
  - 1.25Gb/s for Gigabit Ethernet
  - 2.5Gb/s for InfiniBand
- 10-Bit, SSTL_2/SSTL_3 Interface at up to 250MHz, HSPI Interface Compatible
- ASIC-Friendly™ Timing to the Transmitter
- Separate Transmitter/Receiver Rate Control
- On-Chip Termination Resistors
- Write Pre-Emphasis
- Cable Equalization in Receiver
- Analog/Digital Signal Detection
- SSTL_2/SSTL_3/LVTTL/PECL REFCLK
- Single 3.3V Supply, 900mW Typical
- 64-Pin, 14mm PQFP Package

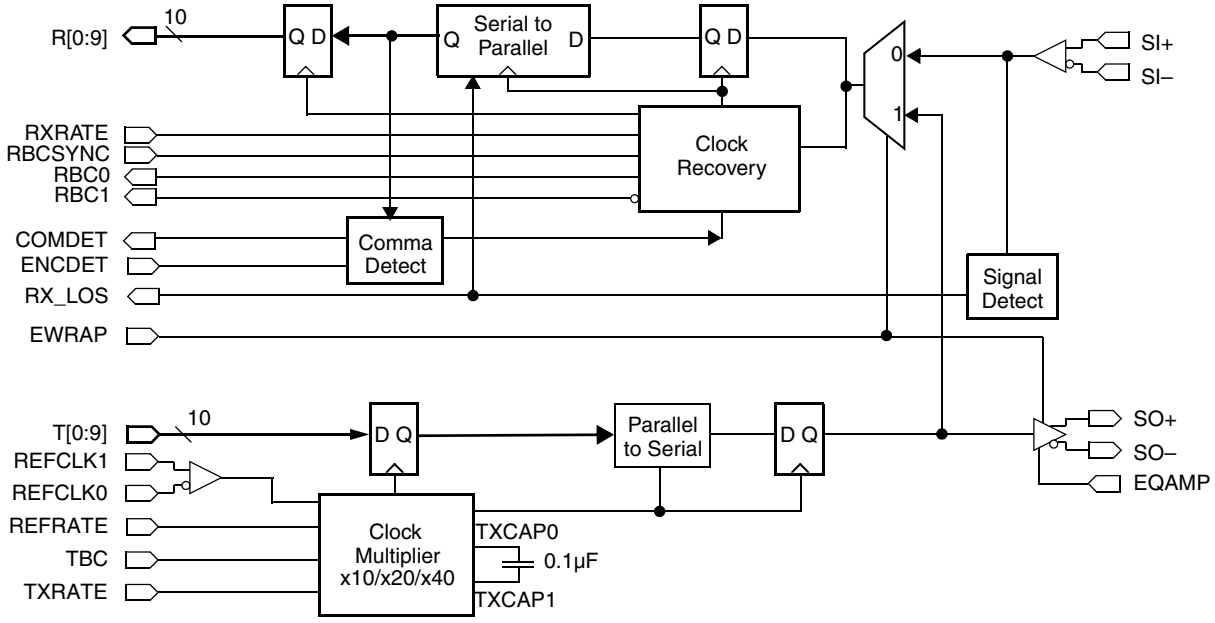
APPLICATIONS

- Fibre Channel
  - Host Adapters
  - Hubs/Switches
  - RAID Systems
- Gigabit Ethernet
  - NICs
  - Switches
  - Proprietary Uplinks
- InfiniBand
  - Host Channel Adapters
  - Target Channel Adapters
  - Switches
- Proprietary Serial Links

GENERAL DESCRIPTION

The VSC7145 is a dual-speed Fibre Channel, Gigabit Ethernet, and InfiniBand Serializer/Deserializer (SerDes) optimized for performance and power in an industry-standard pinout. The VSC7145 accepts 10-bits of Stub-Series Terminated Logic (SSTL), 8B/10B encoded transmit data, latches it synchronously to the Transmit Byte Clock (TBC) and serializes it onto the SO differential output at a baud rate, which is 10, 20, or 40 times the REFCLK frequency. The VSC7145 samples serial receive data on the SI input, recovers the clock and data, de-serializes it onto a 10-bit SSTL bus, and generates two recovered clocks at $1/10^{th}$ or $1/20^{th}$ of the baud rate. Both disparities of the K28.5 characters are detected and used for aligning the serial data to the parallel output bus. Independent speed selectors control the transmitter and receiver separately to support industry-standard Automatic Speed Negotiation protocols. A combined analog/digital signal detect circuit indicates the presence of valid signal levels on the SI input. The VSC7145 contains on-chip (Phase Lock Loop) PLL circuitry for synthesis of the bit rate transmit clock and extraction of the clock from the received serial stream. The parallel bus of the VSC7145 is compatible with the High-Speed Parallel Interface (HSPI) standard developed by the T11.2 Fibre Channel Committee. Refer to the application note, *VSC7145 Compliance to the High-Speed Parallel Interface (HSPI)* for more information.

Functional Block Diagram



Product Options

Three configurations of the device are available and are identified by the part number suffix (for example, -30).

Part Number	Low-Speed I/O	Speed (Gb/s)	High-Speed Termination	Compatibility
VSC7145-30	SSTL_2	1.05 to 1.26 (half speed) or 2.10 to 2.52 (full speed)	100Ω	Agilent HDMP-2630
VSC7145-31	SSTL_3	1.05 to 1.26 (half speed) or 2.10 to 2.52 (full speed)	100Ω	Agilent HDMP-2631
VSC7145-34	SSTL_2	1.05 to 1.26 (half speed) or 2.10 to 2.52 (full speed)	100Ω	Agilent HDMP-2634

If SSTL_2 is required, either the -30 or -34 version of the part should be ordered. If SSTL_3 is required, then the -31 version of the part should be ordered (see "Ordering Information" on page 22). The on-chip differential impedance of these three parts is 100Ω.

These three parts are compatible with the Agilent HDMP-263x devices (as shown above) but dissipate less than half of the power. Unlike the Agilent devices, all versions of the VSC7145 operate from 1.05Gb/s to 1.26Gb/s (half-speed mode) and from 2.10Gb/s to 2.52Gb/s (full-speed mode), which allows single chips to support multiple applications such as Fibre Channel, Gigabit Ethernet, and InfiniBand.

FUNCTIONAL DESCRIPTION

Clock Multiplier Unit

The VSC7145 Clock Multiplier Unit (CMU) multiplies the reference frequency provided on the single-ended/differential REFCLK pin(s) by 20 (if REFRATE is LOW) or 40 (if REFRATE is HIGH) to generate an internal clock between 2.10GHz and 2.52GHz. For example in Fibre Channel, a 53.125MHz REFCLK can be used if REFRATE is HIGH or a 106.25 MHz REFCLK can be used if REFRATE is LOW. The "REFCLK" signal can be either SSTL, LVTTL, or LVPECL and single-ended or differential. If single-ended or LVTTL, connect the input clock to REFCLK1 and leave REFCLK0 open. If SSTL, connect the input clock to REFCLK1 and connect RFCLK0 to VREFT. If LVPECL, connect the inputs to both REFCLK1 and REFCLK0. Internally, the input's buffer pins are biased to VREFT, which is nominally 1.25V (VSC7145-30 and VSC7145-34) or 1.50V (VSC7145-31), if left unconnected, or can be driven externally by the user for better matching to the I/O type. The on-chip clock multiplier's PLL requires a single 0.1µF capacitor to be connected between TXCAP0 and TXCAP1 to set the loop filter characteristics. Using a NPO capacitor is preferred, however, X7R may be acceptable.

Since REFCLK is used to generate the internal baud rate clocks that affect SO jitter generation and SI jitter tolerance, it is important that noise and jitter be reduced on this input in order to optimize signal quality.

Serializer

The VSC7145 accepts SSTL input data as a parallel 10-bit character on the T[0:9] bus, which is latched into the input register synchronously to TBC. TBC must be derived from the same source as REFCLK although no phase relationship is assumed. It is assumed that TBC will be generated by a PLL on an ASIC and derived from the same clock source as REFCLK. Therefore, TBC will contain jitter (due to PLL noise, power supply noise, and rise/fall time mismatch) and wander (due to thermal drift). Special circuitry is contained in the serializer in order to use TBC as a FIFO clock and tolerate TBC jitter/wander, which results in extremely low jitter transfer from TBC to REFCLK.

When TXRATE is HIGH for full-speed operation, the timing of this bus is ASIC-Friendly, meaning that TBC and T[0:9] data are generated together in the protocol device in order to facilitate compliance with setup and hold timing. This ASIC-Friendly timing scheme allows the TBC clock to be easily generated by the protocol controller, which can treat it as a toggling 11^{th} data bit. When TXRATE is LOW, the transmitter runs at half speed and data is latched with the falling edge of TBC.

This data will be serialized and transmitted on the SO± differential outputs at a bit rate that is 10, 20, or 40 times the frequency of the REFCLK, as determined by TXRATE and REFRATE, with bit T0 transmitted first. The SO outputs must be AC-coupled to the link. User data should be encoded using 8B/10B block code or an equivalent, run-length-limited, DC-balanced code. An encoded byte is 10 bits and is referred to as a transmission character. The 10-bit interface on the VSC7145 corresponds to a transmission character. This mapping is illustrated in Table 1.

Table 1. Transmission Order and Mapping of an 8B/10B Character

Parallel Data Bits	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
8B/10B Bit Position	j	h	g	f	i	e	d	c	b	a
K28.5-Character	0	1	0	1	1	1	1	1	0	0

Last Data Bit Transmitted — First Data Bit Transmitted

The SO differential output, formed by SO+/SO–, has two modes of operation:

- when EWRAP is HIGH, the output of the serializer is multiplexed internally to the receiver and the SO output is HIGH (SO+ = HIGH, SO– = LOW)
- when EWRAP is LOW, the output of the serializer is transmitted on the SO output.

Pre-Emphasis

In order to compensate for long copper traces, the VSC7145 contains an optional mode to decrease the rise/fall time of narrow pulses, which tends to improve jitter at the receivers at the far end of the trace. When EQAMP is HIGH, pre-emphasis is disabled. When EQAMP is LOW, pre-emphasis is enabled. Pre-Emphasis may increase the jitter measured near the SO outputs but will reduce jitter at the receiver on longer traces.

Transmitter Bus Timing

Full-Speed Operation ASIC-Friendly Timing

As an example, for 2.5Gb/s operation with TBC = 125MHz and TXRATE is HIGH, the transmitter operates in full-speed mode. Transmitted data is generated synchronously to each rising/falling edge of TBC. An internal PLL generates a clock to latch T[0:9] midway between TBC edges. The internal clock uses both the rising and falling edges of TBC to align the internal clock at the optimal location in the cycle for latching the data.

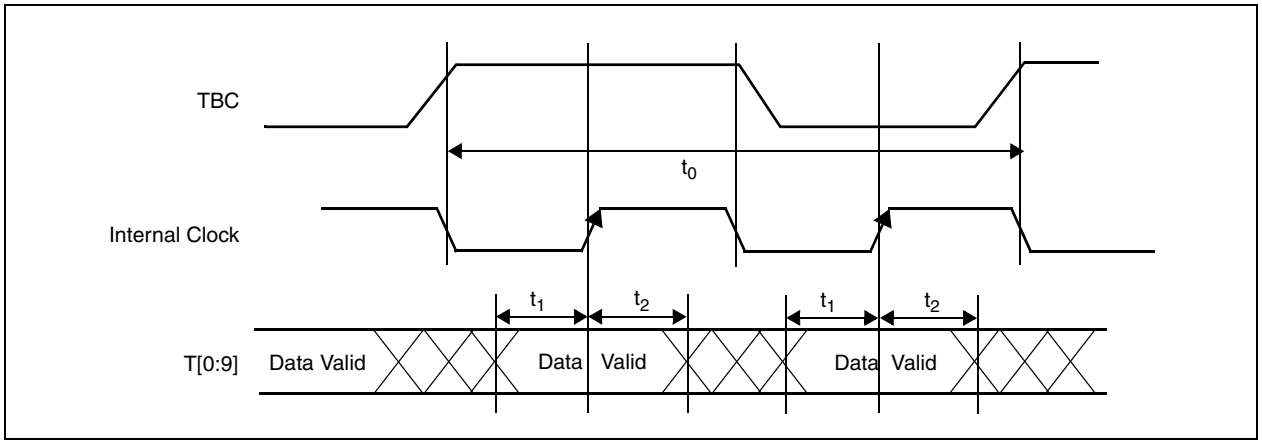


Figure 1. ASIC-Friendly Transmit Timing Waveforms (TXRATE = HIGH)

Table 2. Transmit AC Characteristics (TXRATE = HIGH)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_1	T[0:9] setup time before the mid-point between TBC edges	600	250		ps	2.5Gb/s operation.
		600	250		ps	2.12Gb/s operation.
t_2	T[0:9] hold time after the mid-point between TBC edges	600	450		ps	2.5Gb/s operation.
		600	330		ps	2.12Gb/s operation.

Half-Speed Operation

If TXRATE is LOW, the transmitter operates in half-speed mode even though the clock synthesizer still operates at full-speed. During half-speed operation the transmitted data is sampled on the falling edges of TBC. An internal digital PLL lines up an internal clock to latch T[0:9] with the falling edges of TBC.

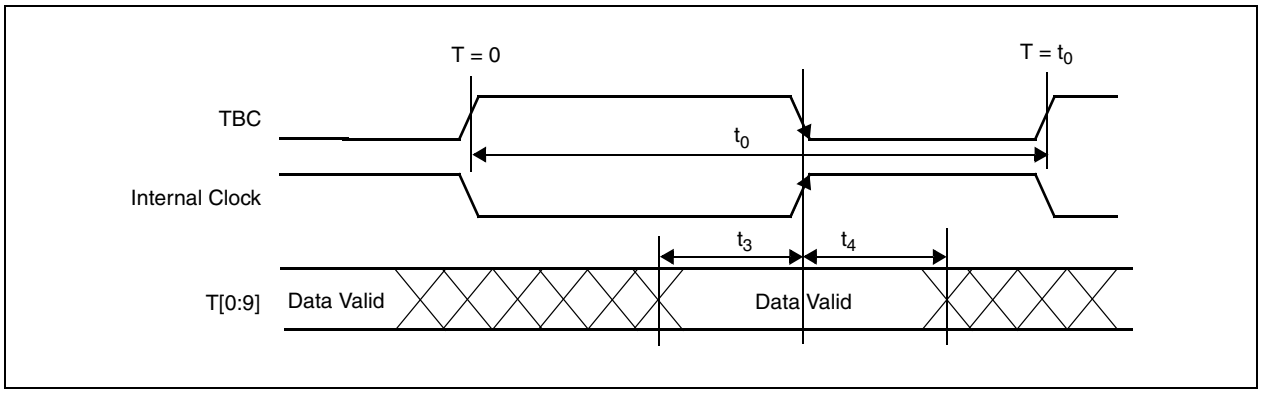


Figure 2. Transmit Timing Waveform (TXRATE = LOW)

Table 3. Transmit AC Characteristics (TXRATE = LOW)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_3	T[0:9] setup time before the falling edge of TBC	600	250		ps	TXRATE = LOW.
t_4	T[0:9] hold time after the falling edge of TBC	600	250		ps	TXRATE = LOW.

Table 4. Transmit AC Characteristics (regardless of TXRATE)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_0	TBC frequency	105		126	MHz	TBC is frequency-locked to REFCLK.
t_0	TBC clock period	7.93		9.53	ns	
t_R,t_F	SO+/SO– rise and fall time	75		175	ps	20% to 80%. Pre-emphasis off.
t_{LAT}	Latency from T[0:9] to T0 appearing on SO	10		30	bc	bc = bit clock.
t_J	Total SO± output jitter (peak-to-peak)			120	ps	REFRATE = 0.
				160		REFRATE = 1.
t_{DJ}	SO± deterministic jitter (peak-to-peak)			40	ps	

Serial Input Buffer

The SI± inputs connect to a high-speed differential input buffer that receives incoming serial data. The VSC7145 contains a differential termination resistor between SI+ and SI– to optimally match the transmission line characteristics of the media. AC-coupling capacitors are located between this resistor and the input buffer in order to allow DC-coupling of the SI± inputs for all DC-coupled applications such as InfiniBand. The output of the SI input buffer connects to a multiplexer, which connects to the Clock Recovery Unit (CRU).

Clock Recovery

The CRU accepts differential high-speed serial input on SI+/SI– (when EWRAP is LOW) or from the transmitter (when EWRAP is HIGH), extracts the clock and retimes the data. A cable equalizer is included in the SI input buffer to open the data eye and compensate for InterSymbol Interference (ISI) that may be present due to long cable or traces. The CRU operates at full speed (2.10Gb/s to 2.52Gb/s) if RXRATE is HIGH or half speed (1.05Gb/s to 1.26Gb/s) if RXRATE is LOW.

The serial bit stream should be encoded so as to provide DC balance and limited run length by an 8B/10B (or equivalent) encoding scheme. For proper operation, the baud rate of the data stream to be recovered should be within ±200ppm of the internal baud rate of the transmitter. For example, if the REFCLK used is 125MHz, then the incoming serial baud rate must be 1.25 giga baud ±200ppm, which allows the use of cost effective ±100ppm oscillators on each side of the link.

Deserializer

The recovered data is then deserialized onto the 10-bit SSTL Class I bus along with complementary recovered clocks that are divided versions of the recovered bit clock. Data bit R0 is received prior to R1 and so forth. RXRATE and RBCSYNC determine the speed of the recovered clock, RBC0/RBC1, and its timing relationship to data R[0:9] as shown in Table 5.

Table 5. Receiver Operation (example for 1.25Gb/s to 2.5Gb/s speeds)

RXRATE	RBCSYNC	SI Input Rate	RBC Rate	Comments
0	0	1.25	62.5	Half-speed mode, RBC0/1 rising edge in middle of R[0:9]
0	1	1.25	125	Half-speed mode, RBC1 rising edge lined up with R[0:9]
1	0	2.5	125	Full-speed mode, RBC0/1 rising edge in middle of R[0:9]
1	1	2.5	125	Full-speed mode, RBC1 rising and falling edges lined up with R[0:9]

Signal Detection

The VSC7145 receiver has an output, RX_LOS, which indicates (when LOW) that the SI input contains a valid signal. A combination of one analog and two digital checks are used to determine if the incoming signal contains valid data.

- **Transition Detection**. Analog transition detection is performed on the SI input to verify that the signal swings are of adequate amplitude. The SI input buffer contains a differential voltage comparator that will go LOW if the differential peak-to-peak amplitude is greater than 200mV or HIGH if under 80mV. If the amplitude is between 80mV and 200mV, the output is indeterminate. This check is always enabled.
- **RLL Checking.** The incoming serial data on SI is monitored for a run length violation. Normally 8B/10B encoded data will not contain more than five consecutive 1s or 0s. If the input data contains six or more consecutive 1s or 0s, the signal is determined to be invalid. If EWRAP is HIGH, this check is ignored because internal data is not coming from SI.
- **K28.5 Checking.** The incoming serial data on SI is monitored for both disparities of K28.5 (0011111010 and 1100000101), regardless of the state of ENCDET. For Fibre Channel, Gigabit Ethernet, and InfiniBand, valid data will contain a K28.5 character during any 2^{17} bit period. A 17-bit counter, called the K28.5 Density Checker, is reset to a count of zero upon the detection of a K28.5 character. The counter begins counting until it is either reset again by the occurrence of another K28.5 or the counter overflows and stops if a K28.5 character does not occur within 2^{17} bits. If EWRAP is HIGH, this check is ignored because internal data is not coming from SI.

RX_LOS is an asynchronous output and will be asserted (LOW) when all of the following conditions have been met:

- During the previous 40-bit period, SI must have been of sufficient amplitude to trigger the Transition Detection circuitry.
- If EWRAP is LOW, during the previous 40-bit period, a Run Length violation must not have occurred.
- If EWRAP is LOW, during the previous 40-bit period, the K28.5 Density Check counter should not be in an overflow condition (indicating that at least 2^{17} bits have occurred without the detection of a K28.5 character).

If any of the criteria above is not met, RX_LOS will go HIGH.

NOTE: *It is not recommended to use RX_LOS as a speed-detection circuit. The user should monitor recovered data on R[0:9] instead.*

Table 6. Signal Detect Behavior

EWRAP	Transition Detect	RLL Violation	K28.5 Density	Mode
0	Enabled	Enabled	Enabled	Normal Operation
1	Enabled	Disabled	Disabled	Loopback

Word Alignment

The VSC7145 provides 10-bit K28.5 (comma) character recognition and data word alignment. Word alignment is enabled by asserting ENCDET HIGH. When enabled, the receiver examines the recovered serial data for the presence of the K28.5 character, both 0011111010 and 1100000101, where the left-most bit corresponds to the first bit received. Improper alignment of the K28.5 character is defined as any of the following conditions:

- The K28.5 straddles the boundary between two 10-bit transmission characters.
- The K28.5 is properly aligned but occurs in the received character presented during the wrong edge of RBC0/RBC1.

When ENCDET is HIGH and an improperly-aligned K28.5 is encountered, the recovered clock is stretched so that the K28.5 character and recovered clocks are aligned properly to R[0:9] and RBC0/RBC1. During realignment, some data (and possibly the first K28.5) may be lost. However, the second K28.5 character and subsequent data will be output correctly and properly aligned. When ENCDET is LOW, the current alignment of the serial data is maintained indefinitely, regardless of the data pattern.

Figure 3a shows the typical process of the received serial bit stream deserialized and after the latency time of RLAT, appears at R[0:9]. In this case, RBCSYNC is HIGH causing RBC to be edge-aligned with the data. Figure 3b shows the case where the ENCDET signal has been asserted and an improperly aligned K28.5 is encountered straddling the boundary between two transmission characters. R[0:9] data and RBC clocks are stretched to allow for proper alignment of the K28.5 character in the deserializer. After the period RLAT, the properly aligned data appears at the outputs. It also shows the alignment of the COMDET pulse, where RBCSYNC is HIGH, in relation to the K28.5 character on R[0:9] and the RBC signal.

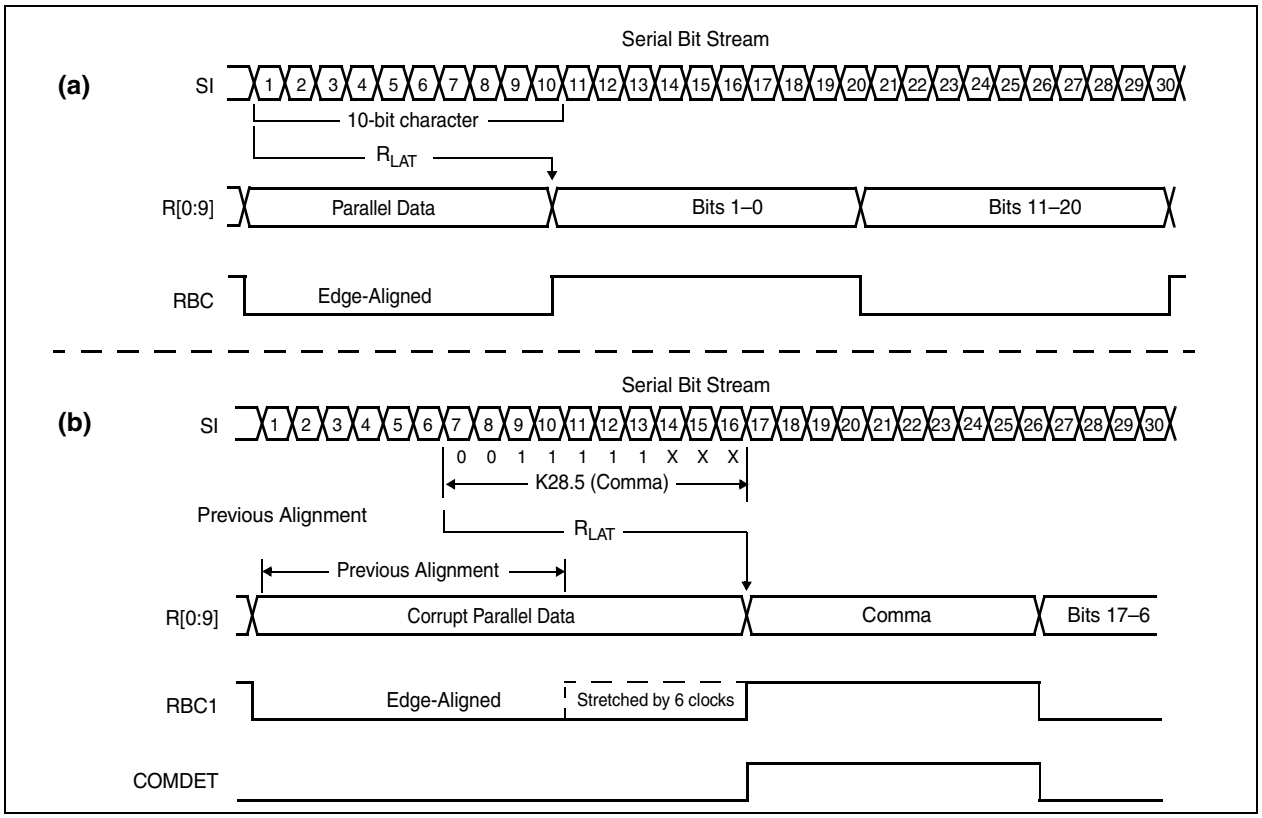


Figure 3. Aligned and Misaligned K28.5 Characters (ENCDET = HIGH, RBCSYNC = HIGH)

Table 7. VSC7145 Configuration for Fibre Channel

Signal	1x Mode	2x Mode	Comments
REFCLK	106.25MHz 53.125MHz		REFRATE = 0 REFRATE = 1
TBC	106.25MHz	106.25MHz	Frequency locked to REFCLK
T[0:9]	106.25Mb/s	212.5Mb/s	Controlled by TXRATE
RBC0/1	106.25MHz or 53.125MHz	106.25MHz 106.25MHz	RBCSYNC = HIGH RBCSYNC = LOW
R[0:9]	106.25Mb/s	212.5Mb/s	Controlled by RXRATE

Table 8. VSC7145 Configuration for Gigabit Ethernet (1x mode) and InfiniBand (2x mode)

Signal	1x Mode	2x Mode	Comments
REFCLK	125MHz 62.5MHz		REFRATE = 0 REFRATE = 1
TBC	125MHz	125MHz	Frequency locked to REFCLK
T[0:9]	125Mb/s	250Mb/s	Controlled by TXRATE
RBC0/1	125MHz or 62.5MHz	125MHz 125MHz	RBCSYNC = HIGH RBCSYNC = LOW
R[0:9]	125Mb/s	250Mb/s	Controlled by RXRATE

Receive Bus Operation

Case A: Receive Bus Operation (RXRATE = LOW, RBCSYNC = LOW)

When RXRATE is LOW and RBCSYNC is LOW, the deserializer runs at half speed (1.06Gb/s or 1.25Gb/s). The RBC0/RBC1 clocks run at 1/20th of the baud rate (53.125MHz or 62.5MHz), and the rising edges of RBC0 and RBC1 are located in the middle of the R[0:9] valid period. This mode is the normal mode for half-speed operation and is compatible with the 10-bit interface specification for Fibre Channel and Gigabit Ethernet.

If ENCDET is HIGH, the RBC clocks will be stretched up to 19 bits in order to align incoming serial data with the parallel bus as indicated by the K28.5 detector. COMDET will always be centered on the rising edge of RBC1.

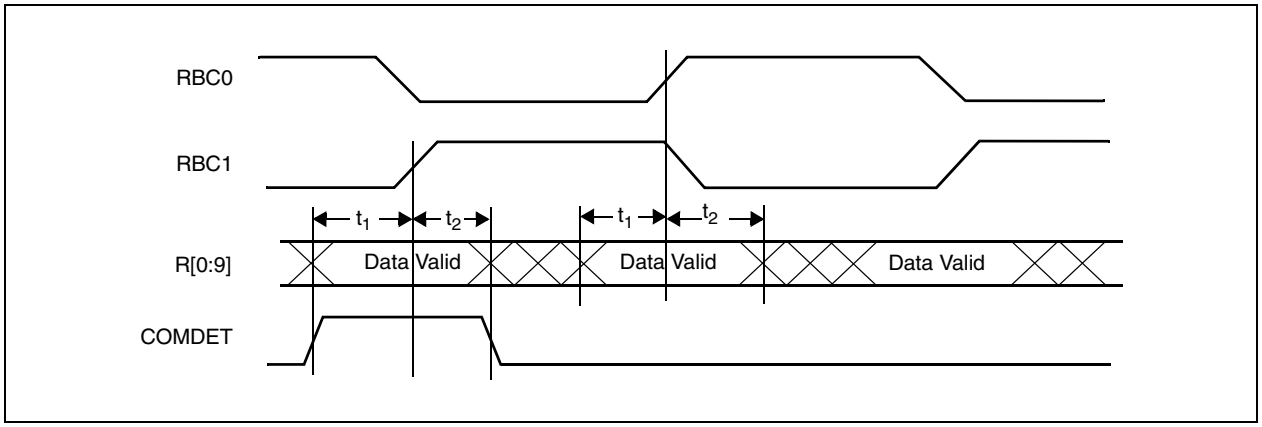


Figure 4. Receive Timing Waveforms (RXRATE = 0, RBCSYNC = 0)

Table 9. Receive AC Characteristics (RXRATE = 0, RBCSYNC = 0)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_1	R[0:9], COMDET valid prior to RBC0/RBC1 rising edge	3.0	3.9		ns	1.25Gb/s operation.
		3.0	4.5		ns	1.06Gb/s operation.
t_2	R[0:9], COMDET valid after RBC0 or RBC1 rising edge	2.0	3.5		ns	1.25Gb/s operation.
		2.0	4.5		ns	1.06Gb/s operation.
R_{LAT}	Latency from Rx to R[0:9]		40bc + 5ns		bc ns	bc = bit clock.

Case B: Receive Bus Operation (RXRATE = LOW, RBCSYNC = HIGH)

When RXRATE is LOW and RBCSYNC is HIGH, the deserializer runs at half-speed (1.06Gb/s or 1.25Gb/s). The RBC0/RBC1 clocks run at 1/10th of the baud rate (106.25MHz or 125MHz). The falling edge of RBC1 and the rising edge of RBC0 are used to clock the data into the attached device.

If ENCDET is HIGH, the RBC clocks will be stretched up to 9 bits in order to align incoming serial data with the parallel bus as indicated by the K28.5 detector. If an incoming data pattern is a correctly aligned K28.5, a data-data-K28.5 RBC realignment will not occur. In Cases A, C, or D, this incoming data pattern will cause realignment.

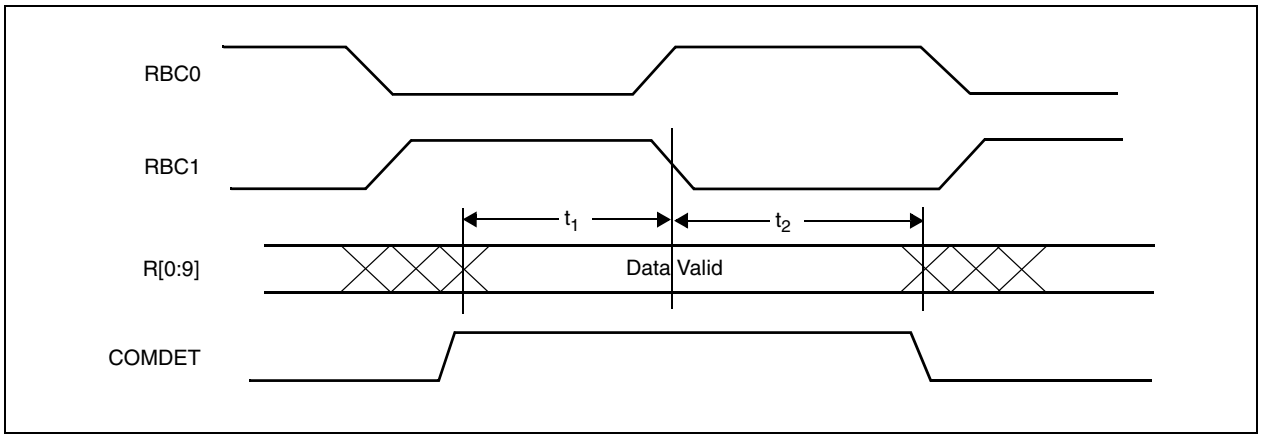


Figure 5. Receive Timing Waveforms (RXRATE = 0, RBCSYNC = 1)

Table 10. Receive AC Characteristics (RXRATE = 0, RBCSYNC = 1)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_1	R[0:9], COMDET valid prior to RBC0 rising edge and RBC1 falling edge	2.0	3.8		ns	1.25Gb/s operation.
		2.0	4.5		ns	1.06Gb/s operation.
t_2	R[0:9], COMDET valid after RBC0 rising edge and RBC1 falling edge	2.0	3.8		ns	1.25Gb/s operation.
		2.0	4.5		ns	1.06Gb/s operation.
R_{LAT}	Latency from Rx to R[0:9]		40bc + 5ns		bc ns	bc = bit clock.

Case C: Receive Bus Operation (RXRATE = HIGH, RBCSYNC = LOW)

When RXRATE is HIGH and RBCSYNC is LOW, the deserializer runs at full speed (2.12Gb/s or 2.5Gb/s). The RBC0/RBC1 clocks run at 1/20th of the baud rate (106.25MHz or 125MHz) and the rising edges of RBC0 and RBC1 are located in the middle of the R[0:9] valid period. This mode is the normal mode for full-speed operation and is compatible with the HSPI interface of Fibre Channel.

If ENCDET is HIGH, the RBC clocks will be stretched up to 19 bits in order to align incoming serial data with the parallel bus as indicated by the K28.5 detector. COMDET will always be centered on the rising edge of RBC1.

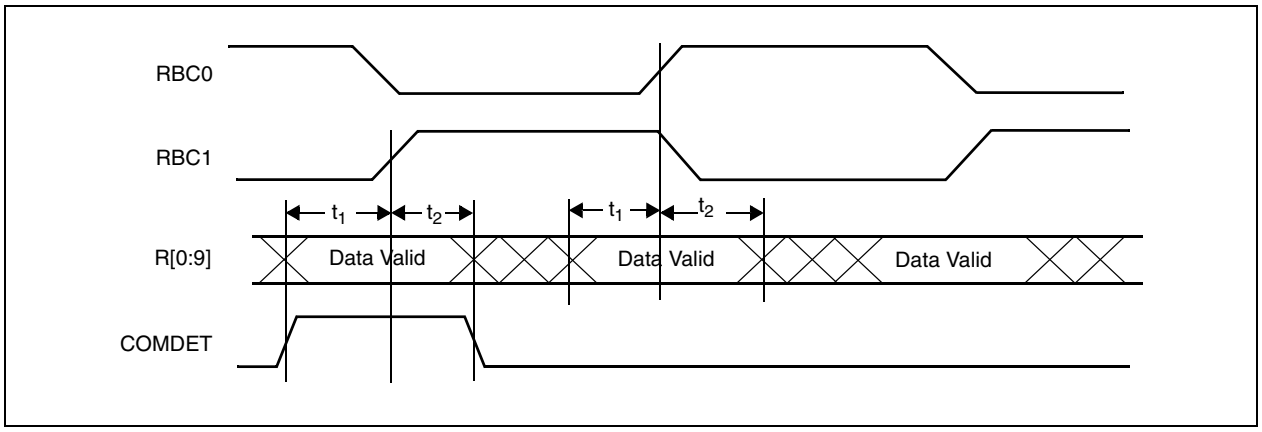


Figure 6. Receive Timing Waveforms (RXRATE = 1, RBCSYNC = 0)

Table 11. Receive AC Characteristics (RXRATE = 1, RBCSYNC = 0)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_1	R[0:9], COMDET valid prior to RBC0/RBC1 rising edge	900	1500		ps	2.5Gb/s operation.
		1500	2200		ps	2.12Gb/s operation.
t_2	R[0:9], COMDET valid after RBC0 or RBC1 rising edge	1100	1700		ps	2.5Gb/s operation.
		1500	2000		ps	2.12Gb/s operation.
R_{LAT}	Latency from Rx to R[0:9]		40bc + 5ns		bc ns	bc = bit clock.

Case D: Receive Bus Operation (RXRATE = HIGH, RBCSYNC = HIGH)

When RXRATE is HIGH and RBCSYNC is HIGH, the deserializer runs at full-speed (2.12Gb/s or 2.5Gb/s). The RBC0/RBC1 clocks run at 1/20th of the baud rate (106.25MHz or 125MHz) and the edges of RBC1 are aligned to the edge of the R[0:9] valid period. This makes the receiver of the VSC7145 function similarly to the Protocol Controller attached to the transmitter bus with ASIC-Friendly timing.

If ENCDET is HIGH, the RBC clocks will be stretched up to 19 bits in order to align incoming serial data with the parallel bus as indicated by the K28.5 detector. COMDET will always be output after the rising edge of RBC1.

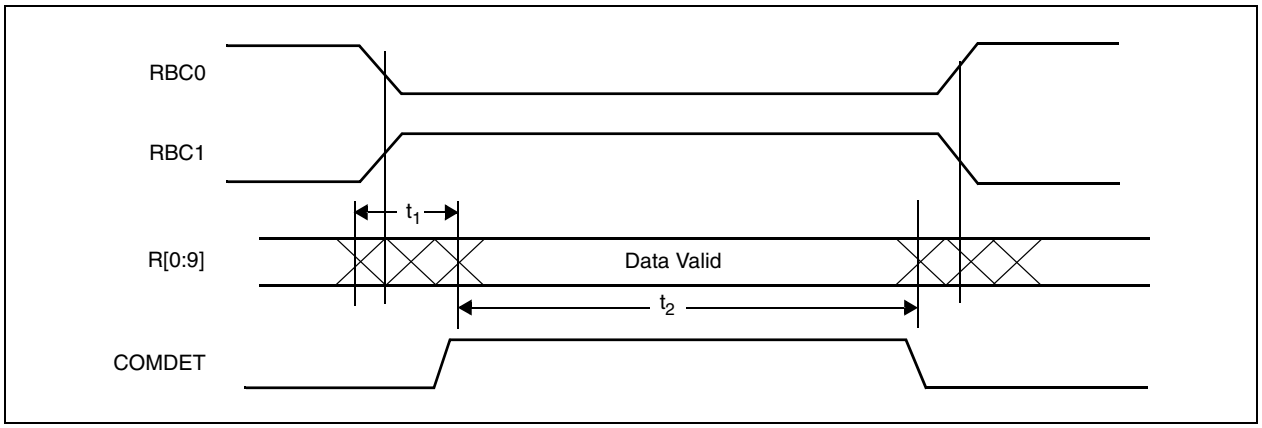


Figure 7. Receive Timing Waveforms (RXRATE = 1, RBCSYNC = 1)

Table 12. Receive AC Characteristics (RXRATE = 1, RBCSYNC = 1)

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_1	R[0:9], COMDET and RBC1 clock transition		0.35	1.2	ns	2.5Gb/s operation.
			0.35	1.4	ns	2.12Gb/s operation.
t_2	R[0:9], COMDET and RBC1 valid time	2.7	3.6		ns	2.5Gb/s operation.
		3.2	4.3		ns	2.12Gb/s operation.
R_{LAT}	Latency from Rx to R[0:9]		40bc + 5ns		bc ns	bc = bit clock.

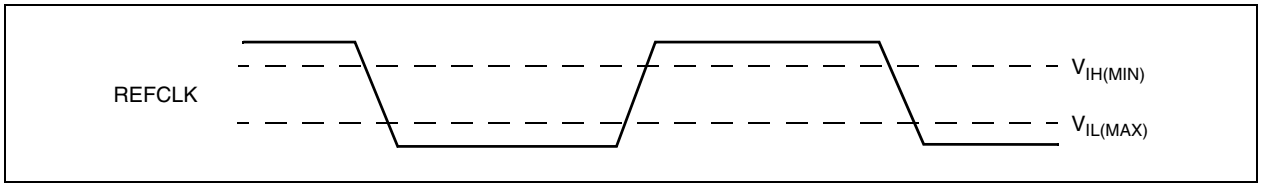


Figure 8. REFCLK Timing Waveforms

Table 13. Reference Clock Requirements

Symbol	Parameter	Min	Typ	Max	Units	Condition
FR	Frequency range	105		126	MHz	REFRATE = LOW.
		52.5		63	MHz	REFRATE = HIGH.
FO	Frequency offset	–200		+200	ppm	Maximum frequency offset between transmit and receive reference clocks on one link.
DC	REFCLK duty cycle	35		65	%	
t_{RCR}, t_{RCF}	REFCLK rise and fall tIme			1.5	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.

Table 14. Receive AC Characteristics (regardless of RXRATE)

Symbol	Parameter	Min	Typ	Max	Units	Condition
F	Frequency offset	–200		+200	ppm	
UI_R	Eye opening at SI±	0.25			UI	
	CRU lock time		300		Data Transistion	Per section 5.3 of FC-PH revision 4.3

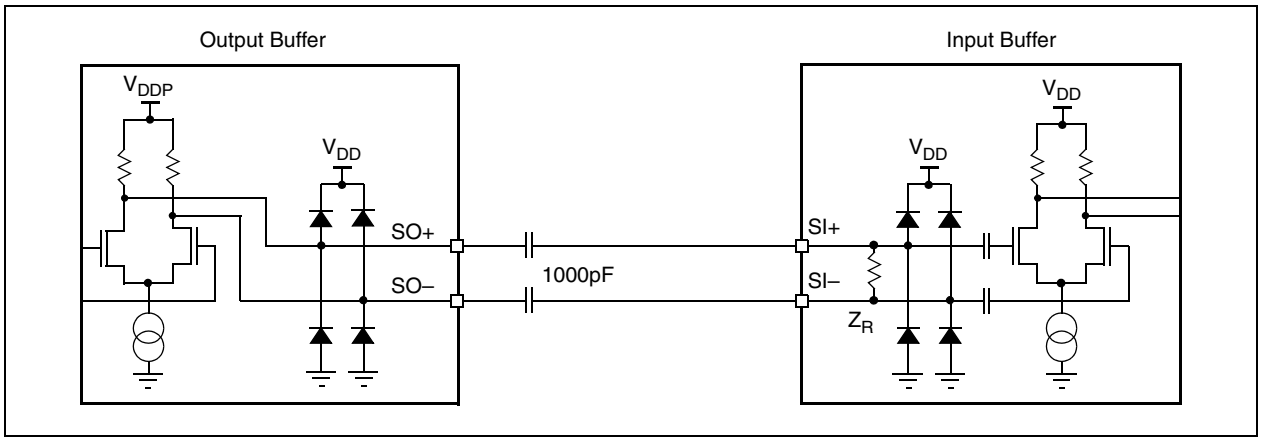


Figure 9. High-Speed Serial Link

SPECIFICATIONS

DC Characteristics

Over Recommended Operating Conditions.

Table 15. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Condition
SSTL_2 and SSTL_3 Inputs/Outputs						
VREFT	Voltage reference input **SSTL_2 (VSC7145-30, VSC7145-34)** **SSTL_3 (VSC7145-31)**	 1.15 1.30	 1.25 1.50	 1.35 1.70	 V V	
V_{IH}	Input HIGH voltage	VREFT+0.35		V_{DDD}+0.30	V	
V_{IL}	Input LOW voltage	–0.30		VREFT–0.35	V	
I_{IH}	Input HIGH current			250	µA	V_{IN} = 2.4V.
I_{IL}	Input LOW current			–150	µA	V_{IN} = 0.5V.
VREFR	Voltage reference output **SSTL_2 (VSC7145-30, VSC7145-34)** **SSTL_3 (VSC7145-31)**	 1.15 1.30	 1.25 1.50	 1.35 1.70	 V V	
V_{OH}	Output HIGH voltage **SSTL_2 (VSC7145-30, VSC7145-34)** **SSTL_3 (VSC7145-31)**	 VREFR+0.45 VREFR+0.45		 V_{DDQ}–0.5 V_{DDQ}	 V V	50Ω transmission line. Unterminated load.
V_{OL}	Output LOW voltage	0		VREFR–0.45	V	50Ω transmission line. Unterminated load.
Miscellaneous						
V_{DD}	Supply voltage (all supplies)	3.14	3.3	3.47	V	3.3V ±5%.
P_D	Power dissipation **VSC7145-30, VSC7145-34** **VSC7145-31**		 1.1 0.9	 1.5 1.1	 W W	 Outputs open. Outputs open.
I_{DD}	Supply current (all supplies) **VSC7145-30, VSC7145-34** **VSC7145-31**		 333 270	 440 330	 mA mA	 Outputs open. Outputs open.
I_{DDA}	Supply current on V_{DDA}			60	mA	

AC Characteristics

Over Recommended Operating Conditions.

Table 16. AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Condition
ΔV_{OUT50}	SO output differential peak-to-peak voltage swing[1] (**VSC7145-30, VSC7145-31)**	800		2000	mVp-p	(SO+) – (SO–). Pre-emphasis off.
ΔV_{OUT50}	SO output differential peak-to-peak voltage swing[1] (**VSC7145-34)**	1000		1600	mVp-p	(SO+) – (SO–). Pre-emphasis off.
ΔV_{IN}	SI input differential peak-to-peak input sensitivity[1]	175		2000	mVp-p	(SI+) – (SI–). Internally AC-coupled.[2]
Z_{IN}	SI input differential input impedance	95	100	105	Ω	100Ω ±5%.

1. *Refer to Application Note, AN-37 for differential measurement techniques.*
2. *If there is no external AC-coupling capacitor for the PELL input, V_{IH} cannot be higher than the power supply of the VSC7145.*

Table 17. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Power supply voltage	+3.135	+3.3	+3.465	V
T	Operating temperature range[1]	0		+110	°C

1. *Lower limit of specification is ambient temperature, and upper limit is case temperature.*

Table 18. Absolute Maximum Ratings

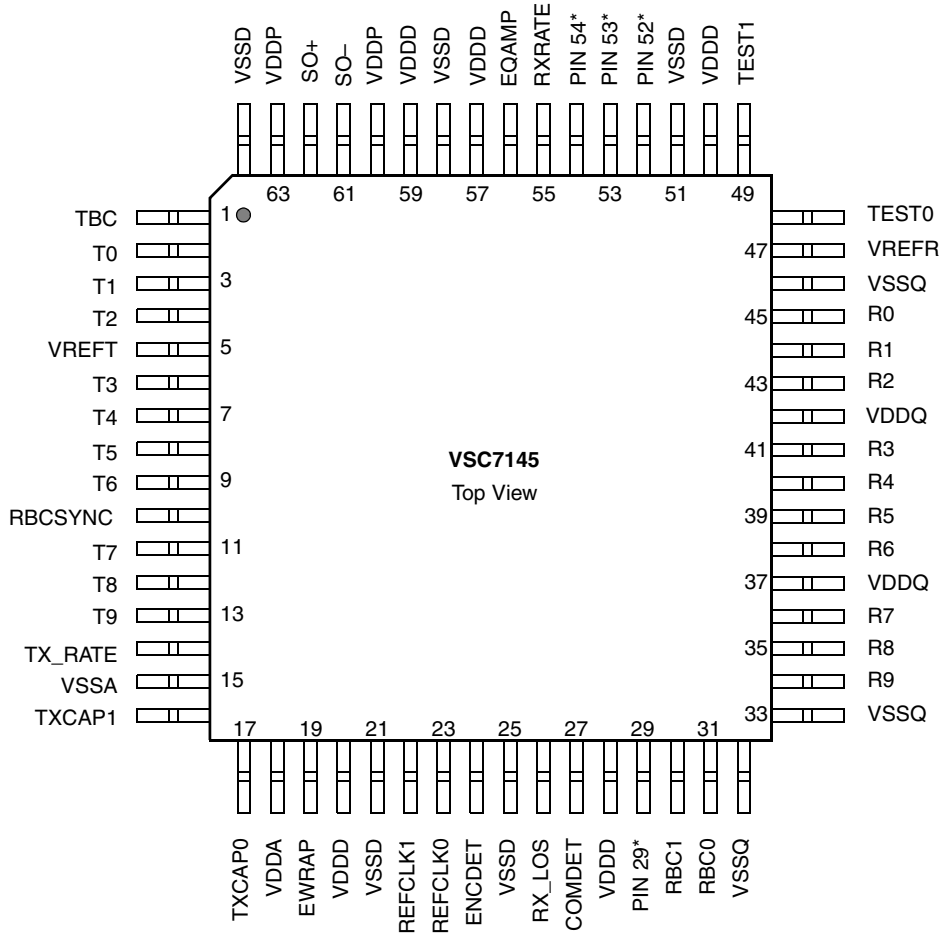
Symbol	Parameter	Min	Max	Units
V_{DD}	Power supply voltage	–0.5	+4.0	V
	DC input voltage (PECL, TTL, SSTL)	–0.5	V_{DD} + 1.0	V
	DC output voltage (PECL, TTL, SSTL)	–0.5	V_{DD} + 0.5	V
I_{OUT}	Output currents (PECL, TTL, SSTL)	–50	+50	mA
T_C	Case temperature under bias	–55	+125	°C
T_S	Storage temperature	–65	+150	°C
V_{ESD}	ESD (Human Body Model)		1600	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PACKAGE INFORMATION



* See Table 19 on page 17 for pin differences between device variants.

Figure 10. Pin Diagram

Table 19. Pin Assignment Differences for VSC7145-30, VSC7145-31, and VSC7145-34

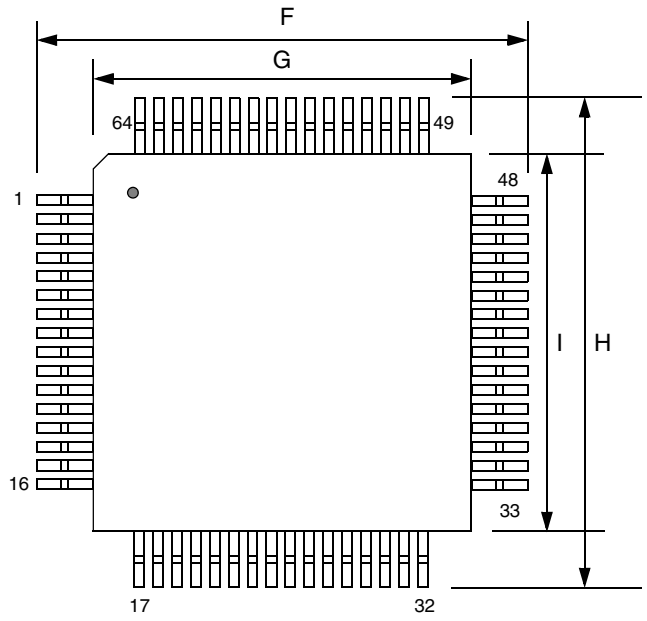
Part Number	Pin 29	Pin 52	Pin 53	Pin 54	
VSC7145-30	REFRATE	SI–	N/C	SI+	Compatible with HDMP-2630
VSC7145-31	REFRATE	SI–	N/C	SI+	Compatible with HDMP-2631
VSC7145-34	N/C	SI+	SI–	N/C	Compatible with HDMP-2634

Table 20. Pin Identification

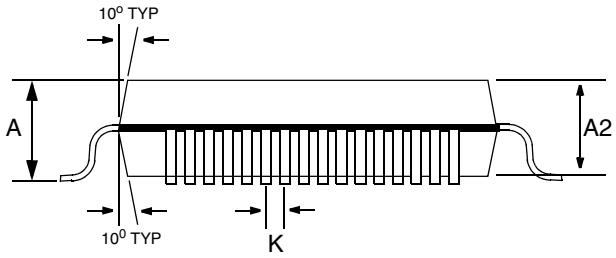
Pin	Signal Name	I/O	Type	Description
2, 3 4, 6 7, 8 9, 11 12, 13	T0, T1 T2, T3 T4, T5 T6, T7 T8, T9	I	SSTL	10-Bit Transmit Character. Parallel data on this bus is clocked into the input register synchronously to TBC. T0 is transmitted first. Referenced to VREFT.
1	TBC	I	SSTL	Transmit Byte Clock. Derived from the same source as REFCLK. TBC is synchronous to T[0:9].
5	VREFT	I	Reference	Voltage Reference for SSTL Inputs. Internally biased to 1.25V (VSC7145-30 and VSC7145-34) or 1.50V (VSC7145-31) but may be driven by an external voltage reference.
22 23	REFCLK1 REFCLK0	I	PECL, SSTL, TTL	Reference Clock for the CMU. Complementary. If SSTL, connect REFCLK1 to the clock and REFCLK0 to VREFT. If LVTTL, connect to REFCLK1 and leave REFCLK0 open. If LVPECL, connect to both REFCLK1 and REFCLK0.
14	TX_RATE	I	SSTL	When HIGH, selects full-speed mode. When LOW, selects half-speed mode. Referenced to VREFT.
62 61	SO+ SO–	O		These pins output the serialized transmit data when EWRAP is LOW. When EWRAP is HIGH, SO+ is HIGH and SO– is LOW. Differential (AC-coupling recommended).
45, 44 43, 41 40, 39 38, 36 35, 34	R0, R1 R2, R3 R4, R5 R6, R7 R8, R9	O	SSTL	10-Bit Received Character. Parallel data on this bus is synchronous to RBC0 and RBC1. R0 is the first bit received. Referenced to VREFR.
See Table 19	SI+ SI–	I		These are the serial receive data inputs when EWRAP is LOW. Differential (AC-coupled internally).
31 30	RBC0 RBC1	O	SSTL	Recovered clock derived from the receive data baud rate. Complementary. Referenced to VREFR. Locks to the REFCLK if there is no high speed data at input SI+/–.
10	RBCSYNC	I	SSTL	Controls RBC to R[0:9] output timing. Referenced to VREFT.
See Table 19	REFRATE	I	STL	Controls whether REFCLK1/REFCLK0 are 1/10th, 1/20th, or 1/40th the transmit bit rate. Pin 29 is a no-connect and disabled in VSC7145-34 version. Referenced to VREFT.
47	VREFR	O	Reference	Voltage Reference Output for SSTL. Nominally biased to 1.25V (VSC7145-30 and VSC7145-34) or 1.50V (VSC7145-31).
55	RXRATE	I	SSTL	Determines the receiver data rate. HIGH for full speed, LOW for half speed. Referenced to VREFT.
24	ENCDET	I	SSTL	Enables COMDET and word re-synchronization when HIGH. When LOW, keeps current word alignment and disables COMDET. Referenced to VREFT.
27	COMDET	O	SSTL	This output goes HIGH to indicate that R[0:9] contains a K28.5 character (0011111010 or 1100000101). COMDET will go HIGH only during a cycle when RBC1 is rising. COMDET is enabled by ENCDET being HIGH. Referenced to VREFT.
26	RX_LOS	O	SSTL	Receiver Loss of Signal. This output goes LOW when the SI input is valid as determined by transition detection, RLL checking and K28.5 checking. This output goes HIGH when the SI input does not meet these criteria. Referenced to VREFT.

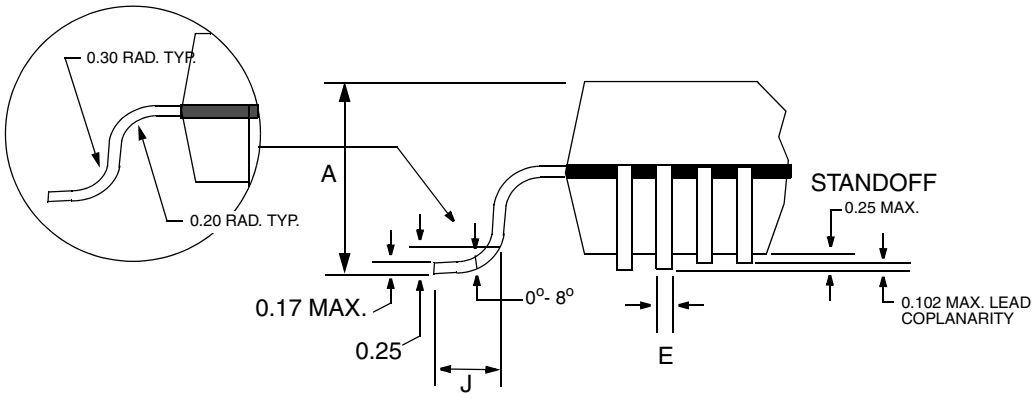
Table 20. Pin Identification (continued)

Pin	Signal Name	I/O	Type	Description
19	EWRAP	I	SSTL	LOW for Normal Operation. When HIGH, an internal loopback path from the transmitter to the receiver is enabled and the SO outputs are held HIGH. Referenced to VREFT.
56	EQAMP	I	TTL	When LOW, pre-emphasis on SO is enabled. When HIGH, pre-emphasis is disabled.
48 49	TEST0 TEST1	I	TTL	These signals are used for factory test. For normal operation, leave unconnected.
17 16	TXCAP0 TXCAP1		Analog	An external 0.1µF (nominal) capacitor is connected between these pins to determine the Clock Multiplier PLL loop filter response.
18	VDDA		Pwr	Analog Power Supply. Separate filtering is recommended.
15	VSSA		Pwr	Analog Ground.
20, 28, 50, 57, 59	VDDD		Pwr	Digital Logic Power Supply.
21, 25, 51, 58, 64	VSSD		Pwr	Digital Logic Ground.
37, 42	VDDQ		Pwr	Power Supply for SSTL.
32, 33, 46	VSSQ		Pwr	Ground for SSTL.
60, 63	VDDP		Pwr	Power Supply for PECL.
See Table 19	N/C			Not Internally Connected. May be connected to V_{DD} externally for compatibility with HDMP-263x.



Item	mm	Tolerance
A	2.35	MAX
A2	2.00	+0.10/–0.05
E	0.35	±0.05
F	17.20	±0.25
G	14.00	±0.10
H	17.20	±0.25
I	14.00	±0.10
J	0.88	+0.15/–0.10
K	0.80	BASIC





NOTES:
Drawing not to scale.

All units in mm unless otherwise noted.

Figure 11. Package Drawing

Package Construction

The VSC7145 is packaged in a 14mm x 14mm, 64-pin PQFP with an industry-standard EIAJ footprint. The construction of the packages is shown in Figure 12.

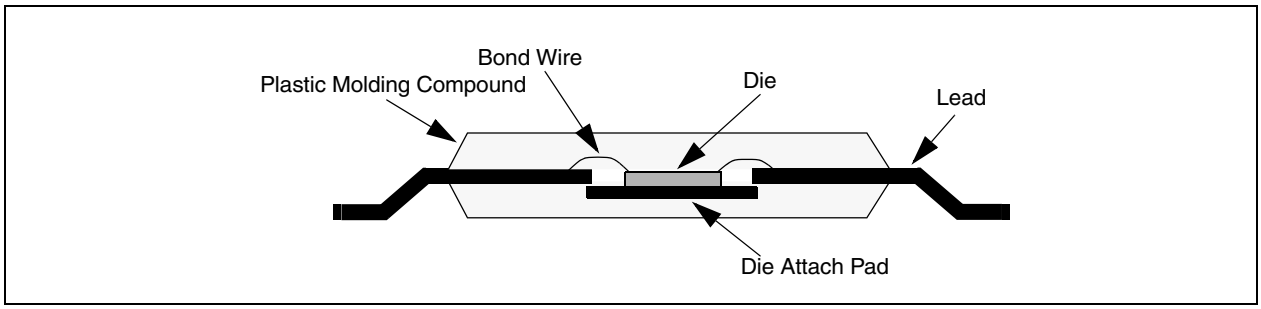


Figure 12. Package Cross Section

Moisture Sensitivity Level

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

ORDERING INFORMATION

Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

VSC7145 Dual Speed 10-Bit Serializer/Deserializer

Part Number	Description
VSC7145RU-30	64-pin PQFP, 14mm x 14mm body, SSTL_2 version
VSC7145XRU-30	Lead-free, 64-pin PQFP, 14mm x 14mm body, SSTL_2 version
VSC7145RU-31	64-pin PQFP, 14mm x 14mm body, SSTL_3 version
VSC7145XRU-31	Lead-free, 64-pin PQFP, 14mm x 14mm body, SSTL_3 version
VSC7145RU-34	64-pin PQFP, 14mm x 14mm body, SSTL_2 version with alternate pinout
VSC7145XRU-34	Lead-free, 64-pin PQFP, 14mm x 14mm body, SSTL_2 version with alternate pinout

NOTE: *Refer to "Product Options" on page 2 for additional information.*

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