

# 2N7002L

## Small Signal MOSFET

60 V, 115 mA, N-Channel SOT-23

### Features

- AEC Qualified
- PPAP Capable
- Pb-Free Packages are Available

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	60	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Drain Current - Continuous $T_C = 25^\circ\text{C}$ (Note 1) - Pulsed (Note 2) $T_C = 100^\circ\text{C}$ (Note 1)	$I_D$ $I_{D(on)}$ $I_{DM}$	$\pm 115$ $\pm 75$ $\pm 800$	mAdc
Gate-Source Voltage - Continuous - Non-repetitive ( $t_p \leq 50 \mu\text{s}$ )	$V_{GS}$ $V_{GSM}$	$\pm 20$ $\pm 40$	Vdc Vpk

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 3) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 4) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .
3. FR-5 =  $1.0 \times 0.75 \times 0.062$  in.
4. Alumina =  $0.4 \times 0.3 \times 0.025$  in 99.5% alumina.

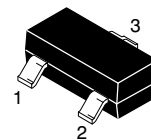
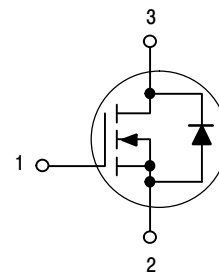


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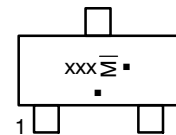
$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	$7.5 \Omega @ 10 \text{ V}, 500 \text{ mA}$	115 mA

### N-Channel



SOT-23  
CASE 318  
STYLE 21

### MARKING DIAGRAM



702 = Device Code  
M = Date Code\*  
■ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
2N7002LT1	SOT-23	3000 Tape & Reel
2N7002LT3		10,000 Tape & Reel
2N7002LT1G	SOT-23 (Pb-free)	3000 Tape & Reel
2N7002LT3G		10,000 Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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### ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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#### OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V <sub>GS</sub> = 0, I <sub>D</sub> = 10 μAdc)	V <sub>(BR)DSS</sub>	60	-	-	Vdc
Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0, V <sub>DS</sub> = 60 Vdc)	I <sub>DSS</sub>	T <sub>J</sub> = 25°C	-	-	1.0
		T <sub>J</sub> = 125°C	-	-	500
Gate-Body Leakage Current, Forward (V <sub>GS</sub> = 20 Vdc)	I <sub>GSSF</sub>	-	-	100	nAdc
Gate-Body Leakage Current, Reverse (V <sub>GS</sub> = -20 Vdc)	I <sub>GSSR</sub>	-	-	-100	nAdc

#### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc)	V <sub>GS(th)</sub>	1.0	-	2.5	Vdc
On-State Drain Current (V <sub>DS</sub> ≥ 2.0 V <sub>DS(on)</sub> , V <sub>GS</sub> = 10 Vdc)	I <sub>D(on)</sub>	500	-	-	mA
Static Drain-Source On-State Voltage (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 500 mAdc) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 50 mAdc)	V <sub>DS(on)</sub>	-	-	3.75	Vdc
		-	-	0.375	
Static Drain-Source On-State Resistance (V <sub>GS</sub> = 10 V, I <sub>D</sub> = 500 mAdc)  (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 50 mAdc)	r <sub>DS(on)</sub>	T <sub>C</sub> = 25°C	-	-	7.5
		T <sub>C</sub> = 125°C	-	-	13.5
		T <sub>C</sub> = 25°C	-	-	7.5
		T <sub>C</sub> = 125°C	-	-	13.5
Forward Transconductance (V <sub>DS</sub> ≥ 2.0 V <sub>DS(on)</sub> , I <sub>D</sub> = 200 mAdc)	g <sub>FS</sub>	80	-	-	mmhos

#### DYNAMIC CHARACTERISTICS

Input Capacitance (V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>iss</sub>	-	-	50	pF
Output Capacitance (V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>oss</sub>	-	-	25	pF
Reverse Transfer Capacitance (V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>rss</sub>	-	-	5.0	pF

#### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	(V <sub>DD</sub> = 25 Vdc, I <sub>D</sub> ≅ 500 mAdc, R <sub>G</sub> = 25 Ω, R <sub>L</sub> = 50 Ω, V <sub>gen</sub> = 10 V)	t <sub>d(on)</sub>	-	-	20	ns
Turn-Off Delay Time		t <sub>d(off)</sub>	-	-	40	ns

#### BODY-DRAIN DIODE RATINGS

Diode Forward On-Voltage (I <sub>S</sub> = 11.5 mAdc, V <sub>GS</sub> = 0 V)	V <sub>SD</sub>	-	-	-1.5	Vdc
Source Current Continuous (Body Diode)	I <sub>S</sub>	-	-	-115	mAdc
Source Current Pulsed	I <sub>SM</sub>	-	-	-800	mAdc

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

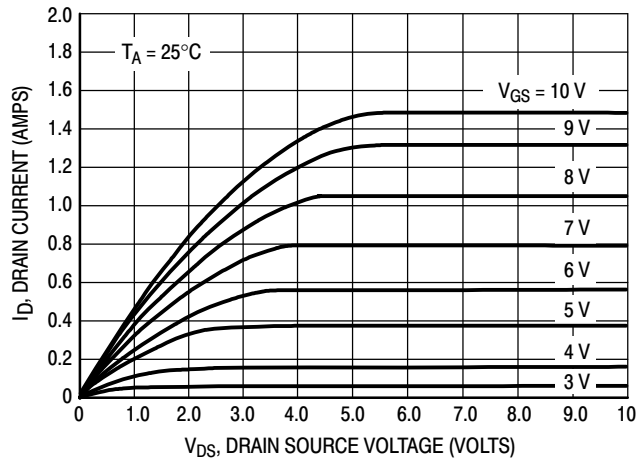


Figure 1. Ohmic Region

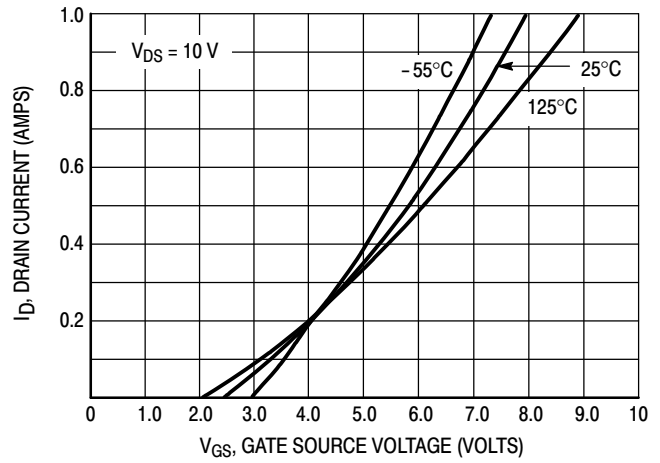


Figure 2. Transfer Characteristics

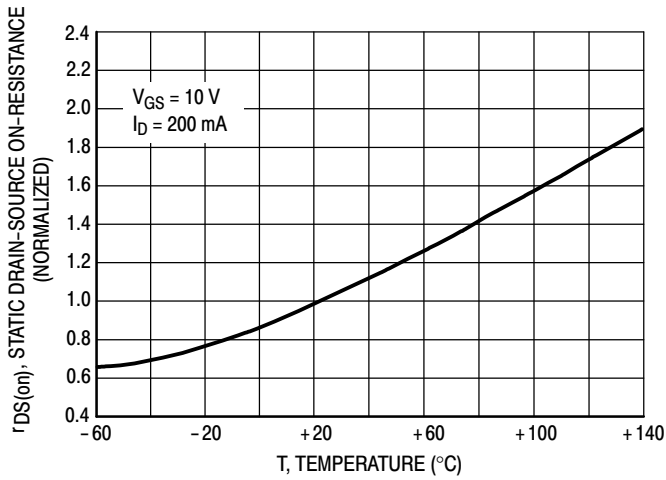


Figure 3. Temperature versus Static Drain-Source On-Resistance

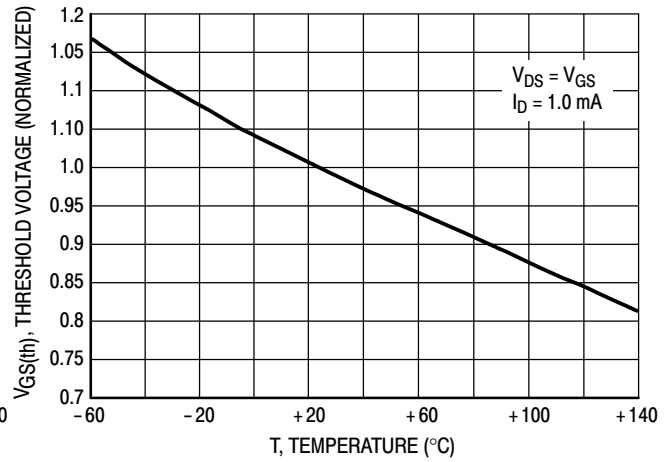
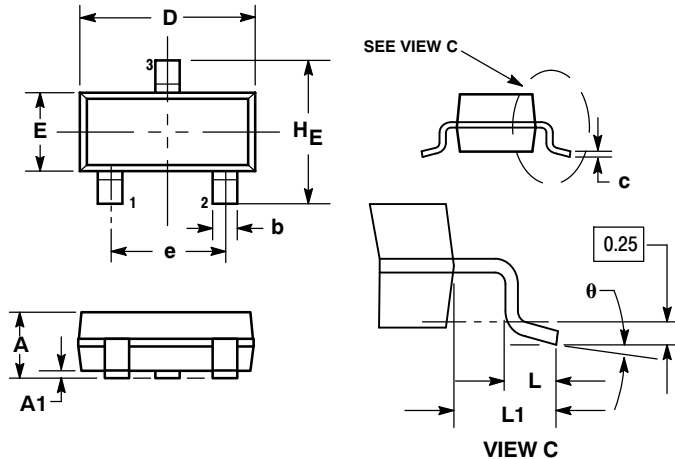


Figure 4. Temperature versus Gate Threshold Voltage

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## PACKAGE DIMENSIONS

### SOT-23 (TO-236) CASE 318-08 ISSUE AN



#### NOTES:

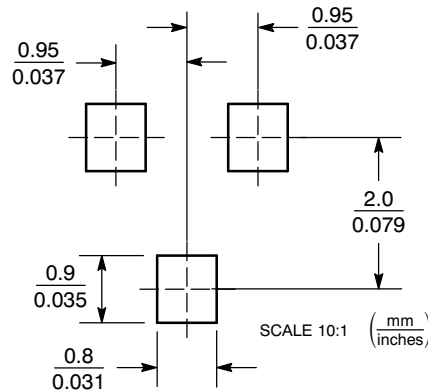
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104


#### STYLE 21:

1. GATE
2. SOURCE
3. DRAIN

## SOLDERING FOOTPRINT



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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