Key Features

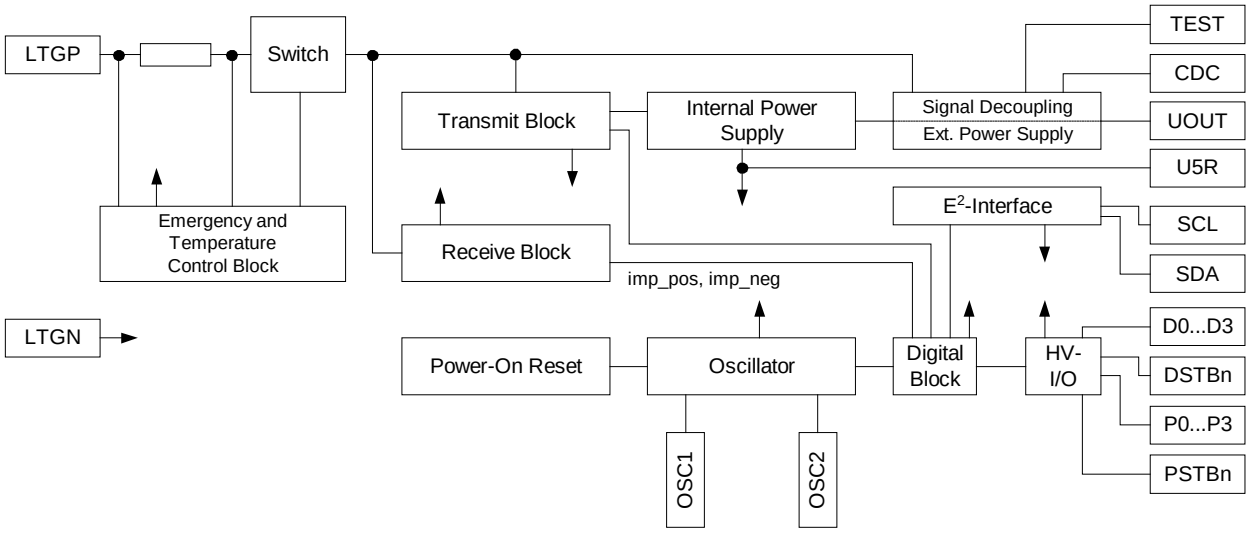
- Simple two-wire bus (ASI line)
- Transmission of both power and signal on the ASI line
- Decoupling of power and signal by the IC without additional external devices
- Transmitting protocol for using the IC and the ASI master in the transmit/receive modes
- Switching of max. 31 ASI slave ICs on one bus possible
- Power supply of peripheral devices from the ASI slave IC of up to 35 mA @ 24V
- Only few external devices necessary for operation (quartz, 4 capacitors, E^2PROM)
- Storing of the configuration data and the slave address in one E^2PROM
- Quartz oscillator for 5.333 MHz without external capacitances
- Standards: AS-Interface–Spec V2.0 and EN 50295

General Description

The signal transmission between the master and the slaves in the ASI system is performed by a parallel two-line wire (ASI-line) to which the IC is connected only via a polarity protection diode and a suppressor diode. The line is powered by a direct dc voltage of up to 33.1 V, on which data pulses with signal amplitudes of (3...8) Vpp are superimposed. The IC extracts its own power and the power for peripherals from the line and detects the bus signals.
The ASI slave IC consists of the following blocks:

- Receive Block
- Transmit Block
- Digital Logic Block
- Emergency Control Block
- Internal and External Power Supply with Signal decoupling
- Oscillator
- Power on Reset
- High Voltage I/O

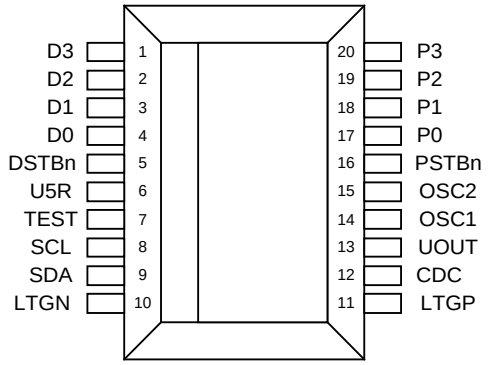
Block Diagram



Package

SOIC 20

Pin Description



Pin	Name	Type	Description
1	D3	I/O	Data input/output 3, configurable
2	D2	I/O	Data input/output 2, configurable
3	D1	I/O	Data input/output 1, configurable
4	D0	I/O	Data input/output 0, configurable
5	DSTBn	I/O	Strobe output for the data port, input for a reset signal (active low)
6	U5R	Voltage OUT	Supply voltage of the E^2PROM, Blocking capacitor CU5R
7	TEST	IN	Connection to the capacitor CTEST
8	SCL	OUT	Serial two-wire bus, puls wire
9	SDA	I/O	Serial two-wire bus, address and data wire
10	LTGN	SUPPLY	ASI wire, negative supply
11	LTGP	SUPPLY	ASI wire, positive supply
12	CDC	Voltage OUT	Blocking capacitor CCDC
13	UOUT	Voltage OUT	Peripherals
14	OSC1	IN	Quartz connection
15	OSC2	OUT	Quartz connection
16	PSTBn	OUT	Strobe output for the parameter port, test mode (without importance for users)
17	P0	OUT	Parameter output 0
18	P1	OUT	Parameter output 1
19	P2	OUT	Parameter output 2
20	P3	OUT	Parameter output 3

Functional Description

The IC identifies and decodes the supply voltage overlapping signals of the master telegram. If the slave address contained within the master telegram coincides with the stored information in the E²PROM of the slave address, the corresponding master command of the addressed ASI slave IC is executed.

After decoding of the master telegram the addressed ASI slave IC responds with a corresponding slave answer on the ASI line.

The ASI slave IC extracts its own supply voltage and the supply voltage for the E²PROM from the ASI line. At the same time, the IC provides a direct voltage for the peripheral UOUT which results from U_{LTGP}-U_{DROP} for a maximum current of 35 mA.

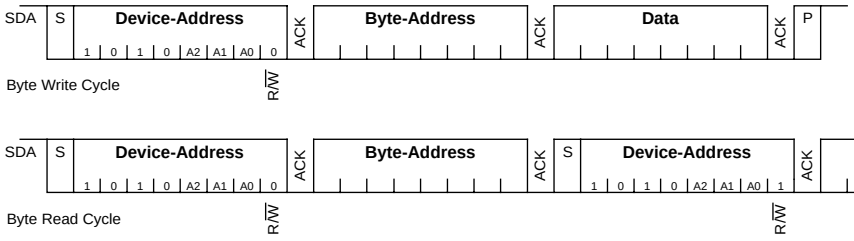
The receive block detects the signal on the ASI wire LTGP. The reference voltages of the signal comparators are (52.5 ± 5) % of the maximum signal value and are controlled by a peak value detector in the following mode: The comparator level is set to its default value by Reset or if a non-correct signal is received.

If a line pause is detected, the level reset is released and the ASIC is able to adapt itself to different signal levels. If the IC is not synchronized yet, the level adaption is faster (smaller attack and decay time constants) as in the synchronous case.

The output information of the receive blocks are the signals: "imp_pos" and "imp_neg".

The transmit block drives the output level for the modulated transmit signal edges. The transmit block consists of the NMOS transistor (transmit transistor), DAC for transmit signal formation and a Jabber-Inhibit Circuitry. The DAC is addressed by the digital block. If the transmitter is active more than typ. 300µs the Jabber-Inhibit circuit separates the IC from the ASI line. This condition can only be left by a Power-On-Reset.

In the digital block the received signal is analyzed, the transmit signal is generated and the data and parameter ports as well as the E²PROM interface are driven. The E²PROM interface acts as a serial two-wire interface with the following transmission strams:



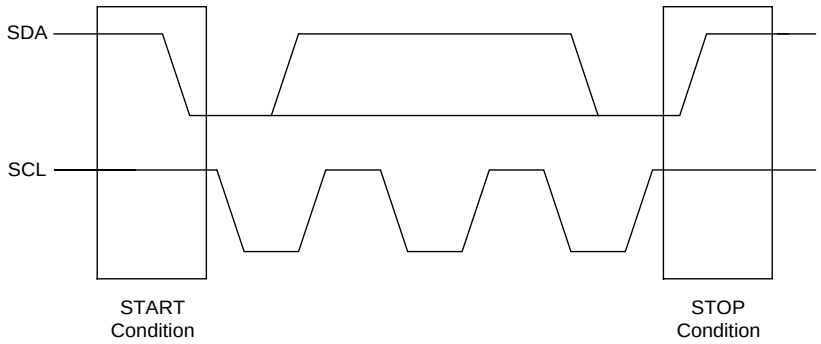
After the ASI slave IC has sent the START condition, the device address is transmitted. This address serves for the selection of a maximum of 8 possible E²PROM ICs on this bus. This device address is defined as 000 within the ASI slave IC interface. Therefore in the application the PINS AO...A2 of the E²PROM are always set at Uss of the E²PROM.

Write Cycle

After the device address, the write cycle R/W-Bit=0, necessary for the identification of the write cycle, is sent. The E²PROM acknowledges the correct receipt with the acknowledge bit ACK. Then the data byte which should be written into the E²PROM reacknowledges with an ACK signal of the E²PROM. The STOP condition ends the cycle.

Read Cycle

The read cycle is similar to the herein described write cycle. In this case the R/W-Bit = 1 which causes the E²PROM to place read data for the received Byte address on the bus after the acknowledge.



The **START condition** is recognized by the E²PROM when a H/L edge arises on the dataline SDA during the high phase of the clock.

The **STOP condition** is present when a L/H edge arises on the dataline SDA during the high phase of the clock SCL. The timing of the E²PROM interface is derived from the ASI quartz frequency of 5.333 MHz.

Functional, electrical and timing characteristics

All voltages are referenced to LTGN = 0V, timing is valid for a clock frequency of 5.333 MHz.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
VLTGP	Positive Voltage	- 0.3	40	V	1
VLTGPOV	Positive Impulse Voltage		50	V	2
Vin1	Voltage at D0...D3, P0...P3, DSTBn, PSTBn, CDC, UOUT, TEST	VLTGN - 0.3	VLTGP + 0.3	V	Vin ≤ 40V
Vin2	Voltage at OSC1, OSC2, SDA, SCL, U5R	VLTGN - 0.3	7	V	
Iin	Input Current on every Pin	-25	25	mA	
H	Non-Condensated Humidity				3
ESD	Electrostatic Discharge		1000	V	4
θSTG	Storing Temperature	-55	125	°C	
θlead	Soldering Temperature		260	°C	5
Ptot	Power Dissipation		1	W	6

Notes:

1 A polarity protection diode is to be used externally

2 Impulse width: ≤ 50 µs; repetition rate: ≤ 0.5 Hz

3 Defined in DIN 40040 cond. F

4 HBM; R = 1.5 kΩ; C = 100pF

5 260 °C for 10 s (reflow and wave soldering), 360 °C for 3 s (manual soldering)

6 SOIC 20: Rthja = 64.5 °K/W typ.

Recommended Operating Conditions

Symbol	Parameter	Min	max	Unit	Note
VLTGP1	Positive Voltage	26.9	33.1	V	1
VLTGP2	Positive Voltage for Sensor Applications	17.5	33.1	V	2
ILTG	Operating Current @ VLTG = 30 V		6	mA	3
IOL	Max. Operating Current @ D0...D3, DSTBn		10	mA	
IOL	Max. Output Current @ P0...P3, PSTBn		6	mA	
fC	Quartz Frequency	5.333		MHz	4
θamb	Operating Temperature	-25	85	°C	

Notes:

1 DC Parameter; VLTGP1min = VUOUTmin + VDROPmax;
VLTGPmax = VUOUTmax + VDROPmin

2 DC Parameter; VLTGP2min = VCOMOFFmax + VDROPmax

3 fC = 5.333 MHz, no load on UOUT and U5R, IC in idle mode

4 “ASI-Quartz”

Power Supply Pins LTGP and LTGN (LTGN = 0 V-reference

The ASI Slave IC's input at LTGP behaves as if a resistor RP and a (non-linear) parallel capacitor CP connect LTGP to LTGN.

LTGP input impedance over frequency is as follows:

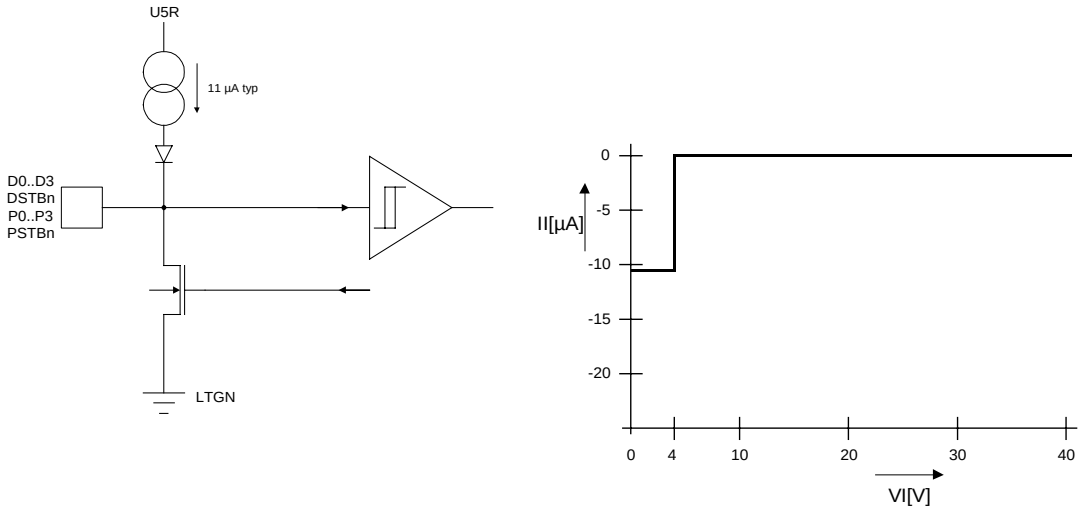
RP	CP	F
≥ 10 kOhm	≤ 35 pF	50 kHz
≥ 10 kOhm	≤ 45 pF	100 kHz
≥ 10 kOhm	≤ 48 pF	125 kHz
≥ 10 kOhm	≤ 51 pF	160 kHz
≥ 10 kOhm	≤ 54 pF	200 kHz
≥ 10 kOhm	≤ 60 pF	300 kHz

Data and Parameter Ports (D0...D3, DSTBn; P0...P3, PSTBn)

These pins are equipped with both an input and output channel as well as a current source based pull-up structure; the I/O-circuit at these pins and their DC-characteristics @ output channel 'Off' are described below.

The ASI slave system concept requires D0...D3 and DSTBn to be bidirectional pins and P0...P3 and PSTBn to be outputs.

The input channel on pins P0...P3 and PSTBn is only implemented to simplify the ASI Slave IC's device test, and is not intended to be used in ASI Slave system applications.



Symbol	Parameter	min	max	Unit	Note
VIL	Input Voltage “Low”	0	1.5	V	
VIH	Input Voltage “High”	3.5	VUOUT	V	
VHYST	Input Hysteresis	0.25	0.5	V	1
VOL11	Output Voltage	0	1	V	IOL11 = 10mA D0...D3, DSTBn
VOL12	Output Voltage	0	1	V	IOL12 = 6mA P0...P3, PSTBn
VOL2	Output Voltage	0	0.4		IOL2 = 2mA
IIL	Input Current	-20	-5	µA	VIL = 1V, Output “off”
IIH	Input Current	-10	10	µA	VU5R ≤ VIH ≤ 40V Output “off”
CDL	Loading Capacitance on DSTBn		10	pF	2

Notes:

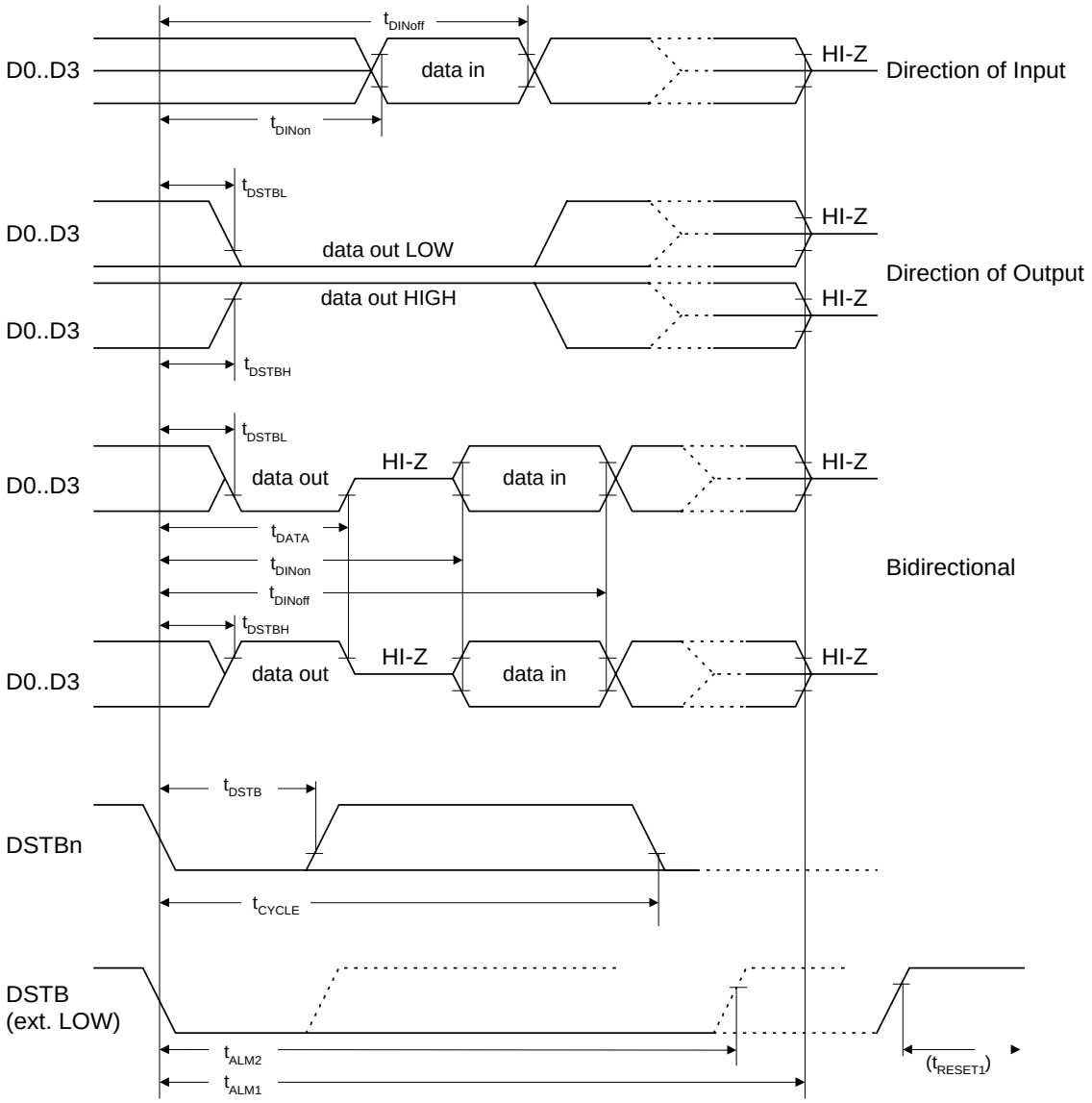
1 Switching points approx. 2.5 V, i.e. 2.5 V ± VHYST

2 For larger capacitive loads an external Pull-Up-Resistor to UOUT must be used, so that the beginning of the DSTB = LOW impulse of VIH ≤ 3.5 V to DSTBn is reached in less than 35 µs, otherwise a reset is the result.

Timing characteristics

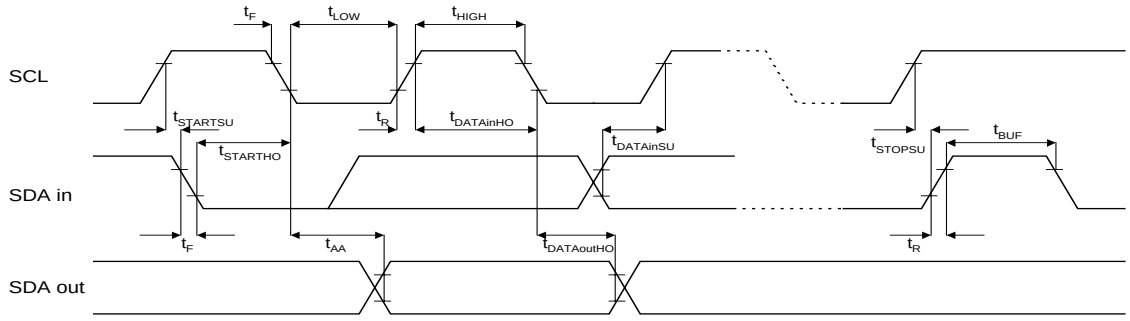
Symbol	Parameter	min	max	Unit	Note
t_{DSTBL}	DSTBn to D0...D3, Direction OUT, Output Data LOW		1	µs	
t_{DSTBH}	DSTBn to D0...D3, Direction OUT, Output Data HIGH		1.5	µs	
t_{DATA}	DSTBn to D0...D3, High Resistive	6.2	7	µs	1
t_{DSTB}	DSTBn Pulse Width	6	6.8	µs	
t_{DINon}	DSTBn to D0...D3, Direction IN, Valid Input Data	6.5	7.7	µs	
t_{DINoff}	DSTBn to D0...D3, End of Direction IN	12.5	t CYCLE	µs	
t_{CYCLE}	Next Cycle	150		µs	
t_{ALM1}	Extension DSTBn to D0...D3, High Resistive		44	µs	
t_{ALM2}	Extension DSTBn (No Reset)	35		µs	

Note 1: Data valid until DSTBn L/H-edge


tDINoff
D0..D3
data in
HI-Z
Direction of Input
tDINon
tDSTBL
D0..D3
data out LOW
HI-Z
Direction of Output
data out HIGH
D0..D3
HI-Z
tDSTBH
tDSTBL
D0..D3
data out
HI-Z
data in
HI-Z
tDATA
tDINon
tDINoff
Bidirectional
tDSTBH
D0..D3
data out
HI-Z
data in
HI-Z
tDSTB
DSTBn
tCYCLE
DSTB
(ext. LOW)
tALM2
tALM1
(tRESET1)

Interface to the ext. E2PROM (U5R, SCL, SDA) / functional, electrical and timing characteristics

Symbol	Parameter	min	max	Unit	Note
VU5R	Output Voltage to E²PROM	4.5	5.5	V	IU5R ≤ 3 mA
CU5R	Load Capacity to U5R	10	220	nF	Ceramics capacitor
IU5R	Output Current to U5R		3	mA	
VOL	Output Voltage “Low”	0	0.2 * VU5R	V	IOL = 10 µA
VOH	Output Voltage “High”	0.8 * VU5R	VU5R	V	-IOH = 10 µA
VIL	Input Voltage “Low” (only SDA)	-0.3	0.3 * VU5R	V	-IIL = 1.5...0.2mA
VIH	Input Voltage “High” (only SDA)	0.7 * VU5R	VU5R + 0.3	V	IIH = -1...1 µA
$t_{DATAinSU}$	Set-up Time for Data Input	0.25		µs	
$t_{DATAinHO}$	Hold Time for Data Input	0		µs	
t_{AA}	Time from SCK Low to SDA Data Out and ACK Out		3.5	µs	
$t_{DATAoutHO}$	Hold Time for Data Output	0.3		µs	
$t_{STARTSU}$	Set-up Time for Start Condition	4.7		µs	
$t_{STARTHO}$	Hold Time for Start Condition	4		µs	
t_{STOPSU}	Set-up Time for Stop Condition	4.7		µs	
t_{BUF}	Time which has to be Free for Bus: Before Next Transmission	4.7		µs	
t_R	Rise Time		1000	ns	
t_F	Fall Time		300	ns	
t_{LOW}	Impulse LOW Time	4700		ns	
t_{HIGH}	Impuls HIGH Time	4000		ns	
t_{SCL}	Clock Frequency for E²PROM		100	kHz	fc = 5.333 MHz



The U5R supply pin provides a typically 5V supply voltage to the external E²PROM, and has a biasing capability only for this purpose.
Programming of the E²PROM is possible with the E²PROM soldered-in into the ASI Slave unit's pc-board by accessing the SCL / SDA serial bus with an external programming hardware.

For successful programming the programmer hardware must have sink/source capability of at least 5 mA, and the ASI Slave IC's supply voltage LTGP has to be in the range of 26.65 V ...33.35 V.
The only E²PROM address locations which can be programmed through the ASI Slave IC (hence over the ASI Bus and by the ASI Master), are locations 0 and 1, which both have been reserved for the ASI Slave unit's address.

The E²PROM has to be programmed in the following way:

E²PROM Address	D7	D6	D5	D4	D3	D2	D1	D0	Initialization Data
0	0	0	0	ASI address					0
1	0	0	0	ASI address					0
2	ID Code			IO Configuration					Custom Specific Data
3	ID Code			IO Configuration					Custom Specific Data

Recommended E²PROM types:

Supplier	Type	Organization
Philips	PCA8581P	128 x 8
ST	ST24C01	128 x 8
Catalyst	CAT24LC02(Z)IP	256 x 8
Xicor	X24LC02PI	256 x 8
Catalyst	CAT24LC04(Z)IP	512 x 8
Xicor	X24(L)C04PI	512 x 8

Sensor / actuator supply pin UOUT / Functional and electrical characteristics

Symbol	Parameter	min	max	Unit	Note
VUOUT	Output Voltage at UOUT	VLTGP – VDROP min	VLTGP – VDROPmin	V	IUOUT = 35 mA
VUOUTp	Overswing of the Output Voltage		1.5	V	CUOUT = 10 µF: Switching 0-35 mA - 0
t_{UOUTP}	Overswing Impulse Width		2.	ms	
VDROP	Voltage Drop from LTGP to UOUT	5.5	6.7	V	
IUOUT	Output Current UOUT	0	35	mA	11.0 V < VUOUT < 27.6 V
CUOUT	Load Capacity UOUT	10	470	µF	

The interface is intended for the supply voltage to actuators, sensors as well as external circuits with a power supply of <35mA without overloading the ASI line in the range of the signal frequency. The ASI slave IC has an internal circuit protector which limits the current during the charging of the load capacitor and which effects a power down at thermal overload, e.g. at too high output currents.

In the case of a current break down on the ASI line of less than 1ms, the internally stored information is retained. The supply voltage of the IC during this time is extracted from the capacitor Pin UOUT which is interrupted from the ASI line.

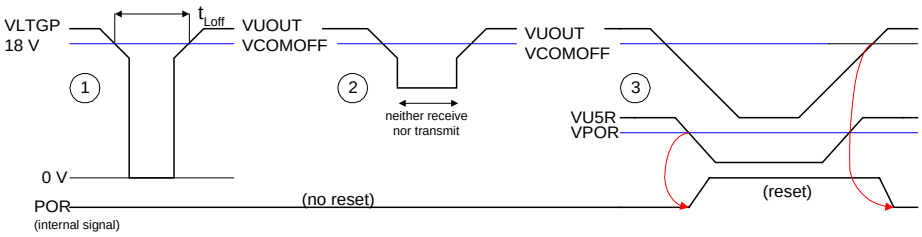
Reset Behaviour

The ASI Slave IC can be in reset condition or reset by the following events:

- at power-up of VLTGP: as long as VUOUT has not yet reached the treshold voltage 9 V ≤ VCOMOFF ≤ 11 V;
- at power-down of VLTGP: as soon as U5R drops below the treshold voltage 3.5 V ≤ VPOR ≤ 4 V;
- by a 'L' input level to DSTBn for more than 44 µs;
- resulting from a "Reset ASI Slave"- command by the ASI Master over the ASI BUS.

The different levels of VCOMOFF and VPOR as per a) and b) and the fact that the U5R supply voltage results from a down-regulation of the VUOUT supply assure a desirable hysteresis in the order of several volts between the VUOUT power-on-reset and power-down-reset threshold. Whereas at power-up the ASI Slave IC is released from reset by VUOUT reaching a level of between 9 V and 11 V, at power-down VUOUT has to come down to a level in the order of 5 V for U5R to drop into the reset-triggering window between 3.5 V and 4 V.

Some different power-down events are illustrated below:



Notes:

as to (1): No reset will be triggered, if VLTGP is lower than 18 V for less than 1 ms

as to (2): If VUOUT < VCOMOFF but still U5R > VPOR, communication over the Data Port is inhibited, but no reset triggered

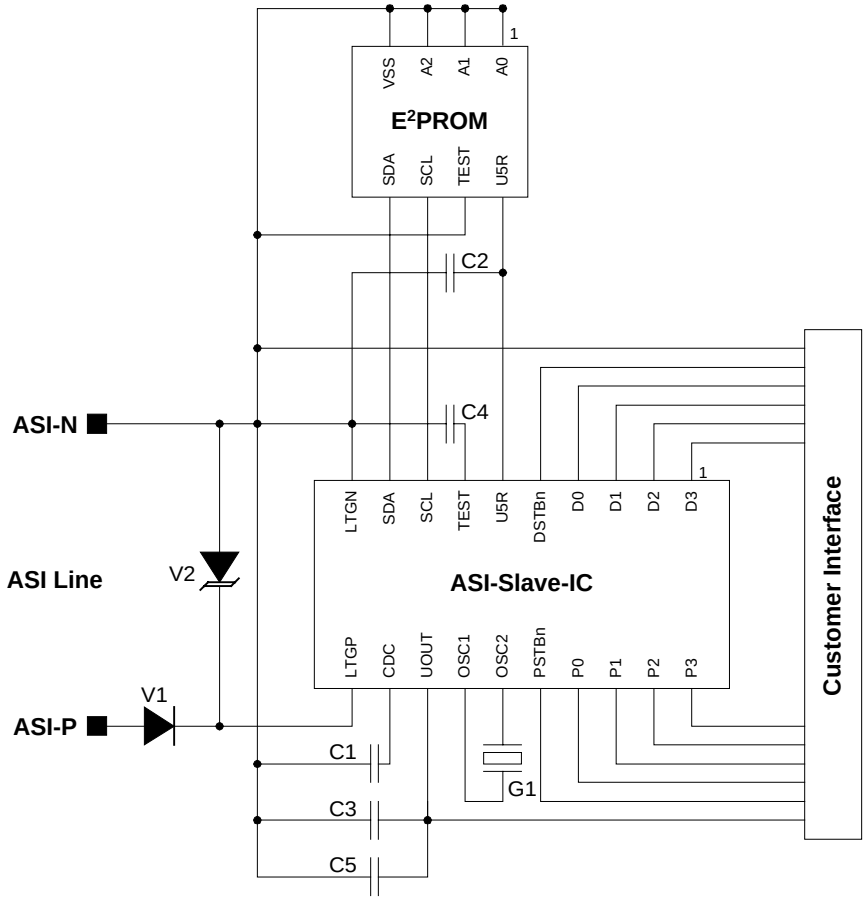
as to (3): If U5R < VPOR (resulting from VUOUT << VCOMOFF), a reset is triggered. Reset is overcome as soon as VUOUT > VCOMOFF (implying U5R > VPOR)

In reset condition internal registers are cleared and data port D0...D3 is switched into high-impedant condition. After release from reset the ASI Slave automatically performs a first read cycle to clear the E^2PROM from any previously interrupted communication state and a second one to load the ASI address, IO Configuration and ID Code into its internal registers.

Symbol	Parameter	min	max	Unit	Note
t reset	Reset Time after the Master Command "Reset ASI Slave" or DSTBn = ext. L/H-Edge		2	ms	
t reset2	Reset Time after Power On		30	ms	
t reset3	Reset Time after Power On with great Load Capacity		1000	ms	CUOUT = 470 µF
t Loff	Voltage Breakdown Time		1	ms	CUOUT > 10 µF
VCOMMoff	Voltage for "Communication OFF"	9	11	V	
VPOR	Voltage for Internal Reset	3.5	4	V	

Application Example 1:

Sensor/actuator circuit supplied by the ASI Slave IC (UOUT) for supply current needs ≤ 35 mA.



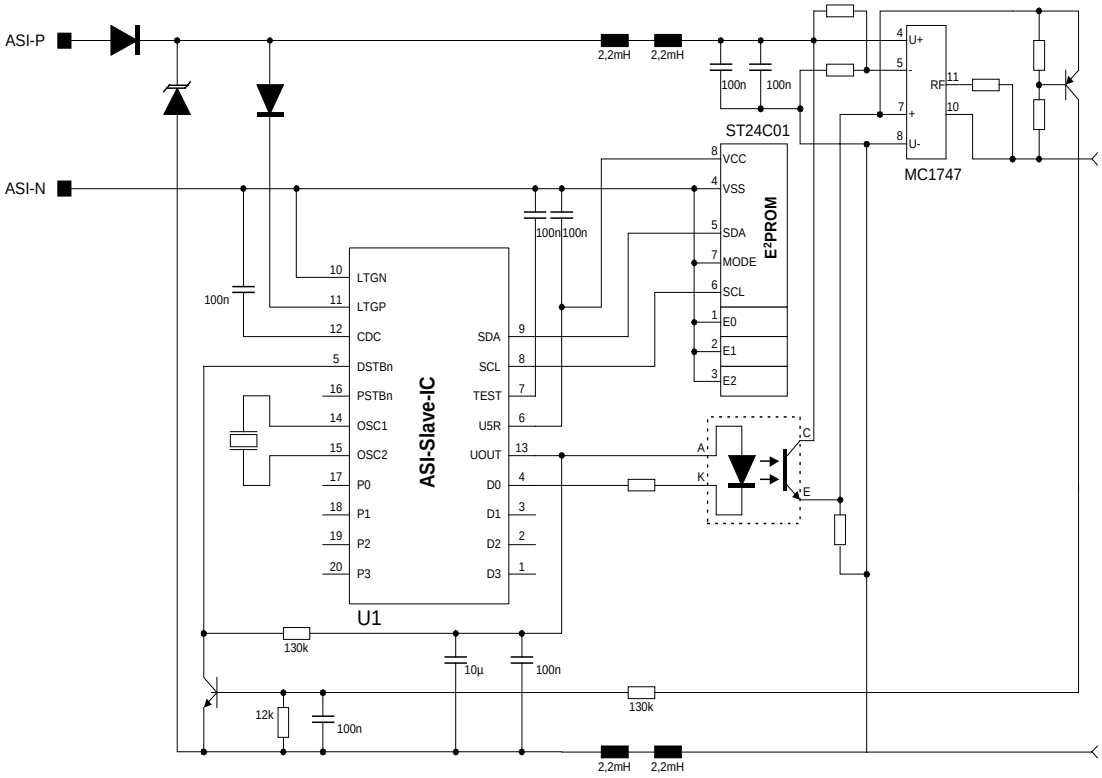
C1 = 22...470 nF / max. ASI BUS DC voltage
C2 = 10...220 nF / max VU5R = 5.5 V
C3 = 10...470 µF / max. (VUOUT + VUOUTp) = 29.1 V
C4 = 22...100 nF / max. (VUOUT + VUOUTp + 1.4 V) = 30.5 V
C5 = 10...100 nF (close to the IC) / max. (VUOUT + VUOUTp) = 29.1 V
V1 = 1N4002 or equivalent
V2 = TGL 41-39A or equivalent
G1 = ASI Crystal 5.333 MHz

For V2 a limiter diode with a small capacitance value should be selected, to ensure that the ASI Bus can be operated with the maximum number of Slave units connected.

In a more general sense care should be taken that the pc board tracks and the external components between the ASI Bus and LTGP / LTGN contribute to the ASI Slave unit's input impedance inductively and highly resistively, rather than capacitively.

Application Example 2:

Sensor / actuator circuit supplied from the ASI Bus for supply current needs > 35 mA
It is recommended to protect the ASI Bus by a fuse in this set-up, if there is a high risk of excessive current extraction due to component failure (e.g.: MC1747 or other components in the sensor / actuator circuitry).



ASI Quartz 5.333 MHz

AS2701A works fine with the following crystal types:

Citizen	CM 309
Philips	SQ 4849

ASI quartz crystals are available from:

Endrich GmbH	Geyer electronic	Kinseki Europe GmbH
Dr. Ing. R. Mäder	J. Reichmann	
Hauptstr. 56	Camerloherstr. 71	Schirmer Str. 76
D-72202 Nagold	D-80689 München	D-40211 Düsseldorf
Tel.: +49-7452-6007-0	+49-89-546868-0	+49-211-36815-0
Fax: +49-7452-1470	+49-89-546868-90	+49-211-36815-10

Application Support

a) For general information and documentation on the ASI concept you may contact the following local ASI Association:

AS-International Association
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D-63571 Gelnhausen
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Tel.: +46-340629-270
Fax: +46-340677-190
e-mail: lars.mattson@marknadspartnermol.se

b) A demoboard, equipped with AS2701A and supporting discrete components, is available from:

Bihl & Wiedemann GmbH
Mr. Bihl
Käfertaler Straße 164
D-68167 Mannheim
Tel.: +49-621-339-2723
Fax: +49-621-339-2239

Leuze electronic GmbH
Mr. Keller
In der Braike 1
D-73277 Owen/Teck
Tel.: +49-7021-573-248
Fax: +49-8021-573-200

c) Technical hotline assistance is provided by:

Bihl & Wiedemann GmbH (see above)

Bibliography

ASI: The Actuator-Sensor-Interface for Automation
Edts.: Werner Kriesel, Otto W. Madelung
Carl Hanser Verlag, Munich and Vienna, 1995
ISBN: 3-446-18265-9

Ordering Information

AS2701A	Package: SOIC 20	Delivery: tubes
AS2701AT	Package: SOIC 20	Delivery: Tape & Reel

Contact

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