

# Quad PLL Programmable Clock Generator with Spread Spectrum

## Features

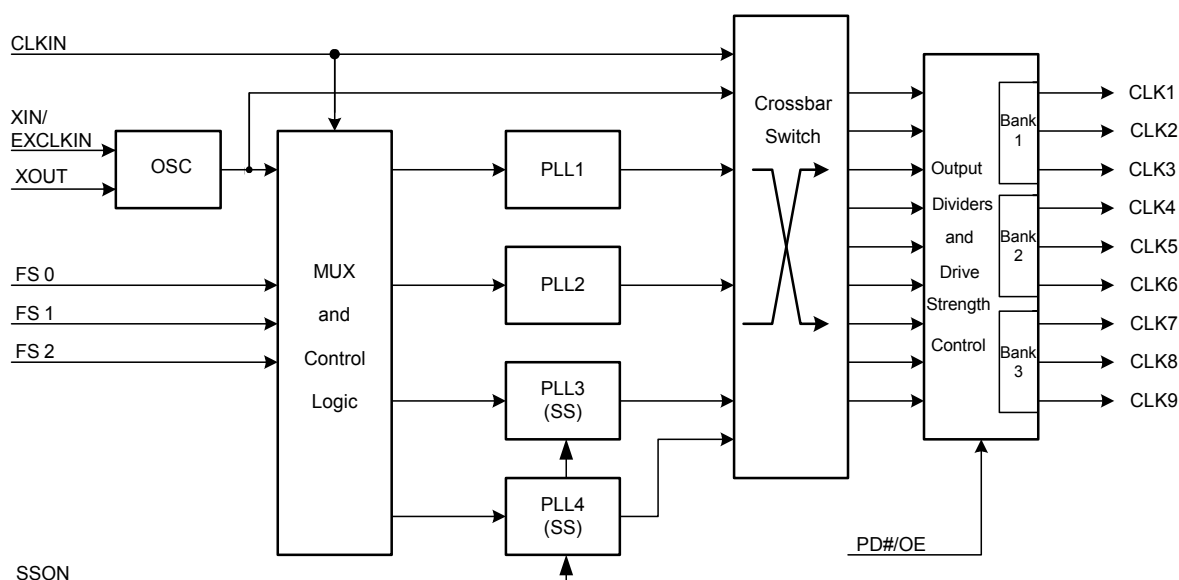
- Four fully integrated phase locked loops (PLLs)
  - External crystal: 8 to 48 MHz for CY2544 and CY2546
  - External reference: 8 to 166 MHz clock
- Reference clock input voltage range
  - 2.5 V, 3.0 V, and 3.3 V for CY2548
  - 1.8 V for CY2544 and CY2546
- Wide operating output frequency range
  - 3 to 166 MHz
- Programmable spread spectrum with center and down spread option and Lexmark and Linear modulation profiles
- VDD supply voltage options:
  - 2.5 V, 3.0 V, and 3.3 V for CY2544 and CY2548
  - 1.8 V for CY2546
- Selectable output clock voltages:
  - 2.5 V, 3.0 V, and 3.3 V for CY2544 and CY2548
  - 1.8 V for CY2546
- Frequency select feature with option to select eight different frequencies over nine clock outputs
- Power down, output enable, and SS ON/OFF controls
- Low jitter, high accuracy outputs

- Ability to synthesize nonstandard frequencies with Fractional-N capability
- Up to nine clock outputs with programmable drive strength
- Glitch free outputs while frequency switching
- 24-pin QFN package
- Commercial and Industrial temperature ranges

## Benefits

- Multiple high performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for personalization of PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Application specific programmable EMI reduction using spread spectrum for clocks
- Programmable PLLs for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitability for PC, consumer, portable, and networking applications
- Capable of Zero PPM frequency synthesis error
- Uninterrupted system operation during clock frequency switch
- Application compatibility in standard and low power systems
- For a complete list of related documentation, click [here](#).

## Logic Block Diagram



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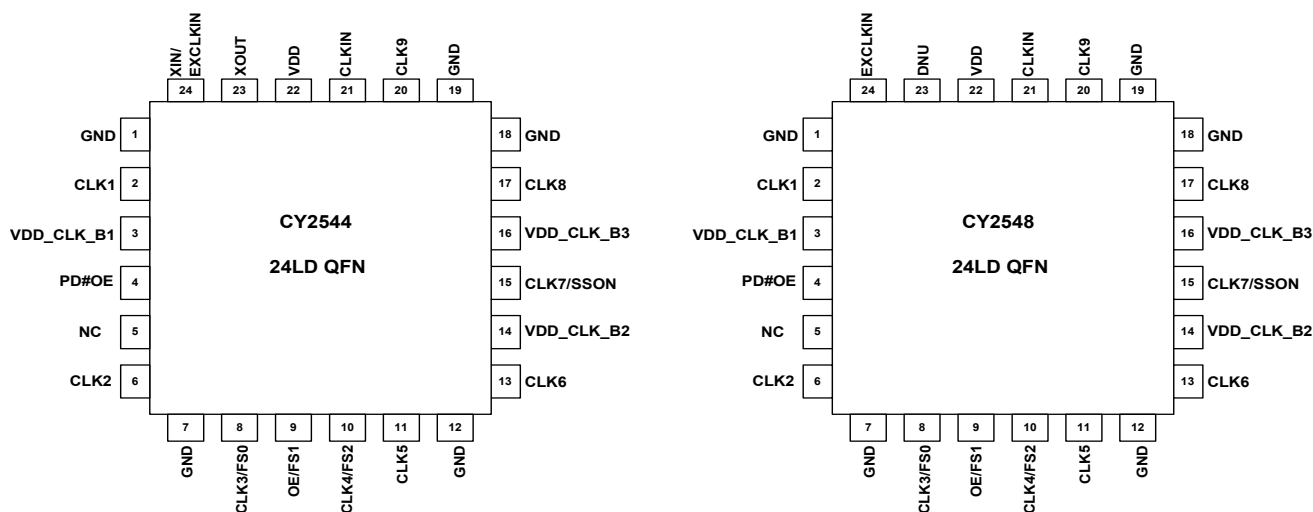
## Device Selection Guide

| Device | Crystal Input | EXCKLKIN Input             | CLKIN Input                | VDD                 | VDD_CLK_BX          |
|--------|---------------|----------------------------|----------------------------|---------------------|---------------------|
| CY2544 | Yes           | 1.8 V LVCMOS               | 2.5 V, 3.0 V, 3.3 V LVCMOS | 2.5 V, 3.0 V, 3.3 V | 2.5 V, 3.0 V, 3.3 V |
| CY2546 | Yes           | 1.8 V LVCMOS               | 1.8 V LVCMOS               | 1.8 V               | 1.8 V               |
| CY2548 | No            | 2.5 V, 3.0 V, 3.3 V LVCMOS | 2.5 V, 3.0 V, 3.3 V LVCMOS | 2.5 V, 3.0 V, 3.3 V | 2.5 V, 3.0 V, 3.3 V |

## Pinout

Figure 1. 24-pin QFN pinout

CY2544 / CY2548



## Pin Definitions

CY2544/CY2548 (VDD = 2.5 V, 3.0 V or 3.3 V Supply)

| Pin Number | Name       | I/O          | Description                                                                                                                                          |
|------------|------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | GND        | Power        | <b>Power supply ground</b>                                                                                                                           |
| 2          | CLK1       | Output       | <b>Programmable clock output.</b> Output voltage depends on VDD_CLK_B1 voltage                                                                       |
| 3          | VDD_CLK_B1 | Power        | <b>Power supply for bank1, (CLK1, CLK2, CLK3) Outputs:</b> 2.5 V/3.0 V/3.3 V                                                                         |
| 4          | PD#/OE     | Input        | <b>Multifunction programmable pin.</b> Output enable or power-down mode                                                                              |
| 5          | NC         | NC           | <b>No Connect</b>                                                                                                                                    |
| 6          | CLK2       | Output       | <b>Programmable Clock Output.</b> Output voltage depends on VDD_CLK_B1 voltage                                                                       |
| 7          | GND        | Power        | <b>Power supply ground</b>                                                                                                                           |
| 8          | CLK3/FS0   | Output/input | <b>Multifunction programmable pin.</b> Programmable clock output clock or frequency select pin. Output voltage of CLK3 depends on VDD_CLK_B1 voltage |
| 9          | OE/FS1     | Input        | <b>Multifunction programmable pin.</b> Output enable or frequency select pin                                                                         |
| 10         | CLK4/FS2   | Output/input | <b>Multifunction programmable pin.</b> Programmable clock output or frequency select input pin. Output voltage of CLK4 depends on VDD_CLK_B2 voltage |

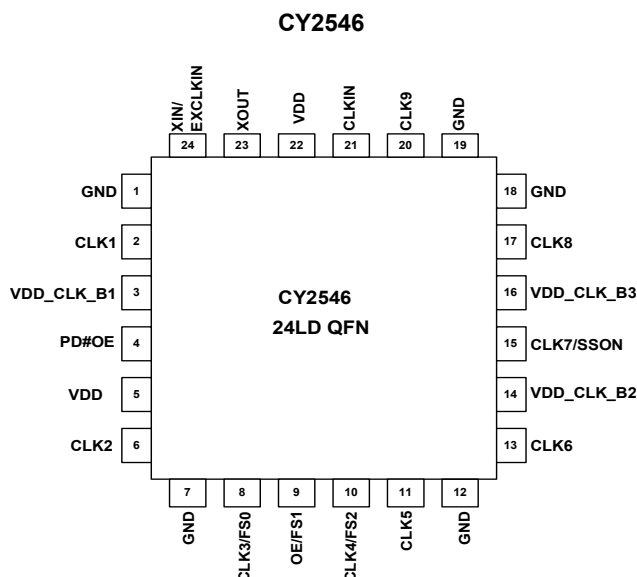
## Pin Definitions (continued)

CY2544/CY2548 (VDD = 2.5 V, 3.0 V or 3.3 V Supply)

| Pin Number | Name        | I/O          | Description                                                                                                                                                   |
|------------|-------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11         | CLK5        | Output       | <b>Programmable clock output.</b> Output voltage depends on VDD_CLK_B2 voltage                                                                                |
| 12         | GND         | Power        | <b>Power supply ground</b>                                                                                                                                    |
| 13         | CLK6        | Output       | <b>Programmable clock output.</b> Output voltage depends on VDD_CLK_B2 voltage                                                                                |
| 14         | VDD_CLK_B2  | Power        | <b>Power supply for bank2, (CLK4, CLK5, CLK6) Outputs.</b> 2.5 V/3.0 V/3.3 V                                                                                  |
| 15         | CLK7/SSON   | Output/input | <b>Multifunction programmable pin.</b> Programmable clock output or spread spectrum ON/OFF control input pin. Output voltage of CLK7 depends on Bank3 voltage |
| 16         | VDD_CLK_B3  | Power        | <b>Power supply for bank3, (CLK7, CLK8, CLK9) Outputs.</b> 2.5 V/3.0 V/3.3 V                                                                                  |
| 17         | CLK8        | Output       | <b>Programmable output clock.</b> Output voltage depends on Bank3 voltage                                                                                     |
| 18         | GND         | Power        | <b>Power supply ground</b>                                                                                                                                    |
| 19         | GND         | Power        | <b>Power supply ground</b>                                                                                                                                    |
| 20         | CLK9        | Output       | <b>Programmable clock output.</b> Output voltage depends on VDD_CLK_B3 voltage                                                                                |
| 21         | CLKIN       | Input        | <b>2.5 V/3.0 V/3.3 V reference clock input.</b> The signal level of CLKIN input must track VDD power supply on pin 22.                                        |
| 22         | VDD         | Power        | <b>Power supply.</b> 2.5 V/3.0 V/3.3 V                                                                                                                        |
| 23         | XOUT        | Output       | <b>Crystal output for CY2544</b>                                                                                                                              |
|            | DNU         | Output       | <b>Do not use this pin for CY2548</b>                                                                                                                         |
| 24         | XIN/EXCLKIN | Input        | <b>Crystal input or 1.8 V external clock input for CY2544</b>                                                                                                 |
|            | EXCLKIN     | Input        | <b>2.5 V/3.0 V/3.3 V external clock input for CY2548</b>                                                                                                      |

## Pinout

Figure 2. 24-pin QFN pinout



## Pin Definitions

CY2546 (VDD = 1.8 V Supply)

| Pin Number | Name        | I/O          | Description                                                                                                                                                        |
|------------|-------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | GND         | Power        | <b>Power supply ground</b>                                                                                                                                         |
| 2          | CLK1        | Output       | <b>Programmable clock output.</b> Output voltage depends on VDD_CLK_B1 voltage                                                                                     |
| 3          | VDD_CLK_B1  | Power        | <b>Power supply for bank1, (CLK1, CLK2, CLK3) Outputs.</b> 1.8 V                                                                                                   |
| 4          | PD#/OE      | Input        | <b>Multifunction programmable pin.</b> Output enable or power down mode                                                                                            |
| 5          | VDD         | Power        | <b>Power supply.</b> 1.8 V                                                                                                                                         |
| 6          | CLK2        | Output       | <b>Programmable clock output.</b> Output voltage depends on VDD_CLK_B1 voltage                                                                                     |
| 7          | GND         | Power        | <b>Power supply ground</b>                                                                                                                                         |
| 8          | CLK3/FS0    | Output/Input | <b>Multifunction programmable pin.</b> Programmable clock output or frequency select input pin. Output voltage of CLK3 depends on VDD_CLK_B1 voltage               |
| 9          | OE/FS1      | Input        | <b>Multifunction programmable pin.</b> Output enable or frequency select pin                                                                                       |
| 10         | CLK4/FS2    | Output/Input | <b>Multifunction programmable pin.</b> Programmable clock output or frequency select input pin. Output voltage of CLK4 depends on VDD_CLK_B2 voltage               |
| 11         | CLK5        | Output       | <b>Programmable clock output.</b> Output voltage depends on VDD_CLK_B2 voltage                                                                                     |
| 12         | GND         | Power        | <b>Power supply ground</b>                                                                                                                                         |
| 13         | CLK6        | Output       | <b>Programmable clock output.</b> Output voltage depends on VDD_CLK_B2 voltage                                                                                     |
| 14         | VDD_CLK_B2  | Power        | <b>Power supply for bank2, (CLK4, CLK5, CLK6) Outputs.</b> 1.8 V                                                                                                   |
| 15         | CLK7/SSON   | Output/input | <b>Multifunction programmable pin.</b> Programmable clock output or spread spectrum ON/OFF control input pin. Output voltage of CLK7 depends on VDD_CLK_B3 voltage |
| 16         | VDD_CLK_B3  | Power        | <b>Power supply for bank3, (CLK7, CLK8, CLK9) Outputs.</b> 1.8 V                                                                                                   |
| 17         | CLK8        | Output       | <b>Programmable clock output.</b> Output voltage depends on VDD_CLK_B3 voltage                                                                                     |
| 18         | GND         | Power        | <b>Power supply ground</b>                                                                                                                                         |
| 19         | GND         | Power        | <b>Power supply ground</b>                                                                                                                                         |
| 20         | CLK9        | Output       | <b>Programmable clock output.</b> Output voltage depends on VDD_CLK_B3 voltage                                                                                     |
| 21         | CLKIN       | Input        | <b>External 1.8 V low voltage reference clock input</b>                                                                                                            |
| 22         | VDD         | Power        | <b>Power supply.</b> 1.8 V                                                                                                                                         |
| 23         | XOUT        | Output       | <b>Crystal output</b>                                                                                                                                              |
| 24         | XIN/EXCLKIN | Input        | <b>Crystal input or 1.8 V external clock input</b>                                                                                                                 |

## General Description

### Four Configurable PLLs

The CY2544, CY2548 and CY2546 have four programmable PLLs that can be used to generate output frequencies ranging from 3 to 166 MHz. The advantage of having four PLLs is that a single device generates up to four independent frequencies from a single crystal.

### Input Reference Clocks

The input to the CY2544, CY2548 and CY2546 can be either a crystal or a clock signal. The input frequency range for crystal (XIN) is 8 MHz to 48 MHz and that for external reference clock (EXCLKIN) is 8 MHz to 166 MHz. The voltage range for the reference clock input of CY2548 is 2.5 V/3.0 V/3.3 V while that

for CY2544 and CY2546 is 1.8 V. This gives user an option for this device to be compatible for different input clock voltage levels in the system.

There is provision for a secondary reference clock input, CLKIN with applied frequency range of 8 MHz to 166 MHz. When CLKIN signal at pin 21 is used as a reference input to the PLL, a valid signal at EXCLKIN (as specified in the AC and DC Electrical Specification table) must be present for the devices to operate properly.

### Multiple Power Supplies

These devices are designed to operate at internal supply voltage of 1.8 V. In the case of the high voltage part (CY2544/CY2548), an internal regulator is used to generate 1.8 V from the 2.5 V/3.0 V/3.3 V VDD supply voltage at pin 22. For the low

voltage part (CY2546), this internal regulator is bypassed and 1.8 V at VDD pin 22 is directly used.

### Output Bank Settings

There are nine clock outputs grouped in three output driver banks. The Bank 1, Bank 2, and Bank 3 correspond to (CLK1, CLK2, CLK3), (CLK4, CLK5, CLK6), and (CLK7, CLK8, CLK9) respectively. Separate power supplies are used for each of these banks and they can be any of 2.5 V, 3.0 V, or 3.3 V for CY2544/CY2548 and 1.8 V for CY2546 giving user multiple choice of output clock voltage levels.

### Output Source Selection

These devices have programmable input sources for each of its nine clock outputs (CLK1–9). There are six available clock sources for these outputs. These clock sources are: XIN/EXCLKIN, CLKIN, PLL1, PLL2, PLL3, or PLL4. Output clock source selection is done using four out of six crossbar switch. Thus, any one of these six available clock sources can be arbitrarily selected for the clock outputs. This gives user a flexibility to have up to four independent clock outputs.

### Spread Spectrum Control

Two of the four PLLs (PLL3 and PLL4) have spread spectrum capability for EMI reduction in the system. The device uses a Cypress proprietary PLL and spread spectrum clock (SSC) technology to synthesize and modulate the frequency of the PLL. The spread spectrum feature can be turned on or off using a multifunction control pin (CLK7/SSON). It can be programmed to either center spread range from  $\pm 0.125\%$  to  $\pm 2.50\%$  or down spread range from  $-0.25\%$  to  $-5.0\%$  with Lexmark or Linear profile.

### Frequency Select

There are three multifunction frequency select pins (FS0, FS1 and FS2) that provide an option to select eight different sets of frequencies among each of the four PLLs. Each output has programmable output divider options.

### Glitch-Free Frequency Switch

When the frequency select pin (FS) is used to switch frequency, the outputs are glitch-free provided frequency is switched using output dividers. This feature enables uninterrupted system operation while clock frequency is being switched.

### PD#/OE Mode

PD#/OE (Pin 4) can be programmed to operate as either power down (PD#) or output enable (OE) mode. PD# is a low-true input. If activated it shuts off the entire chip, resulting in minimum power consumption for the device. Setting this signal high brings the device in the operational mode with default register settings.

When this pin is programmed as Output Enable (OE), clock outputs can be enabled or disabled using OE (pin 4). Individual clock outputs can be programmed to be sensitive to this OE pin.

### Output Drive Strength

The DC drive strength of the individual clock output can be programmed for different values. Table 1 shows the typical rise and fall times for different drive strength settings.

**Table 1. Output Drive Strength**

| Output Drive Strength | Rise/Fall Time (ns)<br>(Typical Value) |
|-----------------------|----------------------------------------|
| Low                   | 6.8                                    |
| Mid Low               | 3.4                                    |
| Mid High              | 2.0                                    |
| High                  | 1.0                                    |

### Generic Configuration and Custom Frequency

There is a generic set of output frequencies available from the factory that can be used for the device evaluation purposes. The devices, CY2544, CY2548 and CY2546 can be custom programmed to any desired frequencies and listed features. For customer specific programming, please contact local Cypress Field application engineer (FAE) or sales representative.

## Absolute Maximum Conditions

| Parameter              | Description                       | Condition                   | Min  | Max                   | Unit |
|------------------------|-----------------------------------|-----------------------------|------|-----------------------|------|
| V <sub>DD</sub>        | Supply voltage for CY2544/CY2548  |                             | -0.5 | 4.5                   | V    |
| V <sub>DD</sub>        | Supply voltage for CY2546         |                             | -0.5 | 2.6                   | V    |
| V <sub>DD_CLK_BX</sub> | Output bank supply voltage        |                             | -0.5 | 4.5                   | V    |
| V <sub>IN</sub>        | Input voltage for CY2544/CY2548   | Relative to V <sub>SS</sub> | -0.5 | V <sub>DD</sub> + 0.5 | V    |
| V <sub>IN</sub>        | Input voltage for CY2546          | Relative to V <sub>SS</sub> | -0.5 | 2.2                   | V    |
| T <sub>S</sub>         | Temperature, storage              | Non functional              | -65  | +150                  | °C   |
| ESD <sub>HBM</sub>     | ESD protection (Human body model) | JEDEC EIA/JESD22-A114-E     | 2000 | –                     | V    |
| UL-94                  | Flammability rating               | V-0 at 1/8 in.              | –    | 10                    | ppm  |
| MSL                    | Moisture sensitivity level        |                             | 3    |                       |      |

## Recommended Operating Conditions

| Parameter              | Description                                                                                              | Min  | Typ | Max  | Unit |
|------------------------|----------------------------------------------------------------------------------------------------------|------|-----|------|------|
| V <sub>DD</sub>        | VDD Operating voltage for CY2544/CY2548                                                                  | 2.25 | –   | 3.60 | V    |
| V <sub>DD</sub>        | VDD Operating voltage for CY2546                                                                         | 1.65 | 1.8 | 1.95 | V    |
| V <sub>DD_CLK_BX</sub> | Output driver voltage for Bank 1, 2 and 3                                                                | 1.65 | –   | 3.60 | V    |
| T <sub>AC</sub>        | Commercial ambient temperature                                                                           | 0    | –   | +70  | °C   |
| T <sub>AI</sub>        | Industrial ambient temperature                                                                           | -40  | --  | +85  | °C   |
| C <sub>LOAD</sub>      | Maximum load capacitance                                                                                 | –    | –   | 15   | pF   |
| t <sub>PU</sub>        | Power up time for all V <sub>DD</sub> to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | –   | 500  | ms   |

## DC Electrical Specifications

| Parameter        | Description                                         | Conditions                                      | Min                          | Typ | Max                   | Unit |
|------------------|-----------------------------------------------------|-------------------------------------------------|------------------------------|-----|-----------------------|------|
| V <sub>OL</sub>  | Output low voltage                                  | I <sub>OL</sub> = 2 mA, drive strength = [00]   | –                            | –   | 0.4                   | V    |
|                  |                                                     | I <sub>OL</sub> = 3 mA, drive strength = [01]   |                              |     |                       |      |
|                  |                                                     | I <sub>OL</sub> = 7 mA, drive strength = [10]   |                              |     |                       |      |
|                  |                                                     | I <sub>OL</sub> = 12 mA, drive strength = [11]  |                              |     |                       |      |
| V <sub>OH</sub>  | Output high voltage                                 | I <sub>OH</sub> = -2 mA, drive strength = [00]  | V <sub>DD_CLK_BX</sub> - 0.4 | –   | –                     | V    |
|                  |                                                     | I <sub>OH</sub> = -3 mA, drive strength = [01]  |                              |     |                       |      |
|                  |                                                     | I <sub>OH</sub> = -7 mA, drive strength = [10]  |                              |     |                       |      |
|                  |                                                     | I <sub>OH</sub> = -12 mA, drive strength = [11] |                              |     |                       |      |
| V <sub>IL1</sub> | Input low voltage of PD#/OE, FS0, FS1, FS2 and SSON | –                                               | –                            | –   | 0.2 × V <sub>DD</sub> | V    |
| V <sub>IL2</sub> | Input low voltage of CLKIN for CY2544/CY2548        | –                                               | –                            | –   | 0.1 × V <sub>DD</sub> | V    |
| V <sub>IL3</sub> | Input low voltage of EXCLKIN for CY2544             | –                                               | –                            | –   | 0.15                  | V    |

## DC Electrical Specifications (continued)

| Parameter         | Description                                                              | Conditions                                         | Min                 | Typ | Max                 | Unit       |
|-------------------|--------------------------------------------------------------------------|----------------------------------------------------|---------------------|-----|---------------------|------------|
| $V_{IL4}$         | Input low voltage of EXCLKIN for CY2548                                  | —                                                  | —                   | —   | $0.1 \times V_{DD}$ | V          |
| $V_{IL5}$         | Input low voltage of CLKIN, EXCLKIN for CY2546                           | —                                                  | —                   | —   | $0.1 \times V_{DD}$ | V          |
| $V_{IH1}$         | Input high voltage of PD#/OE, FS0, FS1, FS2 and SSON                     | —                                                  | $0.8 \times V_{DD}$ | —   | —                   | V          |
| $V_{IH2}$         | Input high voltage of CLKIN for CY2544/CY2548                            | —                                                  | $0.9 \times V_{DD}$ | —   | —                   | V          |
| $V_{IH3}$         | Input high voltage of EXCLKIN for CY2544                                 | —                                                  | 1.6                 | —   | 2.2                 | V          |
| $V_{IH4}$         | Input high voltage of EXCLKIN for CY2548                                 | —                                                  | $0.9 \times V_{DD}$ | —   | —                   | V          |
| $V_{IH5}$         | Input high voltage of CLKIN, EXCLKIN for CY2546                          | —                                                  | $0.9 \times V_{DD}$ | —   | —                   | V          |
| $I_{IL1}$         | Input low current of PD#/OE and FS1                                      | $V_{IL} = 0$ V                                     | —                   | —   | 10                  | $\mu$ A    |
| $I_{IH1}$         | Input high current of PD#/OE and FS1                                     | $V_{IH} = V_{DD}$                                  | —                   | —   | 10                  | $\mu$ A    |
| $I_{IL2}$         | Input low current of SSON, FS0, and FS2                                  | $V_{IL} = 0$ V<br>(Internal pull dn = 160k typ)    | —                   | —   | 10                  | $\mu$ A    |
| $I_{IH2}$         | Input high current of SSON, FS0, and FS2                                 | $V_{IH} = V_{DD}$<br>(Internal pull dn = 160k typ) | 14                  | —   | 36                  | $\mu$ A    |
| $R_{DN}$          | Pull down resistor of SSON, FS0, FS2 and clocks (CLK1–CLK9) in off-state | Clock outputs in off-state by setting PD# = Low    | 100                 | 160 | 250                 | k $\Omega$ |
| $I_{DD}^{[1, 2]}$ | Supply current for CY2546                                                | PD# = High, No load                                | —                   | 20  | —                   | mA         |
|                   | Supply current for CY2544/CY2548                                         | PD# = High, No load                                | —                   | 22  | —                   | mA         |
| $I_{DDS}^{[1]}$   | Standby current                                                          | PD# = Low                                          | —                   | 3   | —                   | $\mu$ A    |
| $C_{IN}^{[1]}$    | Input capacitance                                                        | SSON, CLKIN, PD#/OE, FS0, FS1, and FS2 pins        | —                   | —   | 7                   | pF         |

### Notes

1. Guaranteed by design but not 100% tested.
2. Configuration dependent.



## AC Electrical Specifications

| Parameter                         | Description                                  | Conditions                                                                                                                                 | Min | Typ | Max | Unit |
|-----------------------------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| F <sub>IN</sub> (crystal)         | Crystal frequency, XIN                       | —                                                                                                                                          | 8   | —   | 48  | MHz  |
| F <sub>IN</sub> (clock)           | Input clock frequency (CLKIN or EXCLKIN)     | —                                                                                                                                          | 8   | —   | 166 | MHz  |
| F <sub>CLK</sub>                  | Output clock frequency                       | —                                                                                                                                          | 3   | —   | 166 | MHz  |
| DC1                               | Output duty cycle, All clocks except ref out | Duty cycle is defined in <a href="#">Figure 4</a> ; t <sub>1</sub> /t <sub>2</sub> , measured at 50% of V <sub>DD-CLK_BX</sub>             | 45  | 50  | 55  | %    |
| DC2                               | Ref Out clock duty cycle                     | Ref In Min 45%, Max 55%                                                                                                                    | 40  | —   | 60  | %    |
| T <sub>RF1</sub> <sup>[3]</sup>   | Output rise/fall Time                        | Measured from 20% to 80% of V <sub>DD-CLK_BX</sub> , as shown in <a href="#">Figure 5</a> , C <sub>LOAD</sub> = 15 pF, Drive strength [00] | —   | 6.8 | —   | ns   |
| T <sub>RF2</sub> <sup>[3]</sup>   | Output rise/fall time                        | Measured from 20% to 80% of V <sub>DD-CLK_BX</sub> , as shown in <a href="#">Figure 5</a> , C <sub>LOAD</sub> = 15 pF, Drive strength [01] | —   | 3.4 | —   | ns   |
| T <sub>RF3</sub> <sup>[3]</sup>   | Output rise/fall time                        | Measured from 20% to 80% of V <sub>DD-CLK_BX</sub> , as shown in <a href="#">Figure 5</a> , C <sub>LOAD</sub> = 15 pF, Drive strength [10] | —   | 2.0 | —   | ns   |
| T <sub>RF4</sub> <sup>[3]</sup>   | Output rise/fall time                        | Measured from 20% to 80% of V <sub>DD-CLK_BX</sub> , as shown in <a href="#">Figure 5</a> , C <sub>LOAD</sub> = 15 pF, Drive strength [11] | —   | 1.0 | —   | ns   |
| T <sub>CCJ</sub> <sup>[3,4]</sup> | Cycle-to-cycle Jitter (peak)                 | Configuration dependent. See <a href="#">Configuration Example for C-C Jitter</a>                                                          | —   | 150 | —   | ps   |
| T <sub>LOCK</sub> <sup>[3]</sup>  | PLL lock time                                | Measured from 90% of the applied power supply level                                                                                        | —   | 1   | 3   | ms   |

## Configuration Example for C-C Jitter

| Ref. Freq. (MHz) | CLK1 Output |                     | CLK2 Output |                     | CLK3 Output |                     | CLK4 Output |                     | CLK5 Output |                     |
|------------------|-------------|---------------------|-------------|---------------------|-------------|---------------------|-------------|---------------------|-------------|---------------------|
|                  | Freq. (MHz) | C-C Jitter Typ (ps) | Freq. (MHz) | C-C Jitter Typ (ps) | Freq. (MHz) | C-C Jitter Typ (ps) | Freq. (MHz) | C-C Jitter Typ (ps) | Freq. (MHz) | C-C Jitter Typ (ps) |
| 14.3181          | 8.0         | 134                 | 166         | 103                 | 48          | 92                  | 74.25       | 81                  | Not Used    |                     |
| 19.2             | 74.25       | 99                  | 166         | 94                  | 8           | 91                  | 27          | 110                 | 48          | 75                  |
| 27               | 48          | 67                  | 27          | 109                 | 166         | 103                 | 74.25       | 97                  | Not Used    |                     |
| 48               | 48          | 93                  | 27          | 123                 | 166         | 137                 | 166         | 138                 | 8           | 103                 |

## Recommended Crystal Specification

For SMD Package

| Parameter       | Description                                  | Range 1 | Range 2 | Range 3 | Unit |
|-----------------|----------------------------------------------|---------|---------|---------|------|
| F <sub>IN</sub> | Crystal frequency                            | 8–14    | 14–28   | 28–48   | MHz  |
| R1              | Maximum motional resistance (ESR)            | 135     | 50      | 30      | Ω    |
| CL              | Parallel load capacitance (see Note 3 below) | 8–18    | 8–14    | 8–12    | pF   |
| DL(max)         | Maximum crystal drive level                  | 300     | 300     | 300     | μW   |

### Notes

- Guaranteed by design but not 100% tested.
- Configuration dependent.

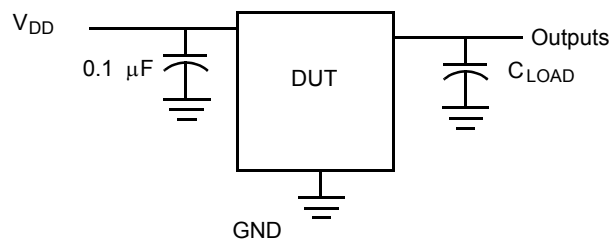
## Recommended Crystal Specification

For Thru-Hole Package

| Parameter <sup>[5]</sup> | Description                                  | Range 1 | Range 2 | Range 3 | Unit     |
|--------------------------|----------------------------------------------|---------|---------|---------|----------|
| $F_{IN}$                 | Crystal frequency                            | 8–14    | 14–24   | 24–32   | MHz      |
| R1                       | Maximum motional resistance (ESR)            | 90      | 50      | 30      | $\Omega$ |
| CL                       | Parallel load capacitance (see Note 6 below) | 8–18    | 8–12    | 8–12    | pF       |
| DL(max)                  | Maximum crystal drive level                  | 1000    | 1000    | 1000    | $\mu W$  |

## Test and Measurement Setup

Figure 3. Test and Measurement Setup



## Voltage and Timing Definitions

Figure 4. Duty Cycle Definition

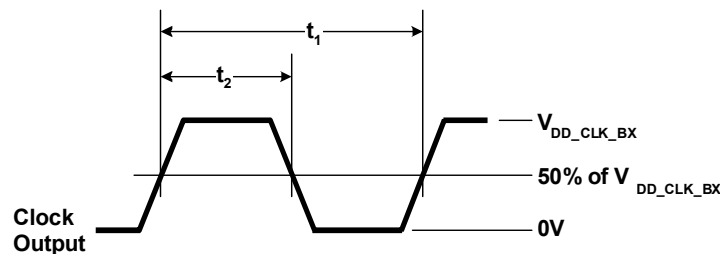
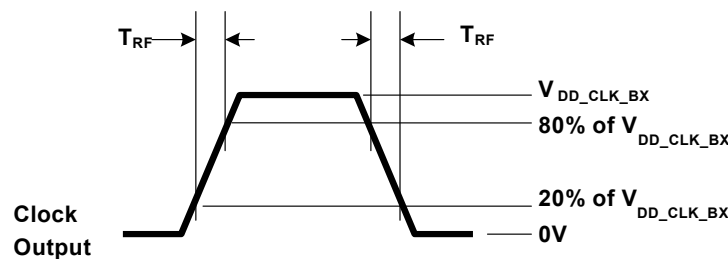


Figure 5. Rise Time =  $T_{RF}$ , Fall Time =  $T_{RF}$



### Notes

5. CY2544, CY2548 and CY2546 have internal crystal load capacitance (CL) adjustment feature.
6. Guaranteed by design but not 100% tested.

## Ordering Information

| Part Number       | Type <sup>[7]</sup>                                                    | Package                    | Supply Voltage        | Operating Range              |
|-------------------|------------------------------------------------------------------------|----------------------------|-----------------------|------------------------------|
| <b>Pb-free</b>    |                                                                        |                            |                       |                              |
| CY2544C           | Field Programmable                                                     | 24-pin QFN                 | 2.5 V, 3.0 V or 3.3 V | Commercial, 0 °C to 70 °C    |
| CY2544CT          | Field Programmable                                                     | 24-pin QFN – Tape and Reel | 2.5 V, 3.0V or 3.3 V  | Commercial, 0 °C to 70 °C    |
| CY2548C           | Field Programmable                                                     | 24-pin QFN                 | 2.5 V, 3.0V or 3.3 V  | Commercial, 0 °C to 70 °C    |
| CY2548CT          | Field Programmable                                                     | 24-pin QFN – Tape and Reel | 2.5 V, 3.0V or 3.3 V  | Commercial, 0 °C to 70 °C    |
| CY2546C           | Field Programmable                                                     | 24-pin QFN                 | 1.8 V                 | Commercial, 0 °C to 70 °C    |
| CY2546CT          | Field Programmable                                                     | 24-pin QFN – Tape and Reel | 1.8 V                 | Commercial, 0 °C to 70 °C    |
| CY2544I           | Field Programmable                                                     | 24-pin QFN                 | 2.5 V, 3.0 V or 3.3 V | Industrial, -40 °C to +85 °C |
| CY2544IT          | Field Programmable                                                     | 24-pin QFN – Tape and Reel | 2.5 V, 3.0 V or 3.3 V | Industrial, -40 °C to +85 °C |
| CY2548I           | Field Programmable                                                     | 24-pin QFN                 | 2.5 V, 3.0 V or 3.3 V | Industrial, -40 °C to +85 °C |
| CY2548IT          | Field Programmable                                                     | 24-pin QFN – Tape and Reel | 2.5 V, 3.0 V or 3.3 V | Industrial, -40 °C to +85 °C |
| CY2546I           | Field Programmable                                                     | 24-pin QFN                 | 1.8 V                 | Industrial, -40 °C to +85 °C |
| CY2546IT          | Field Programmable                                                     | 24-pin QFN – Tape and Reel | 1.8 V                 | Industrial, -40 °C to +85 °C |
| <b>Programmer</b> |                                                                        |                            |                       |                              |
| CY3675-CLKMAKER1  | Programming kit                                                        |                            |                       |                              |
| CY3675-QFN24A     | Socket adapter board, for programming CY2544 and CY2548 <sup>[8]</sup> |                            |                       |                              |

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

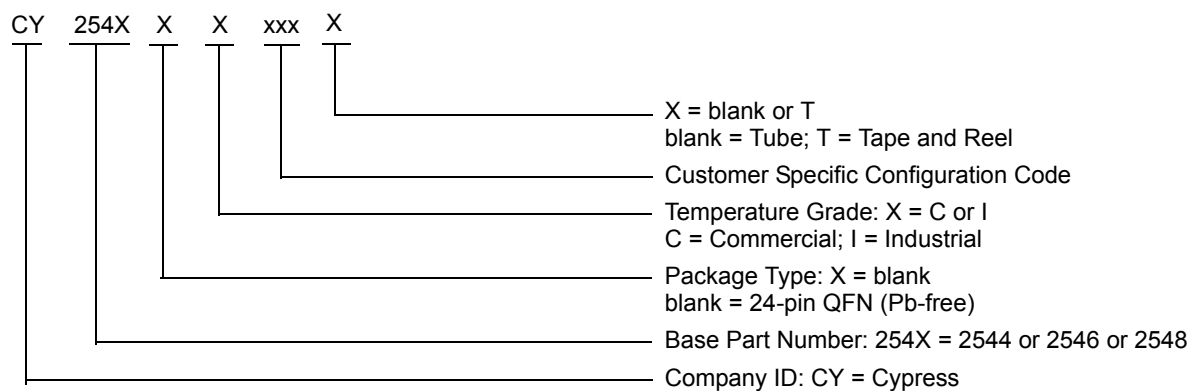
## Possible Configurations

| Part Number <sup>[9]</sup> | Type <sup>[7]</sup> | Package                    | Supply Voltage        | Operating Range              |
|----------------------------|---------------------|----------------------------|-----------------------|------------------------------|
| <b>Pb-free</b>             |                     |                            |                       |                              |
| CY2544Cxxx                 | Factory Programmed  | 24-pin QFN                 | 2.5 V, 3.0 V or 3.3 V | Commercial, 0 °C to 70 °C    |
| CY2544CxxxT                | Factory Programmed  | 24-pin QFN – Tape and Reel | 2.5 V, 3.0 V or 3.3 V | Commercial, 0 °C to 70 °C    |
| CY2548Cxxx                 | Factory Programmed  | 24-pin QFN                 | 2.5 V, 3.0 V or 3.3 V | Commercial, 0 °C to 70 °C    |
| CY2548CxxxT                | Factory Programmed  | 24-pin QFN – Tape and Reel | 2.5 V, 3.0 V or 3.3 V | Commercial, 0 °C to 70 °C    |
| CY2546Cxxx                 | Factory Programmed  | 24-pin QFN                 | 1.8 V                 | Commercial, 0 °C to 70 °C    |
| CY2546CxxxT                | Factory Programmed  | 24-pin QFN – Tape and Reel | 1.8 V                 | Commercial, 0 °C to 70 °C    |
| CY2544Ixxx                 | Factory Programmed  | 24-pin QFN                 | 2.5 V, 3.0 V or 3.3 V | Industrial, -40 °C to +85 °C |
| CY2544IxxxT                | Factory Programmed  | 24-pin QFN – Tape and Reel | 2.5 V, 3.0 V or 3.3 V | Industrial, -40 °C to +85 °C |
| CY2548Ixxx                 | Factory Programmed  | 24-pin QFN                 | 2.5 V, 3.0 V or 3.3 V | Industrial, -40 °C to +85 °C |
| CY2548IxxxT                | Factory Programmed  | 24-pin QFN – Tape and Reel | 2.5 V, 3.0 V or 3.3 V | Industrial, -40 °C to +85 °C |
| CY2546Ixxx                 | Factory Programmed  | 24-pin QFN                 | 1.8 V                 | Industrial, -40 °C to +85 °C |
| CY2546IxxxT                | Factory Programmed  | 24-pin QFN - Tape and Reel | 1.8 V                 | Industrial, -40 °C to +85 °C |

### Notes

- Field Programmable devices are shipped unprogrammed, and must be programmed before being installed on a board. Factory Programmed devices are shipped fully configured and ready to install on a board.
- The CY3675-QFN24A cannot be used to program the CY2546.
- "xxx" is a variable that denotes a specific device configuration. For more details, contact your local Cypress FAE or Cypress Sales Representative.

## Ordering Code Definitions





## Acronyms

| Acronym | Description                                         |
|---------|-----------------------------------------------------|
| DL      | Drive Level                                         |
| DNU     | Do Not Use                                          |
| DUT     | Device Under Test                                   |
| EIA     | Electronic Industries Alliance                      |
| EMI     | Electromagnetic Interference                        |
| ESD     | Electrostatic Discharge                             |
| FAE     | Field Application Engineer                          |
| FS      | Frequency Select                                    |
| JEDEC   | Joint Electron Devices Engineering Council          |
| LVC MOS | Low Voltage Complimentary Metal Oxide Semiconductor |
| OE      | Output Enable                                       |
| OSC     | Oscillator                                          |
| PD      | Power Down                                          |
| PLL     | Phase Locked Loop                                   |
| PPM     | Parts Per Million                                   |
| SS      | Spread Spectrum                                     |
| SSC     | Spread Spectrum Clock                               |
| SSON    | Spread Spectrum On                                  |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure   |
|--------|-------------------|
| °C     | degree Celsius    |
| fF     | femtofarad        |
| MHz    | megahertz         |
| μs     | microsecond       |
| μW     | microwatt         |
| mA     | milliampere       |
| ms     | millisecond       |
| ns     | nanosecond        |
| Ω      | ohm               |
| ppm    | parts per million |
| pF     | picofarad         |
| ps     | picosecond        |
| V      | volt              |
| W      | watt              |

## Document History Page

| Document Title: CY2544/CY2546/CY2548, Quad PLL Programmable Clock Generator with Spread Spectrum<br>Document Number: 001-12563 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                                       | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| **                                                                                                                             | 690257  | RGL             | See ECN         | New data sheet.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| *A                                                                                                                             | 790516  | RGL             | See ECN         | <p>Separated the Pin Configuration drawing into two to show the difference between CY2544 and CY2546 pinouts.</p> <p>Updated <a href="#">DC Electrical Specifications</a>:<br/> Updated Test Conditions of <math>I_{ILPDOE}</math> parameter (Replaced "Internal pull up = 100k typical" with "No Internal pull up").<br/> Changed maximum value of <math>I_{ILPDOE}</math> parameter from 10 <math>\mu A</math> to 1 <math>\mu A</math>.<br/> Updated Test Conditions of <math>I_{IHPDOE}</math> parameter (Replaced "Internal pull up = 100k typical" with "No Internal pull up").<br/> Updated Test Conditions of <math>I_{ILSR}</math> parameter (Replaced "Internal pull down = 100k typical" with "Internal pull down = 160k typical").<br/> Updated Test Conditions of <math>I_{IHSR}</math> parameter (Replaced "Internal pull down = 100k typical" with "Internal pull down = 160k typical").<br/> Changed the maximum value of <math>I_{IHSR}</math> parameter from 10 <math>\mu A</math> to 25 <math>\mu A</math>.<br/> Removed maximum value of <math>I_{DD}</math> parameter (22 mA).<br/> Added typical value of <math>I_{DD}</math> parameter (15 mA).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| *B                                                                                                                             | 1508943 | RGL / AESA      | See ECN         | <p>Changed status from Preliminary to Final.</p> <p>Added <a href="#">Device Selection Guide</a>.</p> <p>Updated <a href="#">Absolute Maximum Conditions</a>:<br/> Changed condition of <math>ESD_{HBM}</math> parameter from "MIL-STD-883, Method 3015" to "JEDEC EIA/JESD22-A114-E".</p> <p>Updated <a href="#">DC Electrical Specifications</a>:<br/> Removed <math>V_{IL}</math>, <math>V_{IH}</math>, <math>V_{ILX}</math>, <math>V_{IHx}</math> parameters and their details.<br/> Added <math>V_{IL1}</math>, <math>V_{IH1}</math>, <math>V_{IL2}</math>, <math>V_{IH2}</math>, <math>V_{IL3}</math>, <math>V_{IH3}</math>, <math>V_{IL4}</math>, <math>V_{IH4}</math>, <math>V_{IL5}</math>, <math>V_{IH5}</math> parameters and their details.<br/> Renamed <math>I_{ILPDOE}</math> parameter as <math>I_{IL1}</math>, updated test conditions and changed maximum value of the same parameter from 1 <math>\mu A</math> to 10 <math>\mu A</math>.<br/> Renamed <math>I_{IHPDOE}</math> parameter as <math>I_{IH1}</math>, updated test conditions and changed maximum value of the same parameter from 1 <math>\mu A</math> to 10 <math>\mu A</math>.<br/> Renamed <math>I_{ILSR}</math> parameter as <math>I_{IL2}</math> and changed maximum value of the same parameter from 1 <math>\mu A</math> to 10 <math>\mu A</math>.<br/> Renamed <math>I_{IHSR}</math> parameter as <math>I_{IH2}</math>, changed maximum value of the same parameter from 25 <math>\mu A</math> to 36 <math>\mu A</math> and also added minimum value of the same parameter as 14 <math>\mu A</math>.<br/> Added <math>R_{DN}</math> parameter and its details.<br/> Changed typical value of <math>I_{DDs}</math> value from 50 <math>\mu A</math> to 3 <math>\mu A</math>.</p> <p>Updated <a href="#">AC Electrical Specifications</a>:<br/> Added <math>T_{RF1}</math>, <math>T_{RF2}</math>, <math>T_{RF3}</math>, <math>T_{RF4}</math> parameters and their details.<br/> Renamed <math>T_{CCJ1}</math> parameter as <math>T_{CCJ}</math> and added typical value.<br/> Removed <math>T_{LTJ}</math> parameter and its details.</p> |
| *B (cont.)                                                                                                                     | 1508943 | RGL / AESA      | See ECN         | <p>Updated <a href="#">Configuration Example for C-C Jitter</a>:<br/> Removed details of "Long Term Jitter".<br/> Updated details corresponding to "Cycle-to-Cycle Jitter".</p> <p>Updated <a href="#">Recommended Crystal Specification</a>:<br/> Removed C0 parameter and its details.</p> <p>Updated <a href="#">Recommended Crystal Specification</a>:<br/> Removed C0 parameter and its details.</p> <p>Updated <a href="#">Ordering Information</a>:<br/> Deleted generic part numbers.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

## Document History Page (continued)

| Document Title: CY2544/CY2546/CY2548, Quad PLL Programmable Clock Generator with Spread Spectrum<br>Document Number: 001-12563 |         |                 |                 |                                                                                                                                                                      |
|--------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                                       | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                |
| *C                                                                                                                             | 2748211 | TSAI            | 08/10/09        | Post to external web.                                                                                                                                                |
| *D                                                                                                                             | 2764011 | CXQ             | 09/15/09        | Updated <a href="#">Ordering Information</a> :<br>Fixed typo (Changed CY2548Cxxx and CY2548CxxxT to CY2548lxxx and CY2548lxxxT for industrial temp parts).           |
| *E                                                                                                                             | 2899758 | KVM             | 03/26/10        | Updated <a href="#">Ordering Information</a> .<br>Updated <a href="#">Package Drawing and Dimensions</a> .<br>Updated copyright section.                             |
| *F                                                                                                                             | 2969587 | KVM             | 07/09/2010      | Minor change:<br>Added "with Spread Spectrum" in first page title to match spec title on the first page with spec title on the document history page.                |
| *G                                                                                                                             | 3115710 | BASH            | 12/21/2010      | Added <a href="#">Ordering Code Definitions</a> .<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .                                           |
| *H                                                                                                                             | 4239875 | CINM            | 01/08/2014      | Updated <a href="#">Package Drawing and Dimensions</a> :<br>spec 51-85203 – Changed revision from *B to *D.<br>Updated in new template.<br>Completing Sunset Review. |
| *I                                                                                                                             | 4586478 | AJU             | 03/12/2014      | Added related documentation hyperlink in page 1.                                                                                                                     |



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