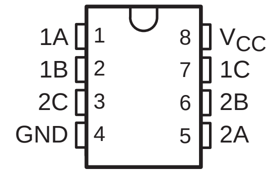
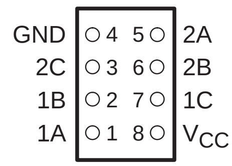
- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **1.65-V to 5.5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 0.8 ns at 3.3 V**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **High Speed, Typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)**
- **Rail-to-Rail Input/Output**
- **Low On-State Resistance, Typically ≈6 Ω (V_{CC} = 4.5 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DCT OR DCU PACKAGE (TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE (BOTTOM VIEW)



description/ordering information

This dual bilateral analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G66 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ − WCSP (DSBGA) 0.17-mm Small Bump − YEA	Reel of 3000	SN74LVC2G66YEAR	_ _ _C6_
	NanoFree™ − WCSP (DSBGA) 0.17-mm Small Bump − YZA (Pb-free)		SN74LVC2G66YZAR	
	NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP		SN74LVC2G66YEPR	
	NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free)		SN74LVC2G66YZPR	
	SSOP − DCT	Reel of 3000	SN74LVC2G66DCTR	C66_ _ _
	VSSOP − DCU	Reel of 3000	SN74LVC2G66DCUR	C66_
		Reel of 250	SN74LVC2G66DCUT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

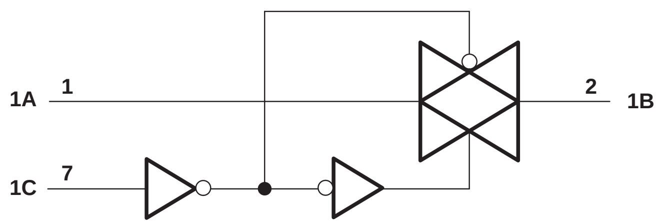
description/ordering information (continued)

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

FUNCTION TABLE
(each section)

CONTROL INPUT (C)	SWITCH
L	Off
H	On

logic diagram, each switch (positive logic)



One of Two Switches

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . −0.5 V to 6.5 V
Input voltage range, V_I (see Notes 1 and 2) . . . . −0.5 V to 6.5 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . −0.5 V to V_{CC} + 0.5 V
Control input clamp current, I_{IK} ($V_I < 0$) . . . . −50 mA
I/O port diode current, I_{IOK} ($V_{I/O} < 0$ or $V_{I/O} > V_{CC}$) . . . . ±50 mA
On-state switch current, I_T ($V_{I/O} = 0$ to V_{CC}) . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 4): DCT package . . . . 220°C/W
DCU package . . . . 227°C/W
YEA/YZA package . . . . 140°C/W
YEP/YZP package . . . . 102°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 5.5 V maximum.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 5)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	$V_{CC} \times 0.65$		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		$V_{CC} \times 0.35$	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature		−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
r_{on}	On-state switch resistance	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V		12.5	30	Ω
			I_S = 8 mA	2.3 V		9	20	
			I_S = 24 mA	3 V		7.5	15	
			I_S = 32 mA	4.5 V		6	10	
$r_{on(p)}$	Peak on-state resistance	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V		85	120	Ω
			I_S = 8 mA	2.3 V		22	30	
			I_S = 24 mA	3 V		12	20	
			I_S = 32 mA	4.5 V		7.5	15	
Δr_{on}	Difference of on-state resistance between switches	$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figures 1 and 2)	I_S = 4 mA	1.65 V			7	Ω
			I_S = 8 mA	2.3 V			5	
			I_S = 24 mA	3 V			3	
			I_S = 32 mA	4.5 V			2	
$I_{S(off)}$	Off-state switch leakage current	$V_I = V_{CC}$ and V_O = GND or V_I = GND and $V_O = V_{CC}$, $V_C = V_{IL}$ (see Figure 3)		5.5 V			±1	μA
							±0.1†	
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$, V_O = Open (see Figure 4)		5.5 V			±1	μA
							±0.1†	
I_I	Control input current	$V_C = V_{CC}$ or GND		5.5 V			±1	μA
							±0.1†	
I_{CC}	Supply current	$V_C = V_{CC}$ or GND		5.5 V			10	μA
							1†	
ΔI_{CC}	Supply-current change	$V_C = V_{CC} - 0.6$ V		5.5 V			500	μA
C_{ic}	Control input capacitance			5 V		3.5		pF
$C_{io(off)}$	Switch input/output capacitance			5 V		6		pF
$C_{io(on)}$	Switch input/output capacitance			5 V		14		pF

† $T_A = 25°C$

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}‡	A or B	B or A		2		1.2		0.8		0.6	ns
t_{en}§	C	A or B	2.3	10	1.6	5.6	1.5	4.4	1.3	3.9	ns
t_{dis}¶	C	A or B	2.5	10.5	1.2	6.9	2	7.2	1.1	6.3	ns

‡ t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
§ t_{PZL} and t_{PZH} are the same as t_{en}.
¶ t_{PLZ} and t_{PHZ} are the same as t_{dis}.

analog switch characteristics, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response† (switch on)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	35	MHz
				2.3 V	120	
				3 V	175	
				4.5 V	195	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	>300	
				2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
Crosstalk‡ (between switches)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	−58	dB
				2.3 V	−58	
				3 V	−58	
				4.5 V	−58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	1.65 V	−42	
				2.3 V	−42	
				3 V	−42	
				4.5 V	−42	
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	1.65 V	35	mV
				2.3 V	50	
				3 V	70	
				4.5 V	100	
Feed-through attenuation‡ (switch off)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	−58	dB
				2.3 V	−58	
				3 V	−58	
				4.5 V	−58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	1.65 V	−42	
				2.3 V	−42	
				3 V	−42	
				4.5 V	−42	
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	1.65 V	0.1	%
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	1.65 V	0.15	
				2.3 V	0.025	
				3 V	0.015	
				4.5 V	0.01	

† Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads −3 dB.
‡ Adjust f_{in} voltage to obtain 0 dBm at input.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	8	9	9.5	11	pF

PARAMETER MEASUREMENT INFORMATION

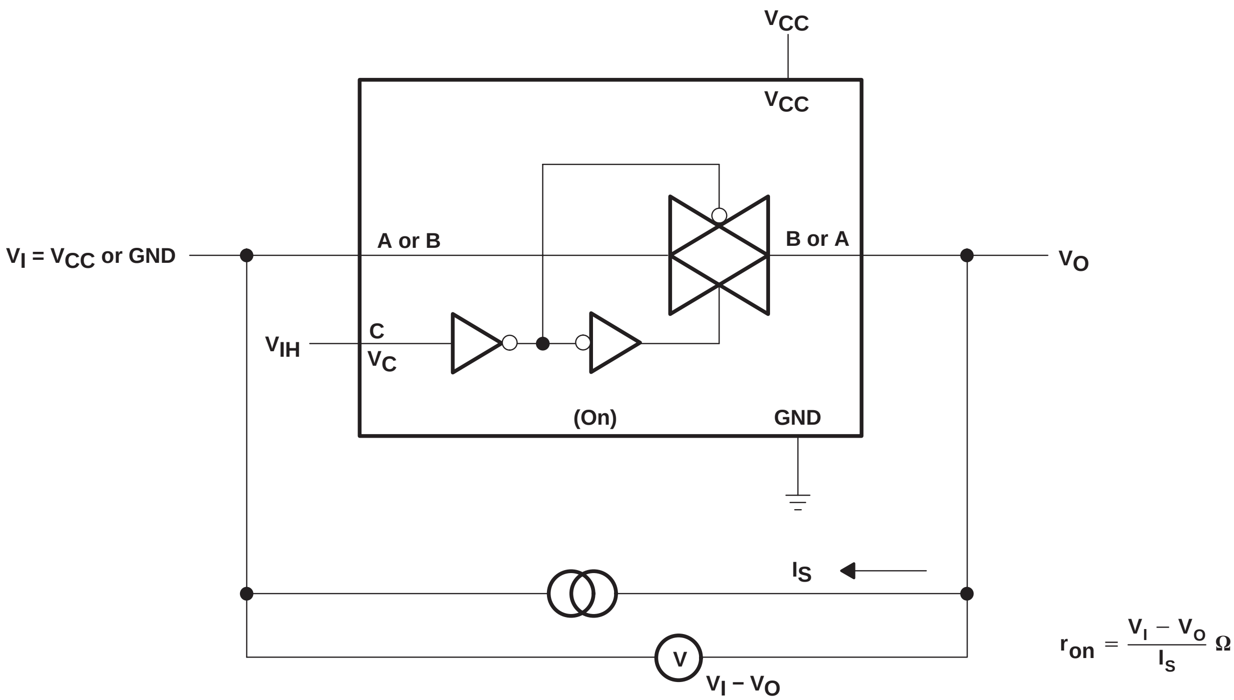


Figure 1. On-State Resistance Test Circuit

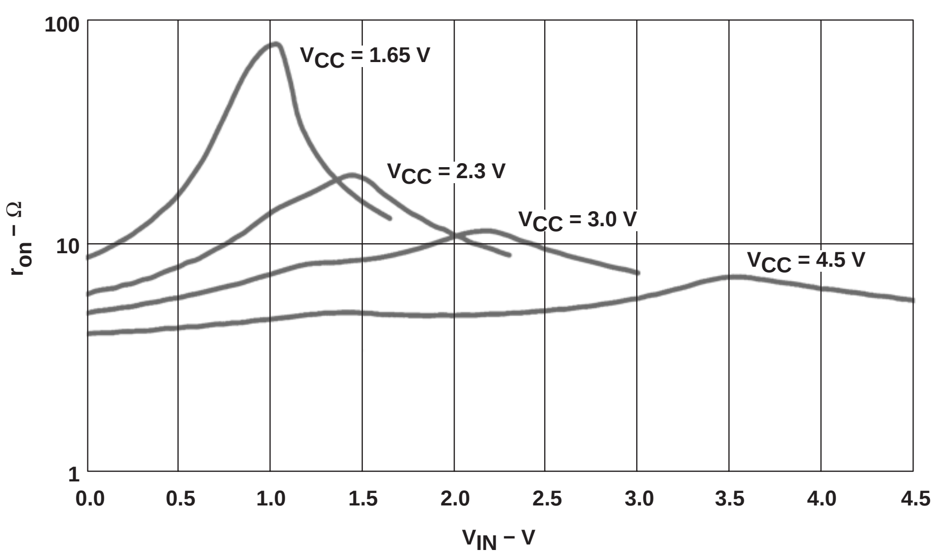


Figure 2. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

PARAMETER MEASUREMENT INFORMATION

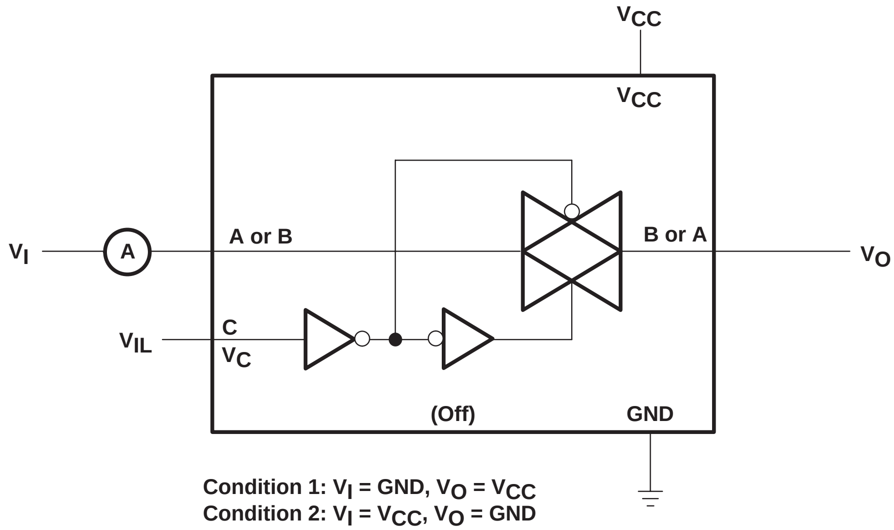


Figure 3. Off-State Switch Leakage-Current Test Circuit

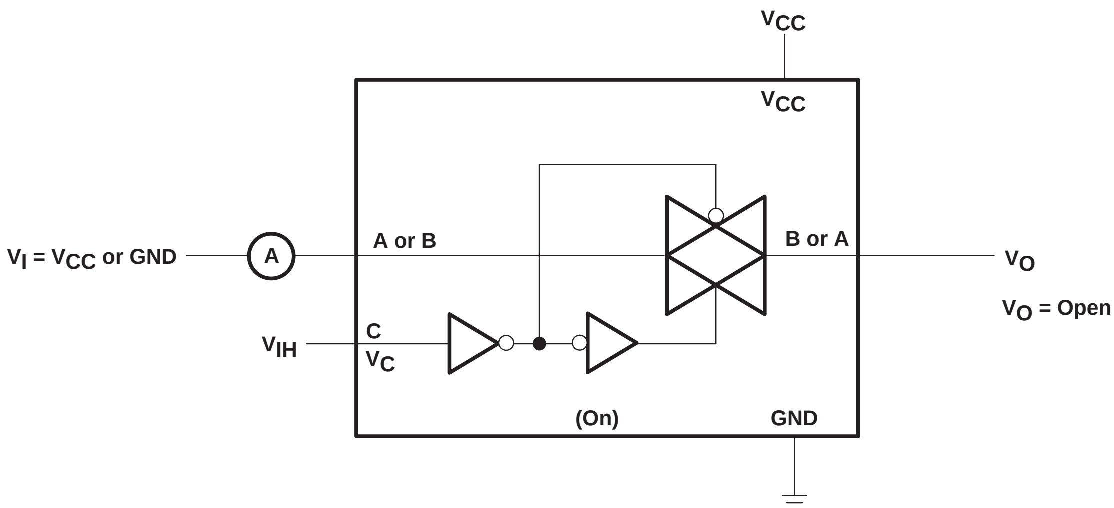
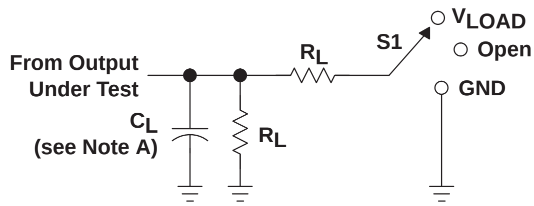


Figure 4. On-State Leakage-Current Test Circuit

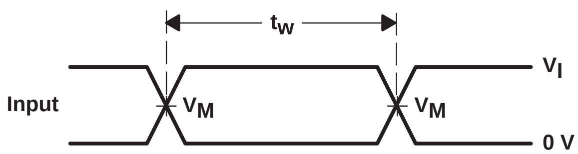
PARAMETER MEASUREMENT INFORMATION



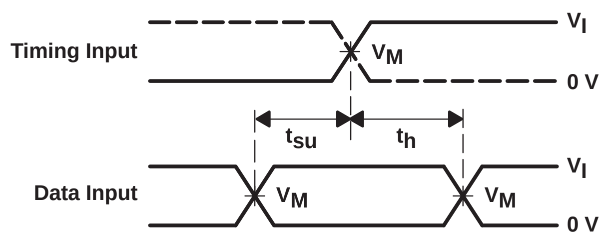
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

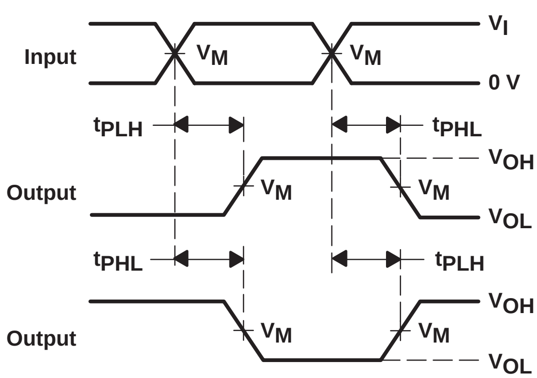
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



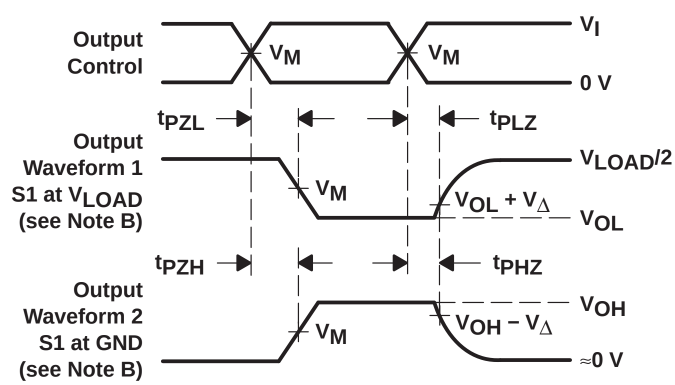
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

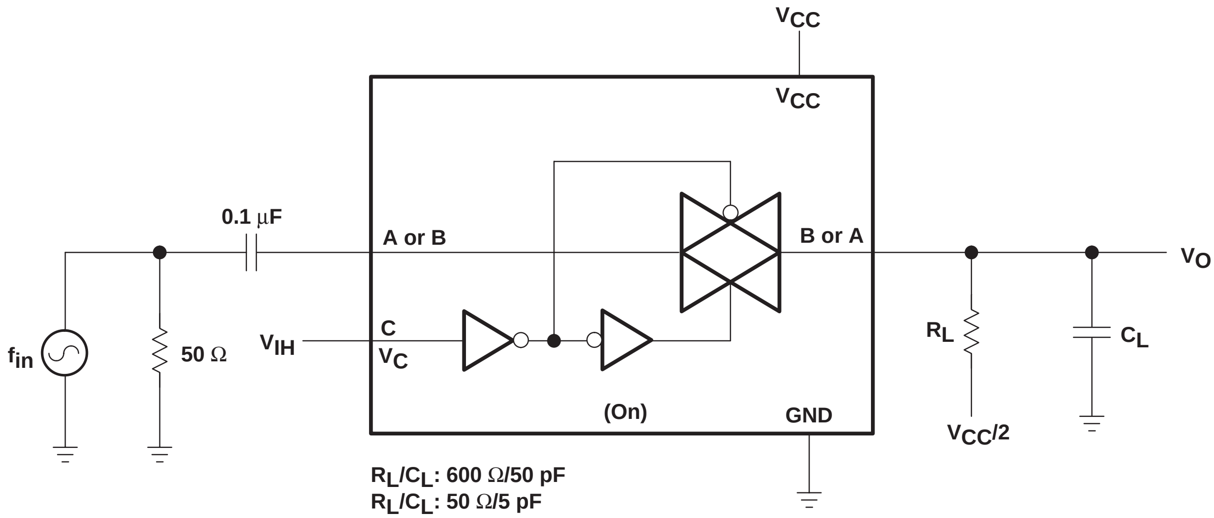


Figure 6. Frequency Response (Switch On)

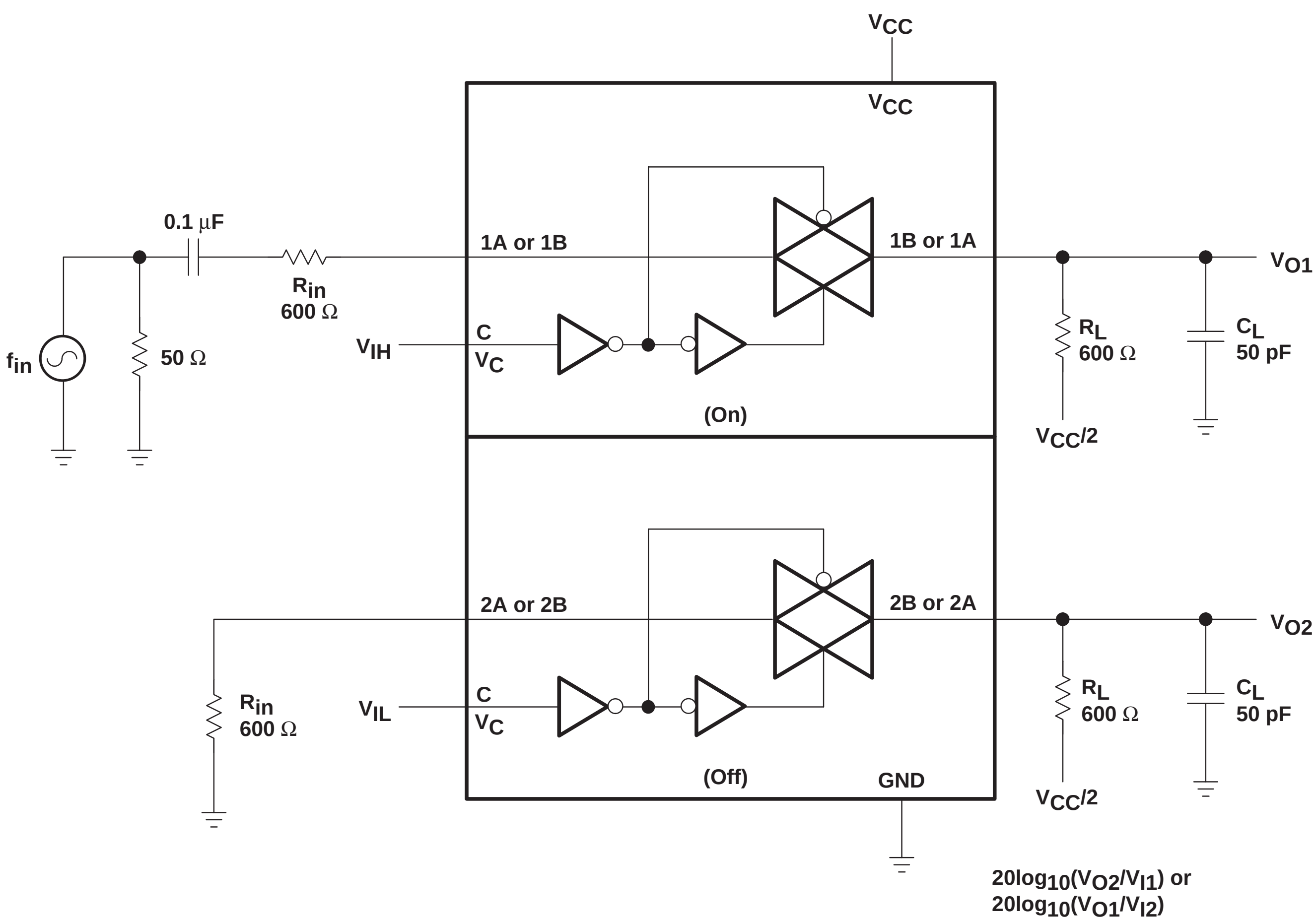


Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION

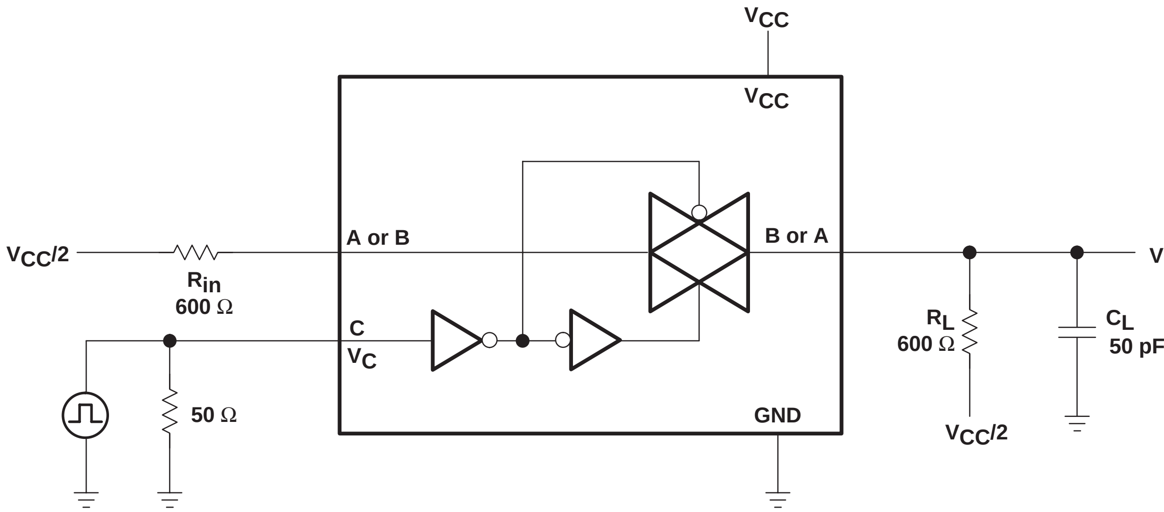


Figure 8. Crosstalk (Control Input, Switch Output)

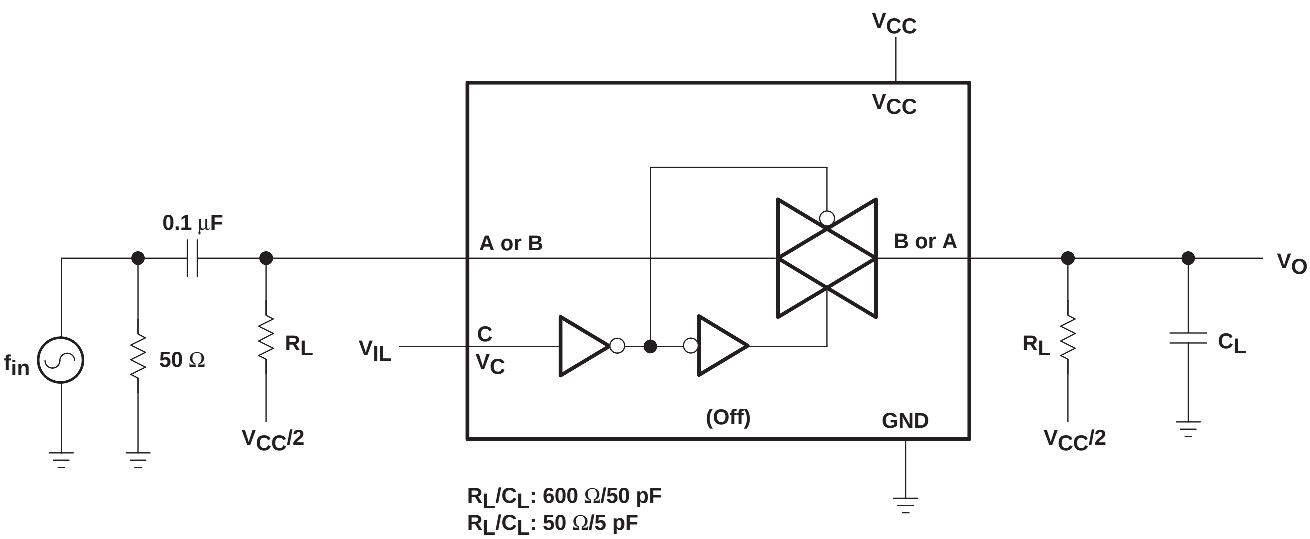
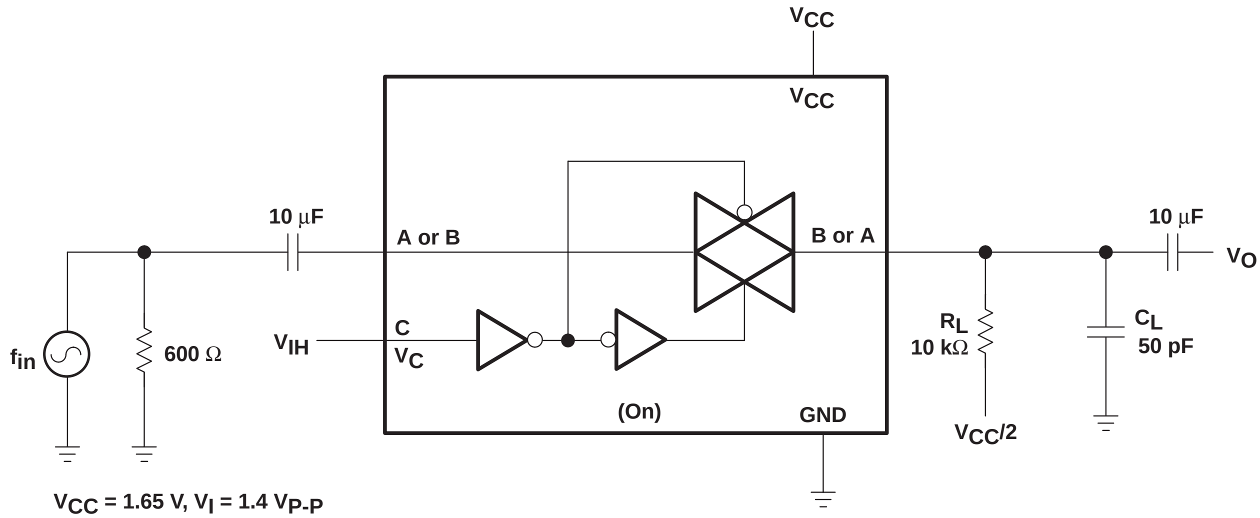


Figure 9. Feed Through (Switch Off)

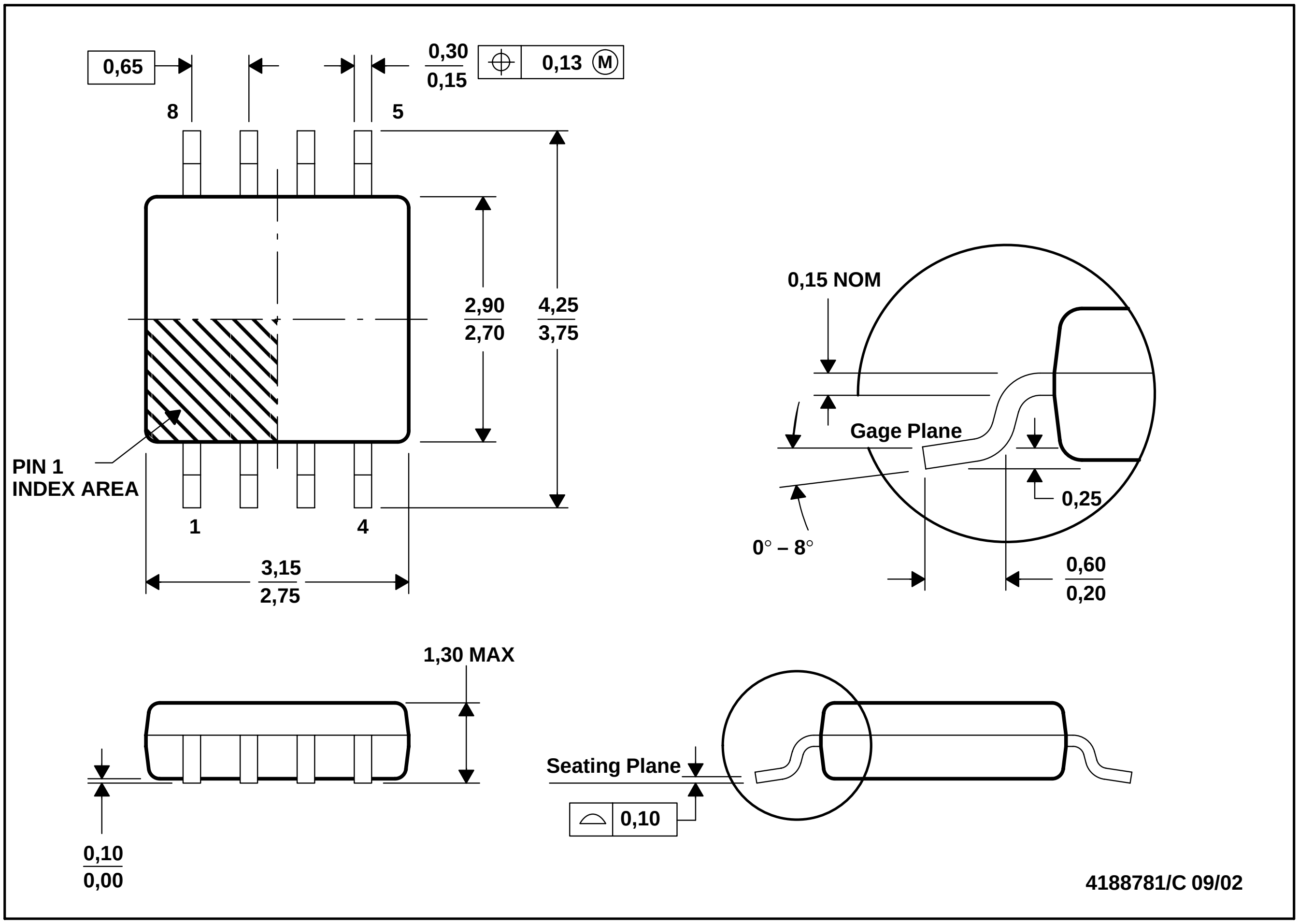
PARAMETER MEASUREMENT INFORMATION



V_{CC} = 1.65 V, V_I = 1.4 V_{P-P}
V_{CC} = 2.3 V, V_I = 2 V_{P-P}
V_{CC} = 3 V, V_I = 2.5 V_{P-P}
V_{CC} = 4.5 V, V_I = 4 V_{P-P}

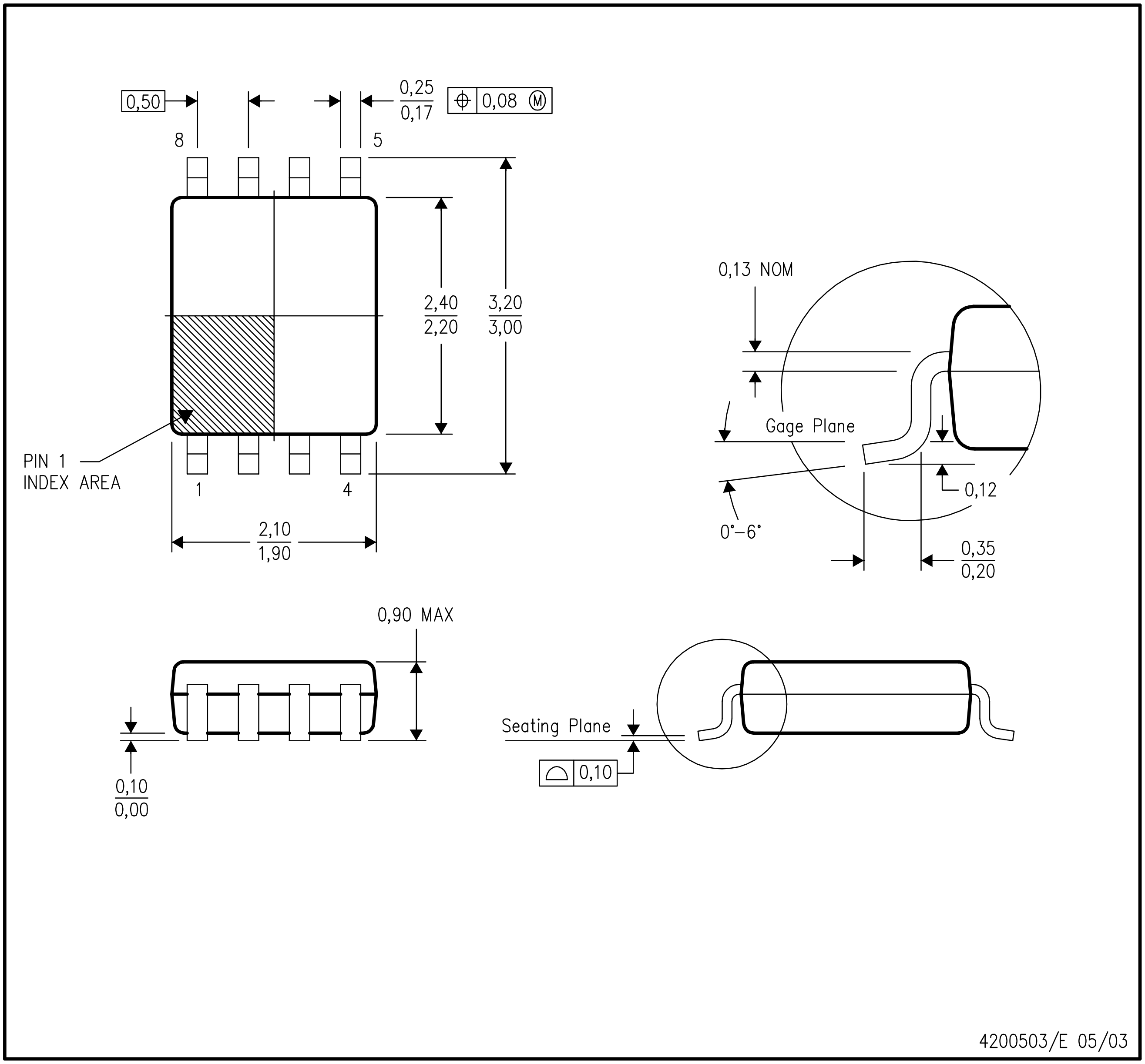
Figure 10. Sine-Wave Distortion

DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



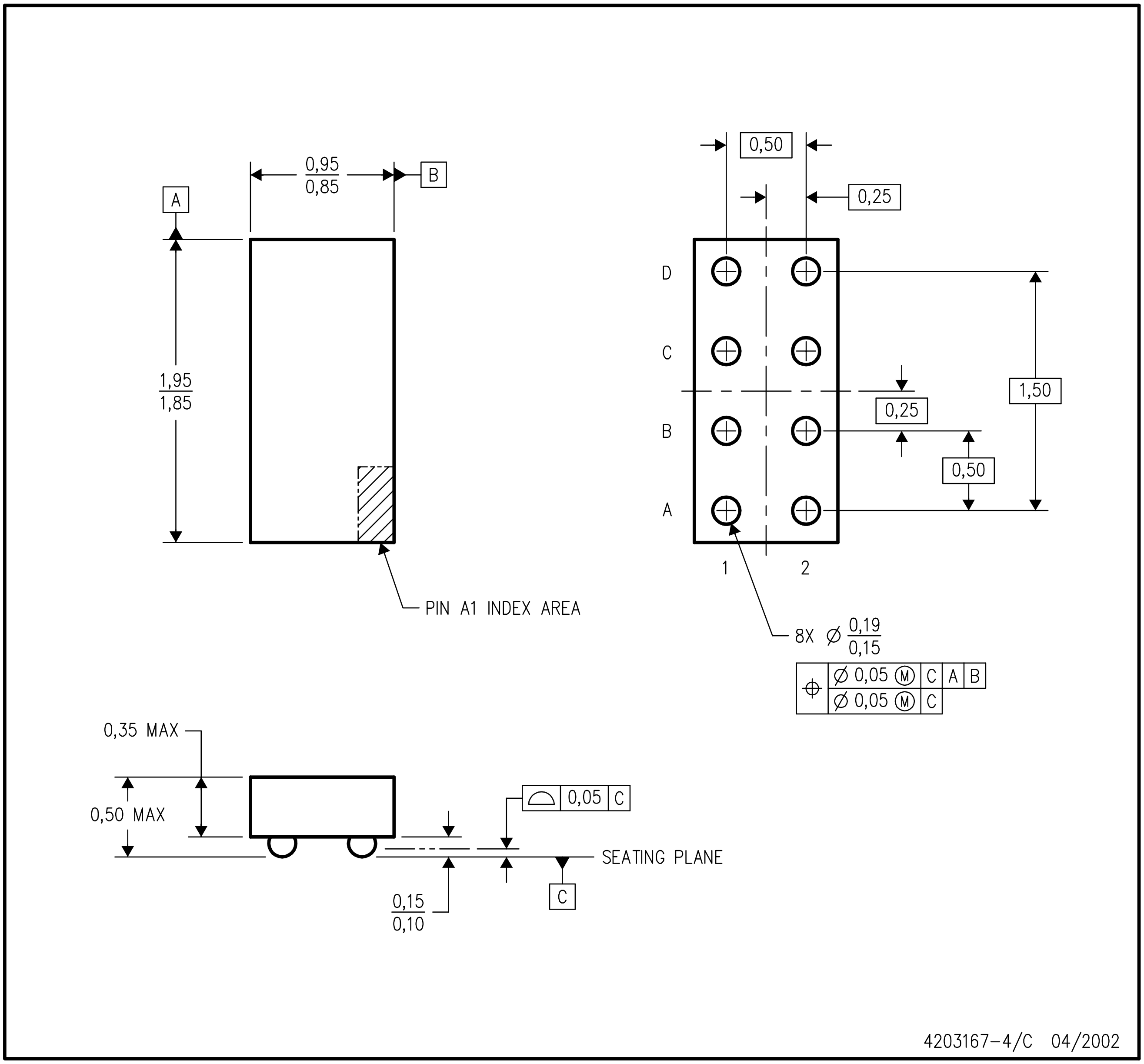
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation CA.

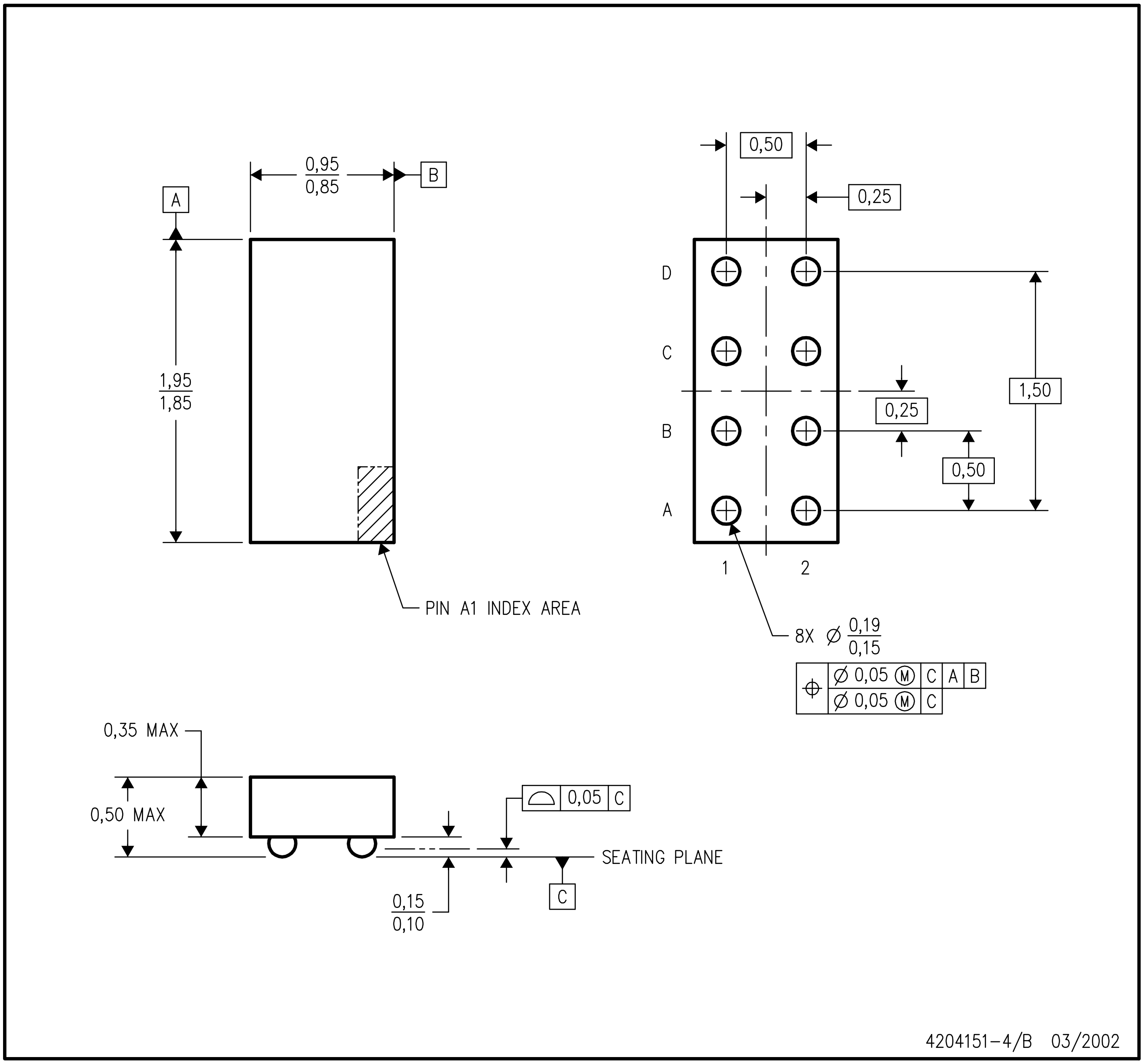
YEA (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. Package complies to JEDEC MO–211 variation EB.
- E. This package is tin–lead (SnPb). Refer to the 8 YZA package (drawing 4204151) for lead–free.

NanoStar is a trademark of Texas Instruments.

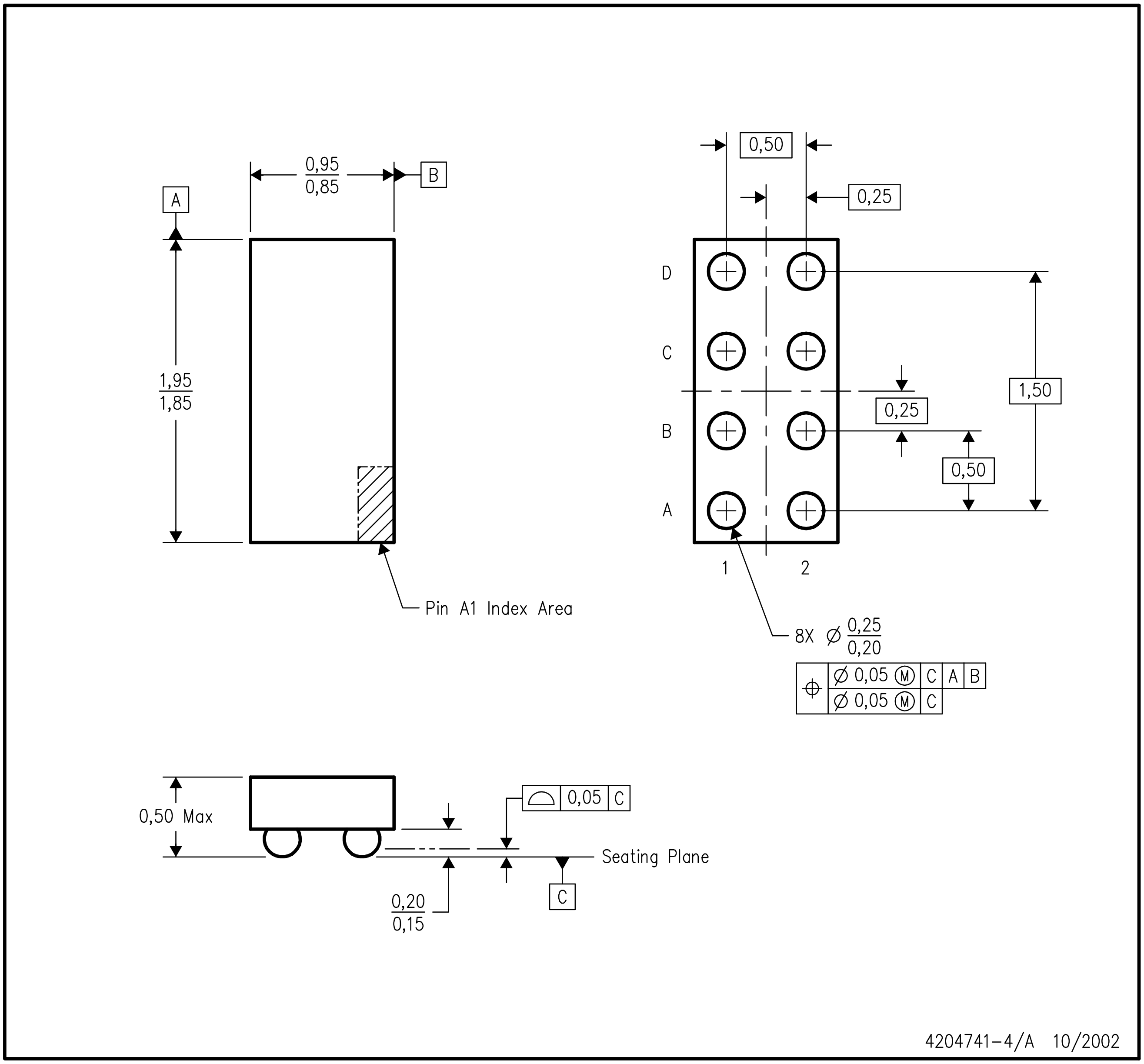
YZA (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. Package complies to JEDEC MO–211 variation EB.
- E. This package is lead–free. Refer to the 8 YEA package (drawing 4203167) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

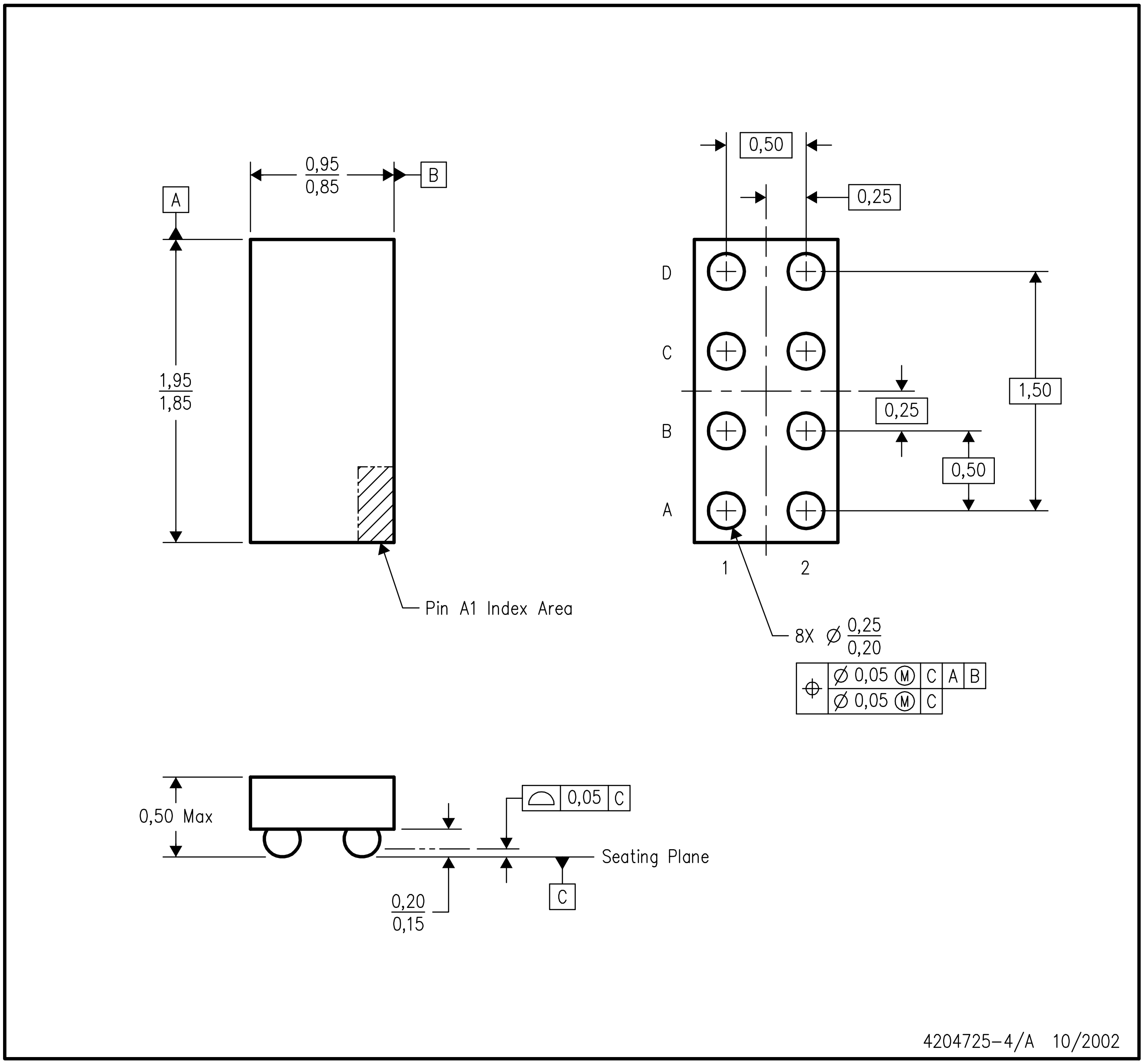
YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 8 YEP package (drawing 4204725) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead–free.

NanoStar is a trademark of Texas Instruments.