THC4231

Wide Bandwidth Fast Settling Operational Amplifier
165MHz Closed Loop Bandwidth

The THC4231 is a wide bandwidth fast settling operational amplifier designed specifically for high-speed, low-gain applications. The op amp design is based on current feedback architecture, a topology that eliminates the gain-bandwidth trade-off of voltage feedback designs while permitting outstanding high-speed performance.

The THC4231 op amp is the ideal design alternative to low-precision open-loop buffers and conventional oscillation prone op amps. The THC4231 offers precise gains from ±1.000 to ±5.000 and linearity that is a true .1% – even in demanding 50 Ohm applications. Traditional open-loop buffers typically have a gain of .95 and linearity of only 3%. And open loop buffer settling time is usually specified with an unrealistically large load resistance or neglecting thermal tail effects. The THC4231 current feedback op amp settles to .05% in 15ns with a 100 Ohm load.

Offsets and drifts were not ignored in the THC4231; the input offset voltage is 1mV and input offset voltage drift is only 10μV/°C. The THC4231 is stable and oscillation-free across the entire gain range and since it's internally compensated, the user is saved the trouble of designing external compensation networks and having to tweak them in production. The absence of a gain-bandwidth trade-off in the THC4231 allows performance to be easily predicted.

The THC4231 is constructed using thin-film resistor/bipolar technology. The THC4231X1B is specified over an ambient range of –25°C to 85°C, while the THC4231X1V operates with guaranteed performance over the –55°C to 125°C case operating range, is manufactured in facilities certified to MIL-STD-1772 and is screened to MIL-STD-883 for military applications. Both are packaged in a 12-lead metal can (TO-8/MO-12 style).

Typical Performance

Parameter	Gain Settings 1	2	5	–1	–2	–5	Units
–3dB Bandwidth	180	165	130	165	150	115	MHz
Rise Time (2V)	1.8	2.0	2.5	2.0	2.2	2.9	ns
Slew Rate	2500	3000	3000	3000	3000	3000	V/μs
Settling Time (to .1%)	12	12	12	12	12	15	ns

Features

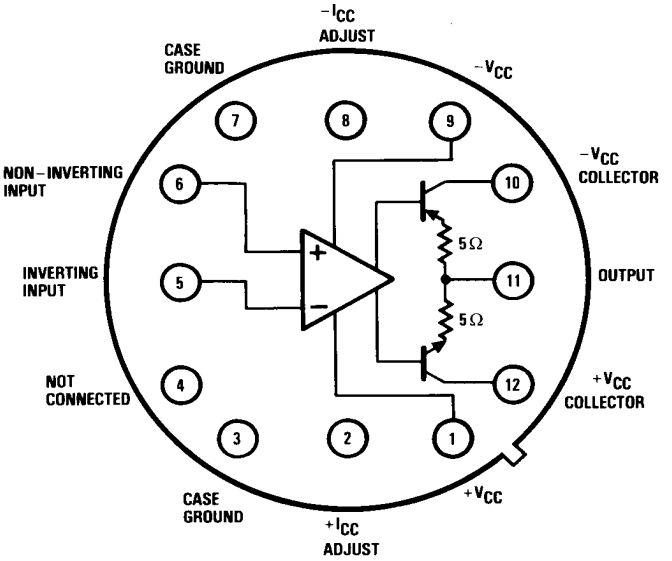
- Current Feedback Architecture
- 165MHz Closed-Loop –3dB Bandwidth
- 15ns Settling To 0.05%
- 1mV Input Offset Voltage, 10μV/°C Drift
- 100mA Output Current
- Excellent AC And DC Linearity
- Available Tested To MIL-STD-883

Applications

- Buffer For Flash A/D Converter
- DAC Current-To-Voltage Conversion
- Precision Line Driving
- Low-Power, Low-Gain, High-Speed Applications

Pin Assignments and Functional Block Diagram

(Bottom View)



12 Lead Metal Can – X1 Package
(TO-8/MO-12 Style)

TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
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Printed in the U.S.A.

Functional Description

General Information

The THC4231 op amp is based on current feedback instead of the traditional voltage feedback topology. The use of the THC4231 is basically the same as that of the conventional op amp, including active filters and differential amplifiers. (Refer to "Current Feedback vs. Voltage Feedback: A Comparison" for theory of operation.) However, to prevent oscillations, active circuit elements should not be used inside the feedback loop.

The THC4231 is designed specifically for low gain applications. The best performance is obtained when the circuit is used at gains between ±1 and ±5. Unlike conventional voltage feedback op amps, the current feedback THC4231 bandwidth is relatively unaffected by the gain setting. Optimum overall performance is achieved and all specifications are guaranteed with a 250 Ohm feedback resistor.

Supply Voltage

The THC4231 is designed to operate from ±15V supplies although it can operate with supplies reduced as low as ±5V. See Current Adjust for operation with reduced supply voltages. Low and high frequency decoupling capacitors (3.9μF and 0.1μF) should be connected in parallel from the $\pm V_{CC}$ Supply pins to the analog ground plane. The 0.1μF capacitors should be less than 0.15" from pins 1 and 9 while the 3.9μF capacitors are within 1" of these pins.

Collector Supply

The $\pm V_{CC}$ Collector pins are connected to the $\pm V_{CC}$ supplies via 33 Ohm resistors. High frequency decoupling capacitors of .01μF should be connected from $\pm V_{CC}$ Collector supply pins to the analog ground. This resistor and capacitor combination provide optimum settling performance with minimum distortion.

Current Adjust

To regain the full bandwidth lost when operating with supplies below ±10V, it is necessary to increase the V_{CC} supply currents by shorting the $\pm I_{CC}$ Adjust (pins 2 and 8) to the respective $\pm V_{CC}$ Supply Voltage (pins 1 and 9). The plot of bandwidth vs. V_{CC} shows the effect of shorting I_{CC} Adjust pins to V_{CC} Supply pins. Care should be taken to not exceed the maximum junction temperature. For this reason, this technique must not be used with supplies exceeding ±10V. For intermediate values of V_{CC}, external resistors between pins 1 and 2 and pins 8 and 9 can be used. When operating with ±15V supplies, pins 2 and 8 must remain open-circuit.

Case Ground

Case ground pins should be connected to the system analog ground.

Inverting and Non-Inverting Input

To prevent output peaking, the ground plane should be removed from the pc board in the vicinity of the inverting and non-inverting input pins.

Output

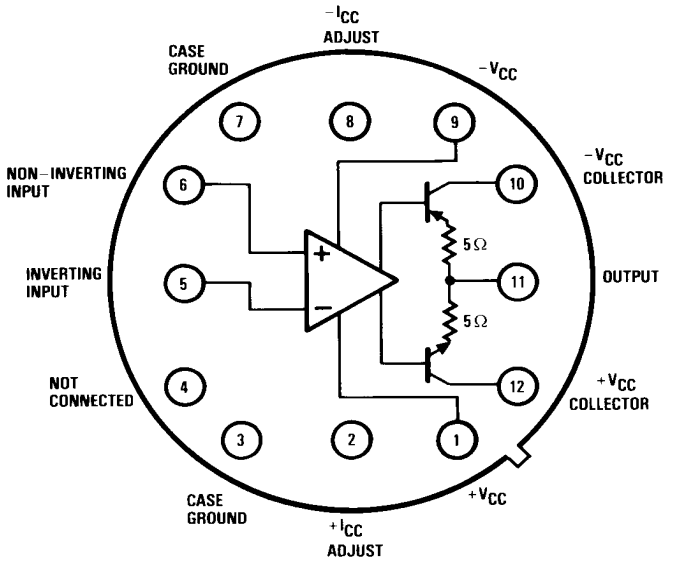
The analog output is capable of swinging V_{CC} - 3V to $-V_{CC}$ + 3V at up to 100mA output current. To prevent output peaking, the ground plane should be removed from the vicinity of the output pin.

No Connect

The No Connect pin is not connected internally to any portion of the circuit.

Pin Assignments and Functional Block Diagram

(Bottom View)



12 Lead Metal Can - X1 Package
(TO-8/MO-12 Style)

Package Interconnections

Signal Type	Signal Name	Function	Value	12-Lead Metal Can
Power	$+V_{CC}$	Positive Supply Voltage	+15V	1
	$+V_{CC}$ Collector	Positive Collector Voltage	+15V	12
	$-V_{CC}$	Negative Supply Voltage	-15V	9
	$-V_{CC}$ Collector	Negative Collector Voltage	-15V	10
	GND	Case Ground	0.0V	3, 7
Current Adjust	$+I_{CC}$ Adjust	Positive Low-Voltage Adjust	See Text	2
	$-I_{CC}$ Adjust	Negative Low-Voltage Adjust	See Text	8
Input	IN+	Non-Inverting	±12V	6
	IN-	Inverting	±12V	5
Output	V_{OUT}	Analog Output	±12V	11
No Connect	NC	None	-	4

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

$\pm V_{CC}$ ..... ±20V

Input

Inverting and Non-inverting input ..... See diagram

Voltage ..... See diagram

Output Current ..... ±100mA

Temperature

Operating, case ..... -65 to +150°C

junction ..... +175°C

Lead, soldering (10 seconds) ..... +300°C

Storage ..... -65 to +150°C

Reliability

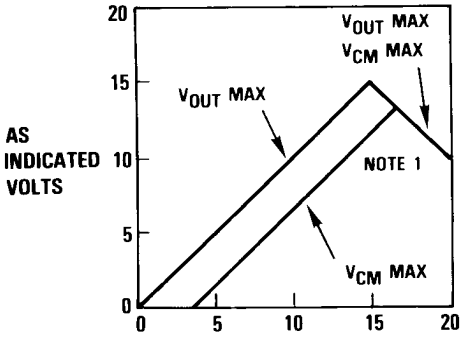
Mean Time Between Failures [2] ..... 2.9×10^6 hours

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. A-grade, Ground Fixed environment @ T_C = 70°C, per MIL-HDBK-217E.

Absolute Maximum Rating

Input and Common Mode Voltage Limits



Note 1: These ratings protect against damage to the input stage caused by saturation of either the input or output stages at lower supply voltages, and against exceeding transistor collector-emitter breakdown ratings at high supply voltages. V_{OUT}(max) is calculated by assuming no output saturation. Saturation is allowed to occur up to this calculated level of $V_{OUT}-V_{CM}$ is defined as the voltage at the non-inverting input, pin 6.

Operating conditions

Parameter		Temperature Range						Units
		Industrial			Extended			
		Min	Nom	Max	Min	Nom	Max	
$\pm V_{CC}$	Supply Voltage	±5	±15		±5	±15		V
GND	Case Ground		0.0			0.0		V
IN+, IN−	Inputs		$\lvert\pm V_{CC}\rvert-3$			$\lvert\pm V_{CC}\rvert-3$		V
V_{OUT}	Output		$\pm V_{CC}$			$\pm V_{CC}$		V
T_A	Ambient Temperature	−25		85				°C
T_C	Case Temperature				−55		125	°C

DC Electrical characteristics within specified operating conditions

(R_L = 100 Ohms, R_f = 250 Ohms, V_{CC} = ±15V, A_V = +2)

Parameter		Test Conditions	Temperature Range						Units
			Industrial			Extended			
			Min	Typ	Max	Min	Typ	Max	
I_{CC}	Supply Current	V_{CC} = ±15V, No Load		18	22		18	22	mA
R_{IN}	Non−Inverting Input Resistance		100	400		100	400		kOhms
C_{IN}	Non−Inverting Input Capacitance			1.3	2.5		1.3	2.5	pF
V_{IO}	Input Offset Voltage			1	4.5		1	4.5	mV
T_{CIO}	Temp Coefficient, Input Offset Voltage			10	25		10	25	µV/°C
I_{IB}	Input Bias Current	Non−Inverting		5	31		5	31	µA
		Inverting		10	35		10	35	µA
T_{CIB}	Temp Coefficient, Input Bias Current	Non−Inverting		50	125		50	125	nA/°C
		Inverting		125	200		125	200	nA/°C
V_{OUT}	Output Voltage Range	No Load	±11	±12		±11	±12		V

AC Electrical characteristics within specified operating conditions

(R_L = 100 Ohms, R_f = 250 Ohms, V_{CC} = ±15V, A_V = +2)

Parameter		Test Conditions	Temperature Range						Units
			Industrial			Extended			
			Min	Typ	Max	Min	Typ	Max	
SSBW	Small Signal Bandwidth	V_{OUT} = $2V_{pp}$ – 3dB	120	165		120	165		MHz
FPBW	Full Power Bandwidth	V_{OUT} = $10V_{pp}$ – 3dB	60	95		60	95		MHz
E_{GPL}	Gain Flatness Peaking, LOW Frequency	V_{OUT} = $2V_{pp}$, 0.1≤ f≤ 50MHz		0.1	0.6		0.1	0.6	dB
E_{GPH}	Gain Flatness Peaking, HIGH Frequency	V_{OUT} = $2V_{pp}$, f> 50MHz		0.1	1.5		0.1	1.5	dB
E_{GR}	Gain Flatness Rolloff	V_{OUT} = $2V_{pp}$, f = 100MHz		0.4	1.0		0.4	1.0	dB
T_{GD}	Group Delay	f≤ 100MHz		3.5 ± .5			3.5 ± .5		ns
E_P	Linear Phase Deviation	f≤ 100MHz		0.5	2.0		0.5	2.0	Degrees
RI_{NI}	Reverse Isolation, Non-Inverting	f≤ 100MHz	43	53		43	53		dB
RI_{IN}	Reverse Isolation, Inverting	f≤ 100MHz	26	36		26	36		dB
R_{OUT}	Output Resistance	f_{OUT} = 100MHz		5			5		Ohms
L_{OUT}	Output Inductance	f_{OUT} = 100MHz		37			37		nH
t_{RS}	Rise Time, Small Signal	2V Output Step		2	2.7		2	2.7	ns
t_{RL}	Rise Time, Large Signal	10V Output Step		5	7.0		5	7.0	ns
t_{FS}	Fall Time, Small Signal	2V Output Step		2	2.7		2	2.7	ns
t_{FL}	Fall Time, Large Signal	10V Output Step		5	7.0		5	7.0	ns
t_S	Settling Time	5V Output Step to .05%		15			15		ns
		2.5V Output Step to .1%		12	22		12	22	ns
E_{OS}	Overshoot	5V Output Step		5	15		5	15	%
SR	Slew Rate	Input Overdriven	1.8	3		1.8	3		V/ns
t_{OR}	Overload Recovery	< 50ns Pulse, 200% Overdrive, to < 1% Error		120			120		ns
HD2	Second Harmonic Distortion	0 dBm, 20MHz	–47	–55		–47	–55		dBc
HD3	Third Harmonic Distortion	0 dBm, 20MHz	–47	–59		–47	–59		dBc
	Equivalent Input Noise, Noise Floor	> 5MHz	–150	–153		–150	–153		dBm(1Hz)
	Equivalent Input Noise, Integrated	5MHz to 200MHz		70	100		70	100	μVrms
PSRR	Power Supply Rejection Ratio		45	50		45	50		dB
CMRR	Common Mode Rejection Ratio		40	46		40	46		dB

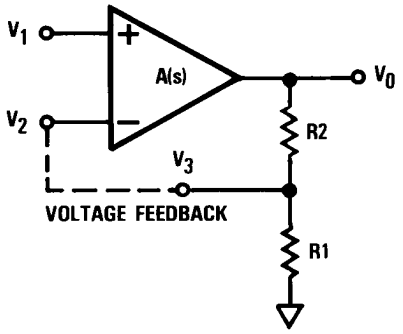
Current Feedback vs. Voltage Feedback: A Comparison

To fully understand the advantages of the THC4231 current feedback op amp, it is helpful to compare its theory of operation to that of the traditional voltage feedback op amp.

Voltage Feedback Op Amp

Traditional voltage feedback op amps have a differential, high input impedance stage followed by several gain stages. The open loop output of this op amp is:

$$V_O = A(s)[V_1 - V_2]$$



With the feedback connection made, a feedback voltage is applied to the inverting input and the closed loop gain is:

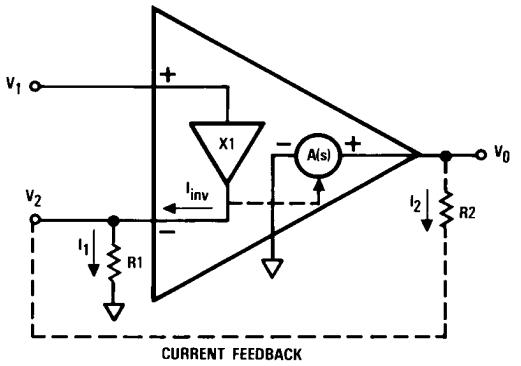
$$\frac{V_O}{V_1} = \frac{\frac{R_1 + R_2}{R_1}}{1 + \frac{\frac{R_1 + R_2}{R_1}}{A(s)}}$$

Substituting $G = (R_1 + R_2)/R_1$

$$\frac{V_O}{V_1} = \frac{G}{1 + \frac{G}{A(s)}}$$

Current Feedback Op Amp

The current feedback op amp has a unity gain voltage buffer amplifier across the inverting and non-inverting inputs. This buffer forces the voltage at V_2 to be identical to the voltage applied at V_1 independent of any external feedback. Because the inverting input is actually the output of the buffer, this node has a very low input impedance, which is further reduced when the feedback resistor (R2) is installed. With respect to V_1, the inverting input is truly a virtual ground and current easily flows into or out of this node.



The transimpedance amplifier is the gain stage inside the THC4231. It senses the current flowing into or out of the inverting input and transforms this current into an output voltage. The transfer function of the transimpedance amplifier is A(s) and the units are Ohms.

The open loop gain of the amplifier is:

$$V_O = I_{inv}\, A(s)$$

With the feedback resistor installed, the closed loop gain equation is:

$$\frac{V_O}{V_1} = \frac{\frac{R_1 + R_2}{R_1 R_2}}{\frac{1}{R_2} + \frac{1}{A(s)}} = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{R_2}{A(s)}}$$

Voltage Feedback Op Amp Continued

Substituting $A(s) = \frac{N(s)}{D(s)}$ yields:

$$\frac{V_O}{V_I} = G \frac{N(s)}{N(s) + (G)\,D(s)}$$

Current Feedback Op Amp Continued

Substituting $G = 1 + \frac{R_2}{R_1}$

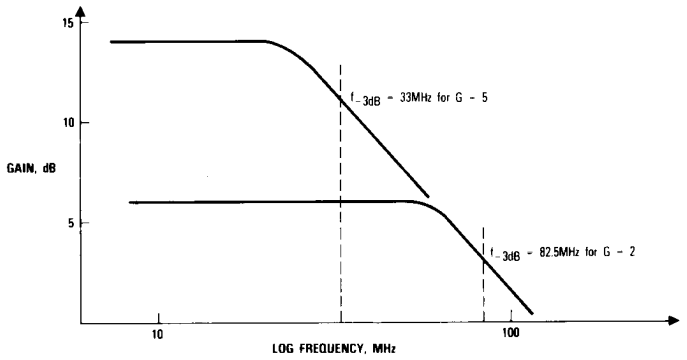
$$\frac{V_O}{V_I} = \frac{G}{1 + \frac{R_2}{A(s)}}$$

Substituting $A(s) = \frac{N(s)}{D(s)}$ yields:

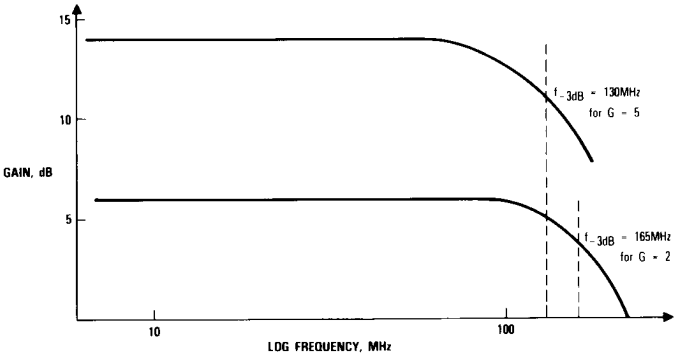
$$\frac{V_O}{V_I} = G \frac{N(s)}{N(s) + R_2 D(s)}$$

Now the two topologies can be compared. In the voltage feedback op amp transfer function, the circuit gain and pole locations are both dependent upon G = (R1 + R2)/R1. Therefore, changing the gain of the circuit causes the pole locations to move. In practice, for a high gain setting, the poles will be at a lower frequency than for a low gain setting. This is shown in the illustration below. Frequency response that depends upon the circuit gain is the biggest drawback of voltage feedback op amps.

By comparison, the current feedback op amp also has circuit gain dependent upon G = (R1 + R2)/R1, but this time the pole locations are dependent only on R_2. This is the advantage of the current feedback topology over voltage feedback topology: frequency response is independent of the circuit gain. In practice, it is easy to keep R2 constant for various gain settings and therefore maintain the frequency response of the op amp. In fact, the design of the THC4231 has been optimized for R2 = 250 Ohms and all specifications are guaranteed with this value of feedback resistor.



Voltage Feedback Op Amp

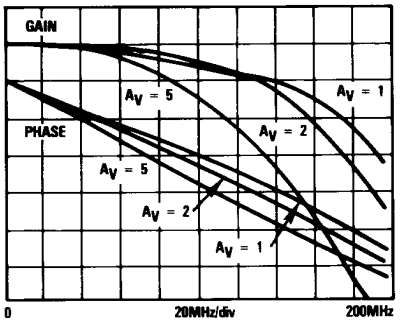


Current Feedback Op Amp

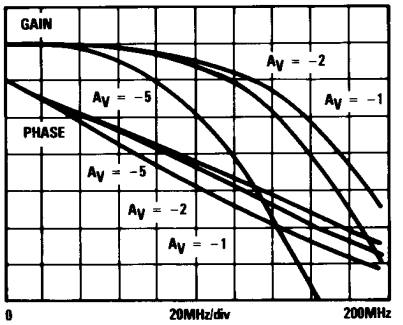
Typical Performance Curves

(T_A = 25°C, A_V = +2, V_{CC} = ±15V, R_L = 100 Ohms, R_f = 250 Ohms)

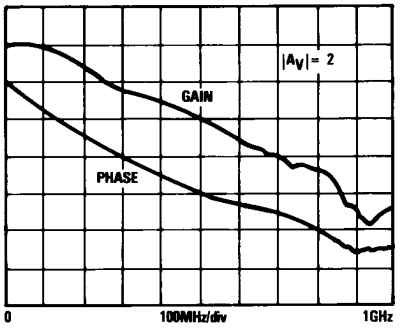
Non-Inverting Gain and Phase



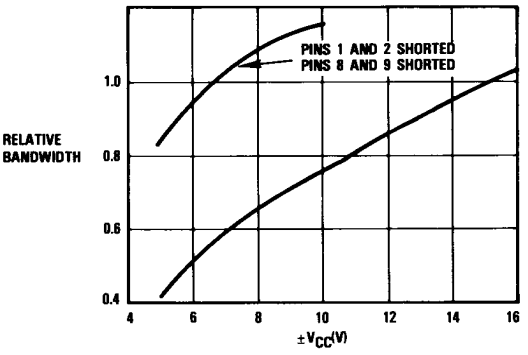
Inverting Gain and Phase



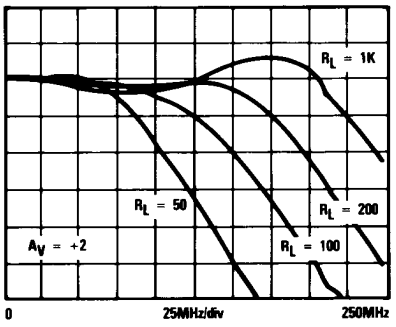
Broadband Gain and Phase



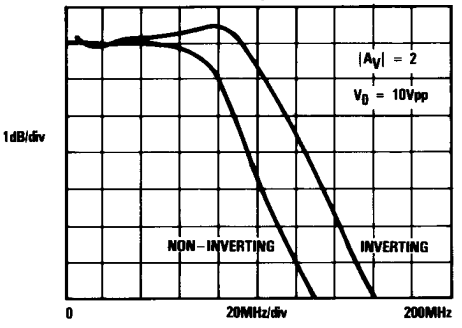
Bandwidth vs. V_{CC}



Gain vs. Frequency for Various R_Ls

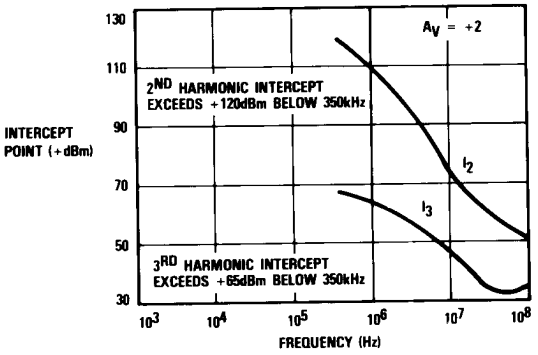


Full Power Gain vs. Frequency

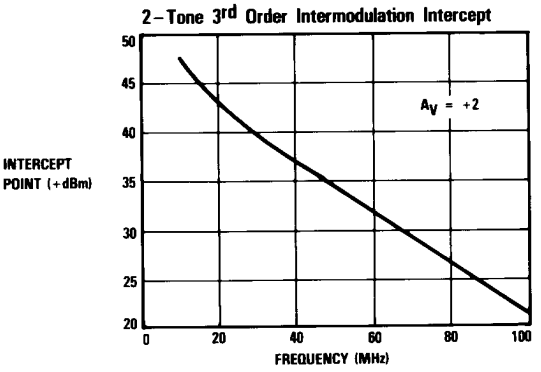


Typical Performance Curves Continued

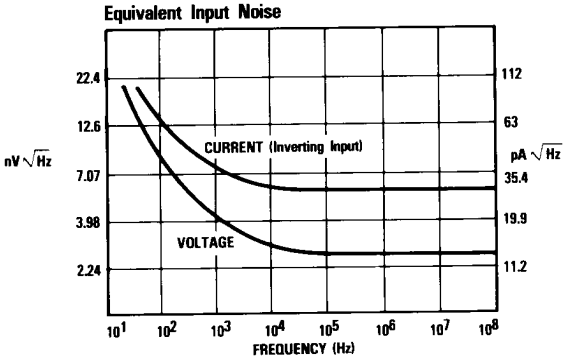
2nd and 3rd Harmonic Distortion Intercept



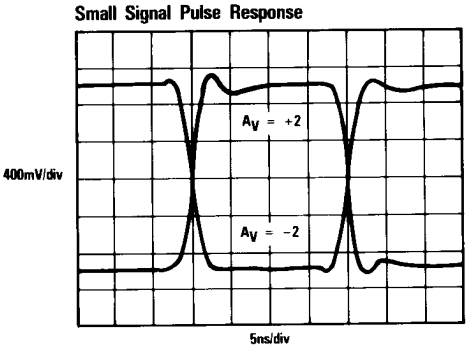
2-Tone 3rd Order Intermodulation Intercept



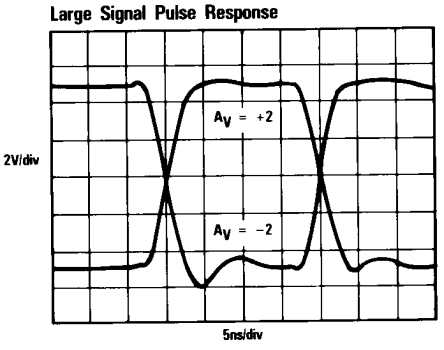
Equivalent Input Noise



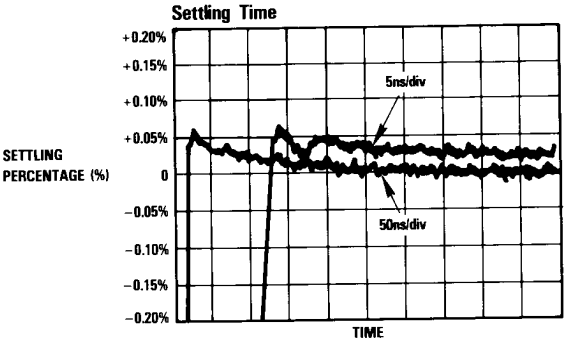
Small Signal Pulse Response



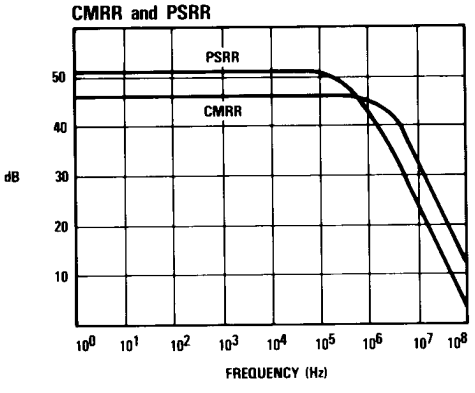
Large Signal Pulse Response



Settling Time



CMRR and PSRR



Layout Considerations

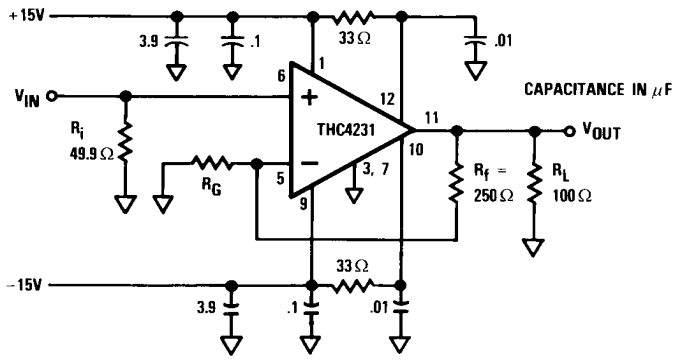
To assure optimum performance from the THC4231, the surrounding circuitry should follow good high-frequency layout practices which minimize unwanted coupling of signals between nodes. When breadboarding, point-to-point wiring should be used, keeping lead lengths less than 0.25". Solid ground plane is recommended. Sockets with small, short pin receptacles or individual high-frequency pins may be used with only slight performance degradation. For optimum performance, the THC4231 leads should be soldered, not socketed.

For printed circuit board layout, all traces should be kept as short and direct as possible. The body of the gain-setting resistor (R_G) should be kept as close to the inverting input (pin 5) as possible to reduce capacitance at that point. Ground plane should be removed from the pc board in the vicinity of the inverting, non-inverting and output pins. To prevent signal distortion caused by reflections from impedance mismatches, terminated microstrip or coaxial cable should be used whenever the signal must traverse more than one inch.

A ground return path for current from the load resistor to the power supply bypass capacitors must be provided. High frequency (surface mount if possible) ceramic capacitors of 0.01 to 0.1μF (with short leads) should be less than .15" from pins 1 and 9. Larger 3.9μF tantalum capacitors should be placed within 1" of these pins. $\pm V_{CC}$ Collector Supply connections (pins 10 and 12) can be made directly from pins 9 and 1, but better supply rejection and settling time performance are obtained if they are seperately bypassed with 0.01μF capacitors and 33 Ohm resistors as shown in the Typical Application Circuits.

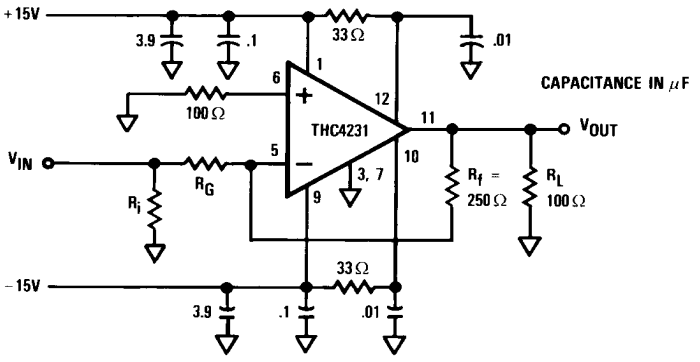
Since the pc board forms such an integral portion of the circuit, it is recommended that a prototype board containing just the THC4231 circuitry is built and evaluated before commiting to a final pc board layout.

Typical Application Circuits



$$A_V = 1 + \frac{R_F}{R_G}$$

Figure 1. Non-Inverting Gain Circuit



$$A_V = -\frac{R_F}{R_G}$$

Figure 2. Inverting Gain Circuit

Distortion And Noise

The graphs of intercept point, I_2 and I_3, versus frequency make it easy to predict the distortion at any frequency given the output voltage of the THC4231. First, convert the output voltage (V_O) to $V_{RMS} = (V_{PP}/2\sqrt{2})$ and then to $P = [(10\log_{10}(20V_{RMS}^2)]$ to get the power output in dBm. At the frequency of interest, its 2nd harmonic will be $S_2 = (I_2 - P)$dB below the level of P. Its third harmonic will be $S_3 = 2(I_3 - P)$dB below P, as will the two-tone third order intermodulation products. These approximations are useful for $P < -1$dB compression levels.

Approximate noise figure can be determined for the THC4231 using the equivalent input noise graph. The following equation can be used to determine noise figure (F) in dB.

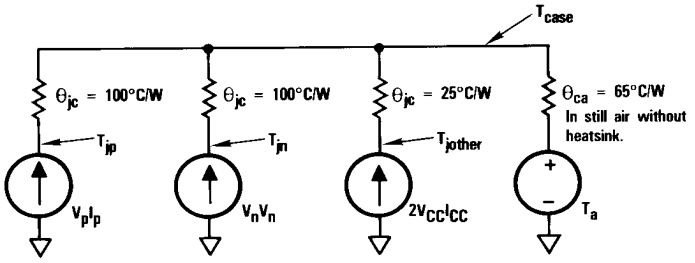
$$F = 10\log\left[1 + \frac{\frac{i_n^2 R_F^2}{A_V^2} + V_n^2}{4kTR_S\,\Delta f}\right]$$

Where V_n is the rms noise voltage and I_n is the rms noise current. Beyond the breakpoint of the curves (i.e., where they are flat), the broadband noise figure equals the spot noise figure, so Δf should equal one (1) and V_n and I_n should be read directly from the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. The thermal model below can be used to predict junction temperatures. Many styles of heat sinks are available for TO-8 packages such as Wakefield 215 and Thermalloy 2240. Radial fin heat sinks cover the circuit board and may interfere with external components unless surface mounted resistors and capacitors are used. A 0.1" spacer can be installed under the TO-8 package so that conventional components can be used with sufficient clearance.

Thermal Model



$P_{circuit} = I_{CC}[(+V_{CC}) - (-V_{CC})]$ where I_{CC} = 16mA at ±15V

$P_{xxx} = [(\pm V_{CC}) - V_{OUT} - (I_{col})(R_{col} + 4)](I_{col})$(% duty cycle)

For positive V_O and V_{CC}, this is the power in the npn output stage.

For negative V_O and V_{CC}, this is the power in the pnp output stage.

$I_{col} = V_{OUT} / R_{load}$ or 4mA whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33 Ohms recommended) between the xxx collector and $\pm V_{CC}$.

$T_{j(pnp)} = P_{pnp}(100 + \theta_{ca}) + (P_{cir} + P_{npn})\theta_{ca} + T_a$.
Similar for $T_{j(npn)}$.

$T_{j(cir)} = P_{cir}(48 + \theta_{ca}) + (P_{pnp} + P_{npn})\theta_{ca} + T_a$.

Ordering Information [1]

Product Number	Temperature Range	Screening	Package	Package Marking
THC4231X1B	IND = −20°C to 85°C	Industrial	12-Lead Metal Can (TO-8/MO-12)	4231X1B
THC4231X1A	EXT = −55°C to 125°C	MIL-STD-883	12-Lead Metal Can (TO-8/MO-12)	4231X1A

Notes:
1. Contact factory for availability.

X1 Package

12 Lead Metal Can (TO-8/MO-12 Style)

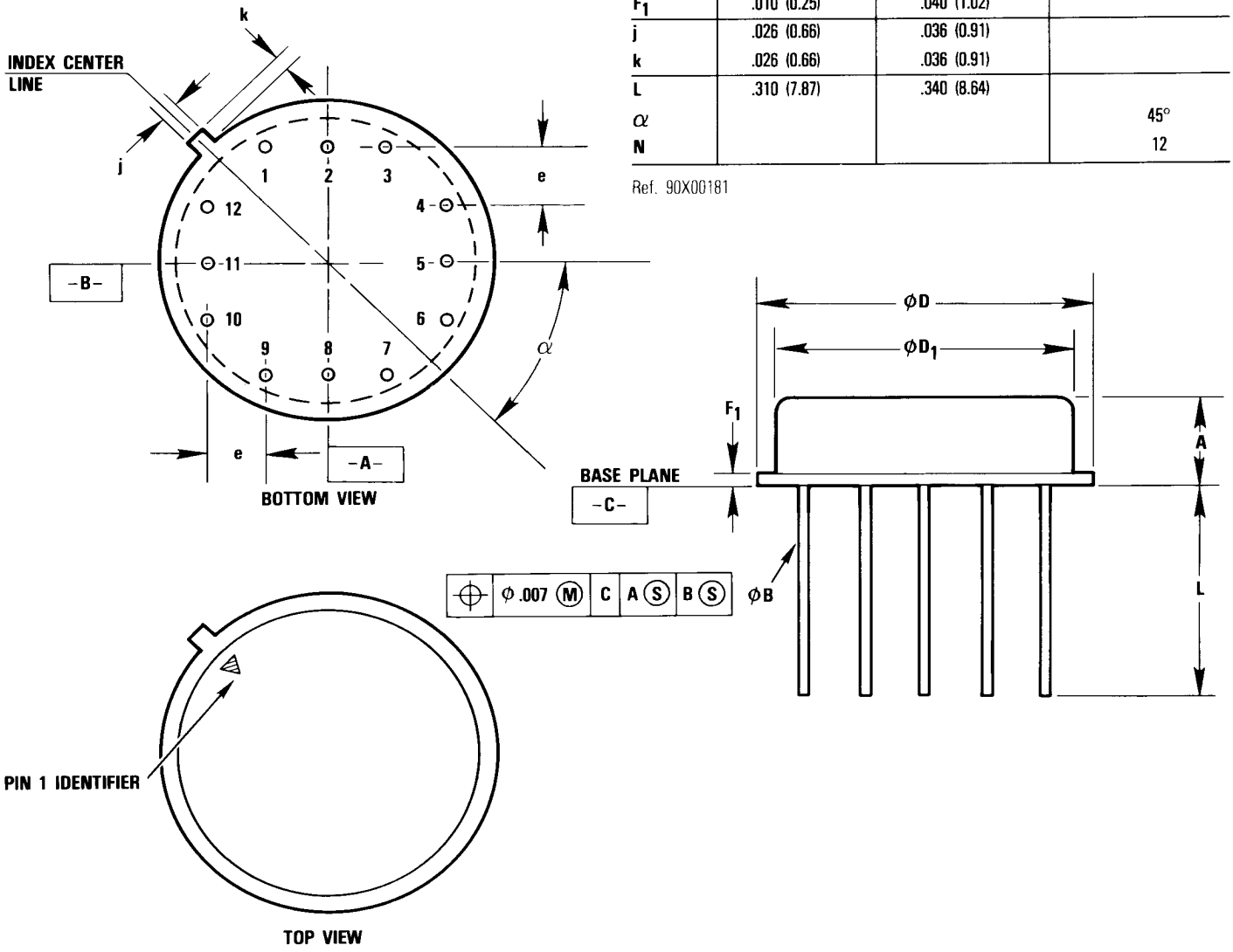
Notes:

1. Controlling dimension: inch.
2. Dimension N: maximum quantity of lead positions.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.145 (3.68)	.170 (4.32)	
ϕB	.016 (0.41)	.019 (0.48)	
ϕD	.598 (15.19)	.602 (15.29)	
$ϕD_1$	.545 (13.84)	.550 (13.97)	
e			.100 (2.54) Basic
F_1	.010 (0.25)	.040 (1.02)	
j	.026 (0.66)	.036 (0.91)	
k	.026 (0.66)	.036 (0.91)	
L	.310 (7.87)	.340 (8.64)	
α			45°
N			12

Ref. 90X00181



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