



LOW-VOLTAGE 10-BIT BUS SWITCH

IDT74CBTLV3384

FEATURES:

- 5Ω A/B bi-directional bus switch
- Isolation under power-off conditions
- Over-voltage tolerant
- Latch-up performance exceeds 100mA
- $V_{CC} = 2.3V - 3.6V$, Normal Range
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- Available in QSOP and TSSOP packages

APPLICATIONS:

- 3.3V High Speed Bus Switching and Bus Isolation

DESCRIPTION:

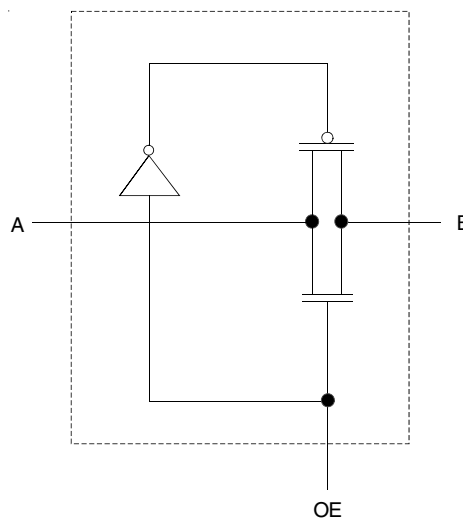
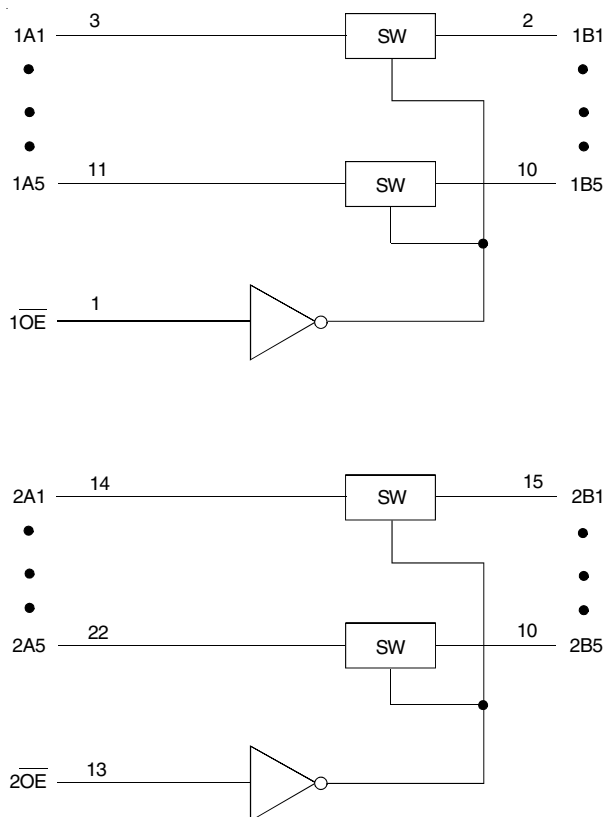
The CBTLV3384 is a ten bit high-speed bus switch with low on-state resistance of the switch allowing connections to be made with minimal propagation delay.

The device is organized as dual 5-bit bus switches with separate output-enable ($\overline{OE}$) inputs, to allow use as two 5-bit bus switches or one 10-bit bus switch. When $\overline{OE}$ is low, the associated 5-bit bus switch is on and A port is connected to B port. When $\overline{OE}$ is high, the switch is open, and a high-impedance state exists between the two ports.

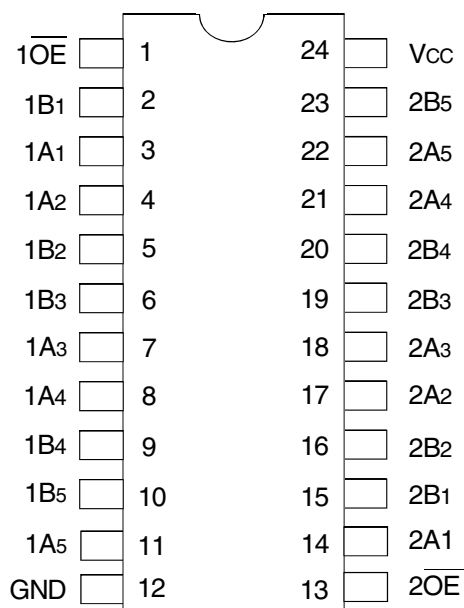
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTIONAL BLOCK DIAGRAM

SIMPLIFIED SCHEMATIC, EACH SWITCH



PIN CONFIGURATION



QSOP/TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{CC}	Supply Voltage Range	−0.5 to +4.6	V
V _I	Input Voltage Range	−0.5 to +4.6	V
	Continuous Channel Current	128	mA
I _{IK}	Input Clamp Current, V _{IO} < 0	−50	mA
T _{STG}	Storage Temperature	−65 to +150	°C

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FUNCTION TABLE⁽¹⁾

Input		Inputs/Outputs	
1OE	2OE	1B1 - 1B5	2B1 - 2B5
L	L	1A1 - 1A5	2A1 - 2A5
L	H	1A1 - 1A5	Z
H	L	Z	2A1 - 2A5
H	H	Z	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance

OPERATING CHARACTERISTICS, T_A = 25°C⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{CC}	Supply Voltage		2.3	3.6	V
V _{IH}	High-Level Control Input Voltage	V _{CC} = 2.3V to 2.7V	1.7	—	V
		V _{CC} = 2.7V to 3.6V	2	—	
V _{IL}	Low-Level Control Input Voltage	V _{CC} = 2.3V to 2.7V	—	0.7	V
		V _{CC} = 2.7V to 3.6V	—	0.8	
T _A	Operating Free-Air Temperature		−40	85	°C

NOTE:

- All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{IK}	Control Inputs, Data I/O	$V_{CC} = 3\text{V}$, $I_I = -18\text{mA}$		—	—	-1.2	V
I_I	Control Inputs, Data I/O	$V_{CC} = 3.6\text{V}$, $V_I = V_{CC}$ or GND		—	—	± 1	μA
I_{OZ}	Data I/O	$V_{CC} = 3.6\text{V}$, $V_O = 0$ or 3.6V , switch disabled		—	—	5	μA
I_{OFF}		$V_{CC} = 0$, V_I or $V_O = 0$ to 3.6V		—	—	50	μA
I_{CC}		$V_{CC} = 3.6\text{V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		—	—	10	μA
$\Delta I_{CC}^{(1)}$	Control Inputs	$V_{CC} = 3.6\text{V}$, one input at 3V , other inputs at V_{CC} or GND		—	—	300	μA
C_I	Control Inputs	$V_I = 3\text{V}$ or 0		—	4	—	pF
$C_{IO(OFF)}$		$V_O = 3\text{V}$ or 0 , $\overline{OE} = V_{CC}$		—	7	—	pF
$R_{ON}^{(2)}$	Max. at $V_{CC} = 2.3\text{V}$ Typ. at $V_{CC} = 2.5\text{V}$	$V_I = 0$	$I_O = 64\text{mA}$	—	5	8	Ω
			$I_O = 24\text{mA}$	—	5	8	
	$V_{CC} = 3\text{V}$	$V_I = 1.7\text{V}$	$I_O = 15\text{mA}$	—	27	40	
			$I_O = 64\text{mA}$	—	5	7	
		$V_I = 2.4\text{V}$	$I_O = 24\text{mA}$	—	5	7	
			$I_O = 15\text{mA}$	—	10	15	

NOTES:

- The increase in supply current is attributable to each current that is at the specified voltage level rather than V_{CC} or GND.
- This is measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

SWITCHING CHARACTERISTICS

Symbol	Parameter	$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		Unit
		Min.	Max.	Min.	Max.	
$t_{PD}^{(1)}$	Propagation Delay A to B or B to A	—	0.15	—	0.25	ns
t_{EN}	Output Enable Time $\overline{OE}$ to A or B	1	5	1	4.3	ns
t_{DIS}	Output Disable Time $\overline{OE}$ to A or B	1	5.5	1	5.5	ns

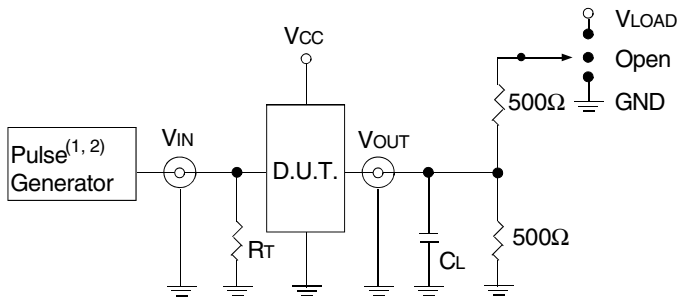
NOTE:

- The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance driven by an ideal voltage source (zero output impedance).

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	$2 \times V_{CC}$	V
V_{IH}	3	V_{CC}	V
V_T	1.5	$V_{CC} / 2$	V
V_{LZ}	300	150	mV
V_{HZ}	300	150	mV
CL	50	30	pF



Test Circuits for All Outputs

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

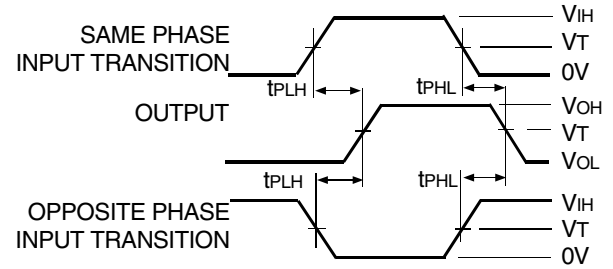
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

NOTES:

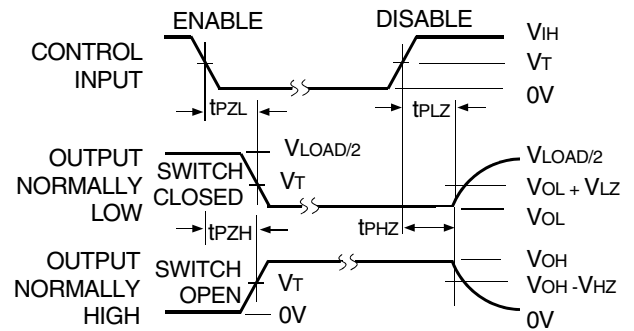
1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_r \leq 2\text{ns}$; $t_f \leq 2.5\text{ns}$.

SWITCH POSITION

Test	Switch
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND
t_{PD}	Open



Propagation Delay



Enable and Disable Times

ORDERING INFORMATION

XX Temp. Range	CBTLV Device Type	XXX Package	
		Q	Quarter-size Small Outline Package
		QG	QSOP - Green
		PG	Thin Shrink Small Outline Package
		PGG	TSSOP - Green
		3384	Low-Voltage 10-Bit Bus Switch
		74	−40°C to +85°C



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