

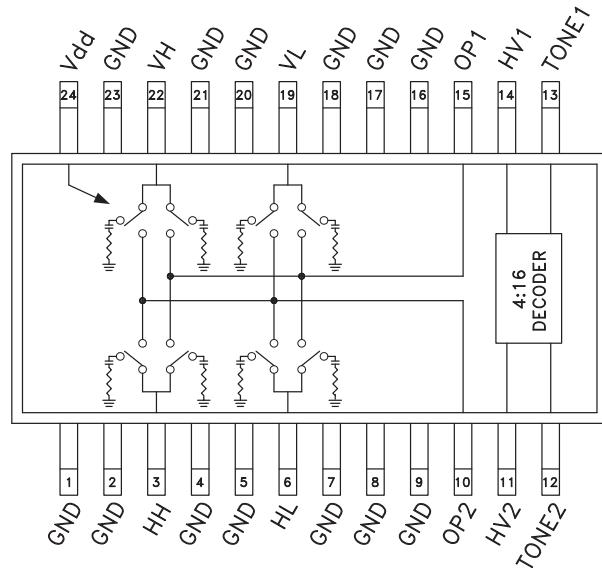


## Typical Applications

4x2 Switch Matrix for 0.7 - 3.0 GHz Applications:

- Cable Modem
- CATV
- Cellular Systems
- DBS

## Functional Diagram



## Electrical Specifications, $T_A = +25^\circ C$ , $Vdd = +5V$ , 50 Ohm System

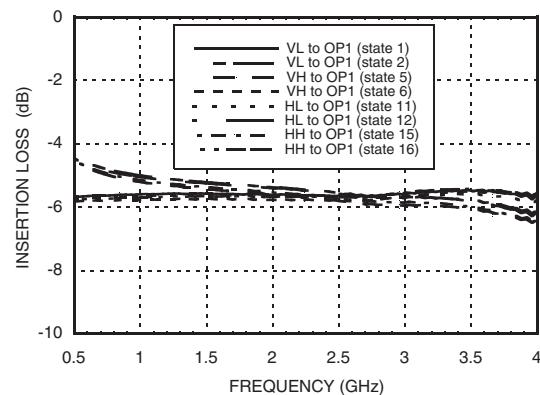
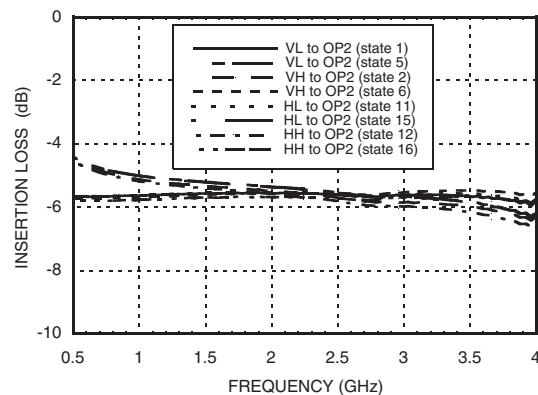
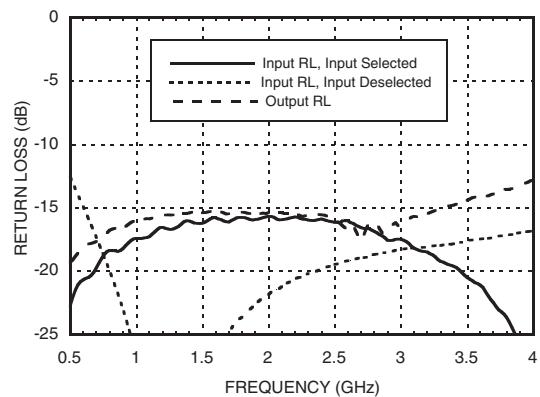
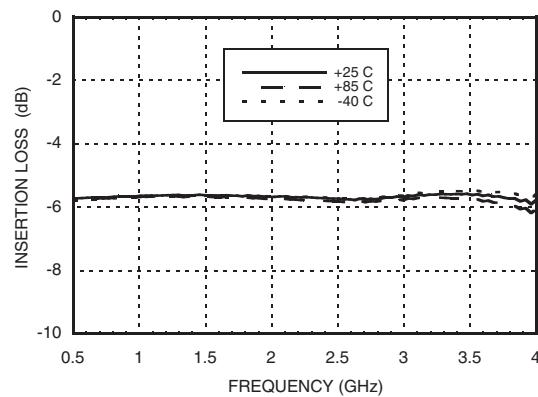
Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	700 - 3000 MHz		6.0	7.0	dB
Isolation	700 - 950 MHz 950 - 1450 MHz 1450 - 2150 MHz 2150 - 3000 MHz	36 See OP1/2 Isolation Tables	40		dB
Return Loss (Input; VL, HL, VH, HH)	700 - 3000 MHz	12	16		dB
Return Loss (Output; OP1, OP2)	700 - 3000 MHz	11	15		dB
Output IP3	700 - 3000 MHz	31	37		dBm
Input Power for 1 dB Compression	700 - 3000 MHz	22	26		dBm
Switching Speed	tRISE / tFALL (10/90% RF) tON / tOFF (50% CTL to 10/90% RF)	700 - 3000 MHz	140 350		ns ns

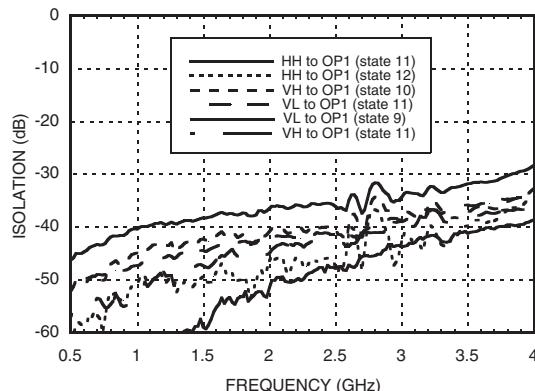
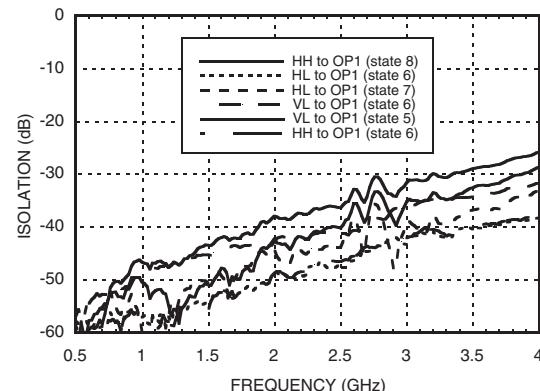
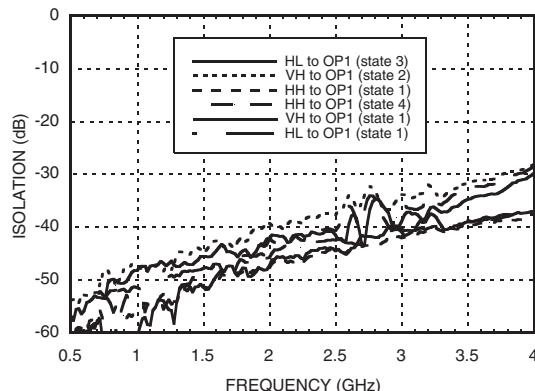
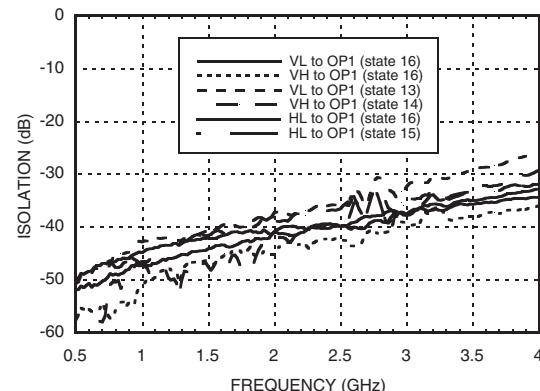
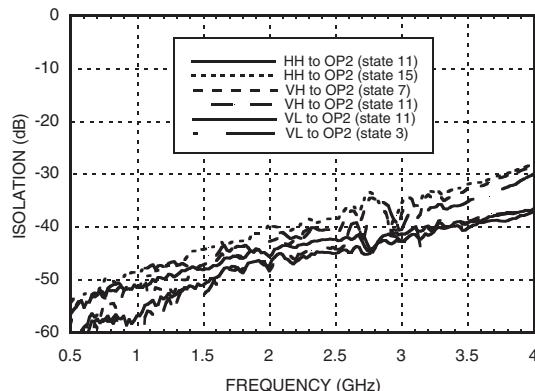
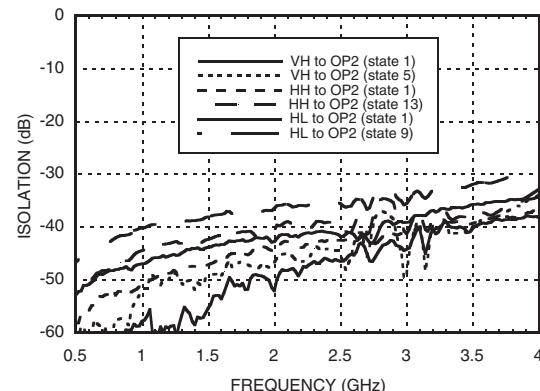

**OP1 Isolation 950 - 1450 MHz**

Input to Output State	Interfering Signal	State	Min. (dB)	Typ. (dB)
HL to OP1	VL to OP1	9	36	38
	All Other States	All Other States	40	>43
VL to OP1	All Other States	All States	40	>43
VH to OP1	All Other States	All States	40	>43
HH to OP1	VL to OP1	13	39	41
	VL to OP1	16	40	42
	HL to OP1	15	39	41
	All Other States	All Other States	40	>43

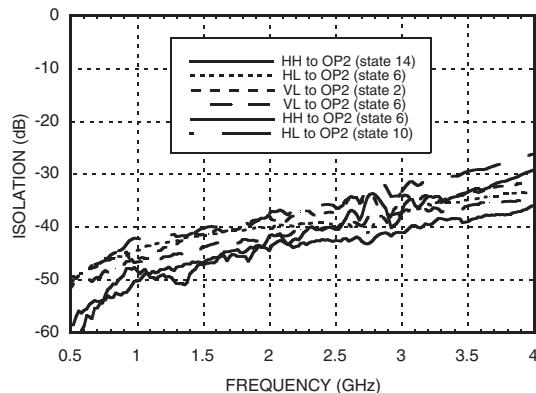
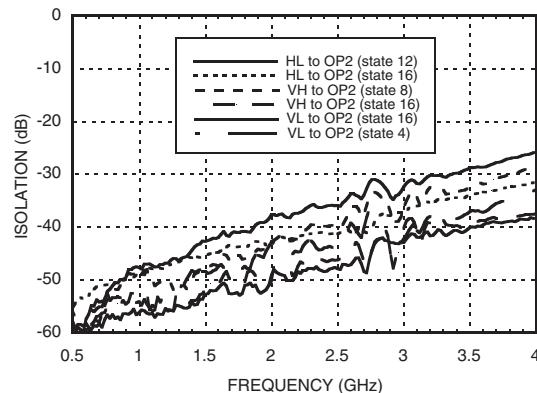
**OP2 Isolation 950 - 1450 MHz**

Input to Output State	Interfering Signal	State	Min. (dB)	Typ. (dB)
HL to OP2	All States	All States	40	>43
VH to OP2	HL to OP2	10	38	40
	HL to OP2	6	39	41
	VL to OP2	2	39	41
	All Other States	All Other States	40	>43
VL to OP2	HL to OP2	9	36	38
	All Other States	All Other States	40	>43
HH to OP2	All States	All States	40	>43

**Insertion Loss on OP1**

**Insertion Loss on OP2**

**Return Loss**

**Typical Insertion Loss vs. Temperature**



**Isolation When HL is Connected to OP1\***

**Isolation When VH is Connected to OP1\***

**Isolation When VL is Connected to OP1\***

**Isolation When HH is Connected to OP1\***

**Isolation When HL is Connected to OP2\***

**Isolation When VL is Connected to OP2\***


\* Isolation is recorded above insertion loss & measured at output of switch.


**GaAs MMIC 4x2 SWITCH  
MATRIX, 0.7 - 3.0 GHz**
**Isolation When VH is Connected to OP2\***

**Isolation When HH is Connected to OP2\***

**Output Third Order Intercept Point**

Path	State	F1 Pout (dBm)	Pout Intermod (dBm)	IMR (dBc)	Output IP3 (dBm)
VL to OP1	1	-12	-106	94	35
VL to OP2	1	-12	-114	102	39
HL to OP1	11	-12	-108	96	36
HL to OP2	11	-12	-110	98	37
VH to OP1	6	-12	-115	103	39.5
VH to OP2	6	-12	-115	103	39.5
HH to OP1	16	-12	-116	104	40
HH to OP2	16	-12	-114	102	39
Test Conditions					
Temperature = +25° C					
F1 = 2150 (MHz): -12 dBm at the Output					
F2 = 2151 (MHz): -12 dBm at the Output					
Vdd = +5V VCTL Low = 0V, High = +5V					

\* Isolation is recorded above insertion loss & measured at output of switch.



### Truth Table

State	Control Input				Output to Input State		RF Path State							
	HV 1	Tone 1	HV 2	Tone 2	OP1	OP2	VL to OP1	HL to OP1	VH to OP1	HH to OP1	VL to OP2	HL to OP2	VH to OP2	HH to OP2
1	0	0	0	0	VL	VL	LOSS	ISOL	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL
2	0	0	0	1	VL	VH	LOSS	ISOL	ISOL	ISOL	ISOL	ISOL	LOSS	ISOL
3	0	0	1	0	VL	HL	LOSS	ISOL	ISOL	ISOL	ISOL	LOSS	ISOL	ISOL
4	0	0	1	1	VL	HH	LOSS	ISOL	ISOL	ISOL	ISOL	ISOL	ISOL	LOSS
5	0	1	0	0	VH	VL	ISOL	ISOL	LOSS	ISOL	LOSS	ISOL	ISOL	ISOL
6	0	1	0	1	VH	VH	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL	LOSS	ISOL
7	0	1	1	0	VH	HL	ISOL	ISOL	LOSS	ISOL	ISOL	LOSS	ISOL	ISOL
8	0	1	1	1	VH	HH	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL	ISOL	LOSS
9	1	0	0	0	HL	VL	ISOL	LOSS	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL
10	1	0	0	1	HL	VH	ISOL	LOSS	ISOL	ISOL	ISOL	ISOL	LOSS	ISOL
11	1	0	1	0	HL	HL	ISOL	LOSS	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL
12	1	0	1	1	HL	HH	ISOL	LOSS	ISOL	ISOL	ISOL	ISOL	ISOL	LOSS
13	1	1	0	0	HH	VL	ISOL	ISOL	LOSS	LOSS	ISOL	ISOL	ISOL	ISOL
14	1	1	0	1	HH	VH	ISOL	ISOL	LOSS	ISOL	ISOL	LOSS	ISOL	ISOL
15	1	1	1	0	HH	HL	ISOL	ISOL	LOSS	ISOL	LOSS	ISOL	ISOL	ISOL
16	1	1	1	1	HH	HH	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL	ISOL	LOSS

### Control Voltages

HV1, Tone1, HV2, Tone2

State	Bias Condition
Low (0)	0 to 0.8 Vdc @ 5 $\mu$ A Typical
High (1)	+2.0 to +5.0 Vdc @ 25 $\mu$ A Typical

### Bias Voltage

Vdd Range = +5.0 Vdc $\pm$ 10 %		
Vdd (Vdc)	Idd (Typ.) (mA)	Idd (Max.) (mA)
+5.0	1	1.5

### DC Blocking And Decoupling Capacitors

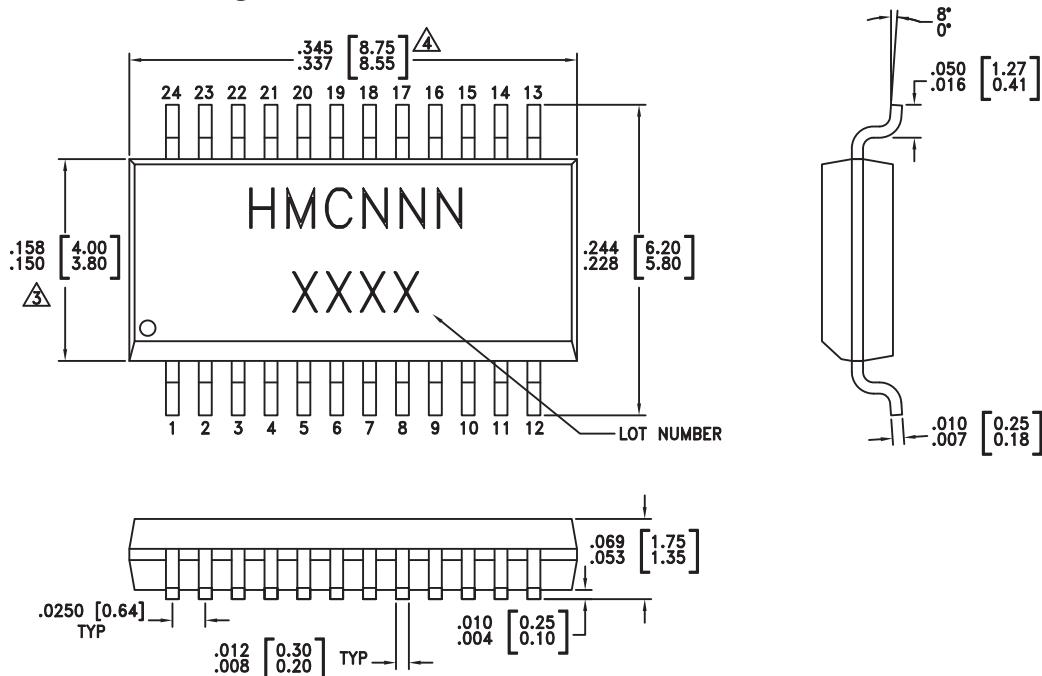
The HMC276QS24(E) requires DC blocks on all 6 RF ports (OP1, OP2, VL, HL, VH, HH). Characterization on the HMC276QS24(E) was done using 0603 size 330pF capacitors on all RF ports. A 0.01 $\mu$ F DC decoupling capacitor (0603 size) is recommended for the Vdd pin.



### Absolute Maximum Ratings

Bias Voltage Range (Vdd)	+8.0 Vdc
Control Voltage Range (All Logic Lines)	Vdd +0.5 to -0.2V Vdc
Channel Temperature	150 °C
Thermal Resistance	325 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
Maximum Input Power	+23 dBm (700 - 2150 MHz)

### Outline Drawing



#### NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

### Package Information

Part Number	Package Body Material	Leadframe Plating	MSL Rating	Package Marking <sup>[3]</sup>
HMC276QS24	Low Stress Injection Molded Plastic Silica and Silicon Impregnated	Sn/Pb Solder	MSL1 <sup>[1]</sup>	HMC276 XXXX
HMC276QS24E	RoHS-compliant Low Stress Injection Molded Plastic Silica and Silicon Impregnated	100% Matte Tin	MSL1 <sup>[2]</sup>	HMC276 XXXX

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX


**GaAs MMIC 4x2 SWITCH  
MATRIX, 0.7 - 3.0 GHz**

### Switch Application Circuit for 4x4 Switch Matrix

The HMC276QS24E switch can operate as a 4x4 switch by connecting the 4 inputs of two switches directly together.

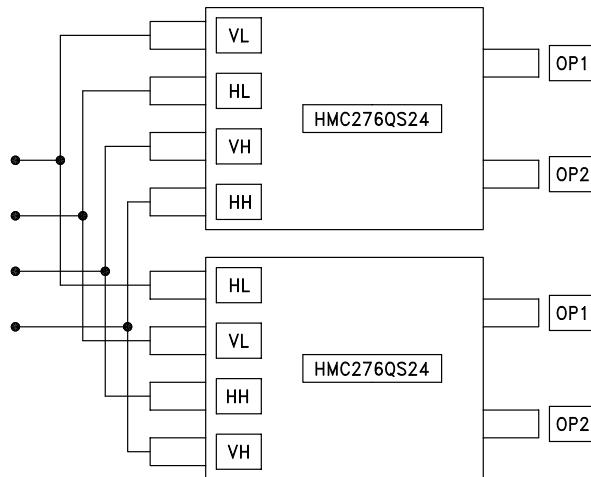
The VL, VH, HL, and HH inputs of the first switch should be connected to the second switch, as illustrated.

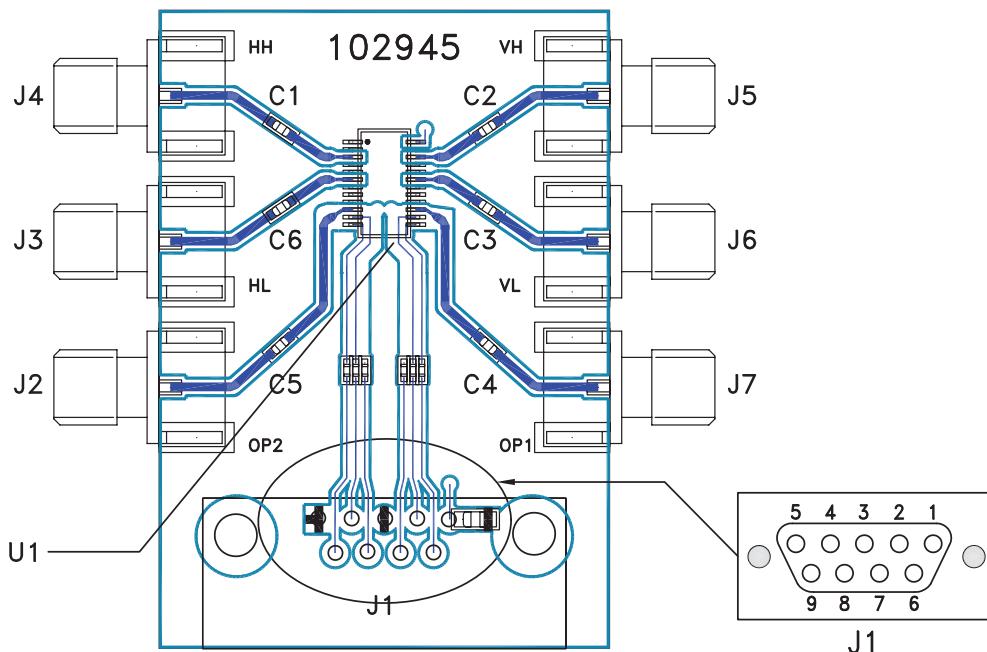
Mirror image switch performance can be realized by inverting the HV1 & HV2 logic control signals of one of the HMC276QS24E switches.

The input loading impedance of two switches in parallel should be 31.25 ohms. The output loading impedance on each output should be 75 ohms. The interconnect RF line between the switch's inputs should be an RF trace with a characteristic impedance of 62.5 ohms. This will allow the switch to remain matched in all possible switch states.

The HMC276QS24E does not provide output to output (OP1 to OP2) isolation. For this reason, It is recommended that external amplifiers should be used at each output. The amplifier's reverse isolation will provide output to output isolation, if this is necessary.

Each HMC276QS24E requires DC blocking capacitors on ALL RF input and output ports.




**Evaluation PCB**

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The circuit board used in the final application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 ohm impedance and the package ground leads should be connected directly to the ground plane similar to that shown above. A generous number of ground vias should be used to interconnect top/bottom ground planes. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.

**List of Materials for Evaluation PCB 102924<sup>[1]</sup>**

Item	Description
J2 - J7	PC Mount SMA RF Connector
J1	DC Pin
C1 - C6	100 pF Capacitor, 0402 Pkg.
U1	HMC276QS24 / HMC276QS24E 4x2 Switch Matrix
PCB <sup>[2]</sup>	102945 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

**Multi Pin DC Interface (J1)**

Pin	Line
1	Vdd
2	HV1
3	GND
4	HV2
5	GND
6	Tone1
7	N/C
8	N/C
9	Tone2