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# KAF-4320

## 2084 (H) x 2085 (V) Full Frame CCD Image Sensor

### Description

The KAF-4320 Image Sensor is a high performance monochrome area CCD (charge-coupled device) image sensor designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

The full imaging array is read out of four outputs, each of which is driven by a low impedance two stage source follower that provides a high conversion gain. This combination enables low noise at a net readout rate of 12 MHz (3 MHz per output).

**Table 1. GENERAL SPECIFICATIONS**

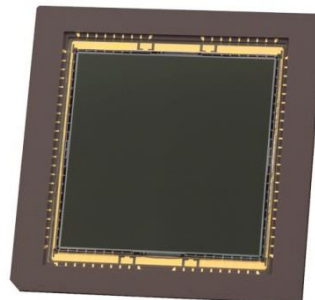
| Parameter                         | Typical Value                                                           |
|-----------------------------------|-------------------------------------------------------------------------|
| Architecture                      | Full Frame CCD                                                          |
| Total Number of Pixels            | 2092 (H) x 2093 (V)                                                     |
| Number of Active Pixels           | 2084 (H) x 2085 (V) = approx. 4.3 Mp                                    |
| Pixel Size                        | 24 $\mu\text{m}$ (H) x 24 $\mu\text{m}$ (V)                             |
| Active Image Size                 | 50.02 mm (H) x 50.02 mm (V)<br>70.7 mm (Diagonal)<br>645 Optical Format |
| Die Size                          | 52.3 mm (H) x 52.7 mm (V)                                               |
| Output Sensitivity                | 10 $\mu\text{V}/\text{e}^-$                                             |
| Saturation Signal                 | 500,000 electrons                                                       |
| Readout Noise                     | 20 electrons (3 MHz)                                                    |
| Outputs                           | 4                                                                       |
| Dark Current                      | < 15 pA/cm <sup>2</sup>                                                 |
| Dark Current Doubling Temperature | 6.4°C                                                                   |
| Dynamic Range                     | 20,000 : 1                                                              |
| Blooming Suppression              | None                                                                    |
| Maximum Data Rate                 | 3 MHz                                                                   |
| Package                           | PGA Package                                                             |
| Cover Glass                       | Clear                                                                   |

NOTE: Parameters above are specified at T = 25°C unless otherwise noted.



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**Figure 1. KAF-4320 Full Frame CCD Image Sensor**

### Features

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for High Sensitivity

### Applications

- Medical Imaging
- Scientific Imaging

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

## KAF-4320

### ORDERING INFORMATION

**Table 2. ORDERING INFORMATION – KAF-4320 IMAGE SENSOR**

| Part Number        | Description                                                                                         | Marking Code               |
|--------------------|-----------------------------------------------------------------------------------------------------|----------------------------|
| KAF-4320-AAA-JP-B1 | Monochrome, No Microlens, PGA Package,<br>Taped Clear Cover Glass (No Coatings), Grade 1            | KAF-4320-AAA<br>Lot Number |
| KAF-4320-AAA-JP-B2 | Monochrome, No Microlens, PGA Package,<br>Taped Clear Cover Glass (No Coatings), Grade 2            |                            |
| KAF-4320-AAA-JP-AE | Monochrome, No Microlens, PGA Package,<br>Taped Clear Cover Glass (No Coatings), Engineering Sample |                            |

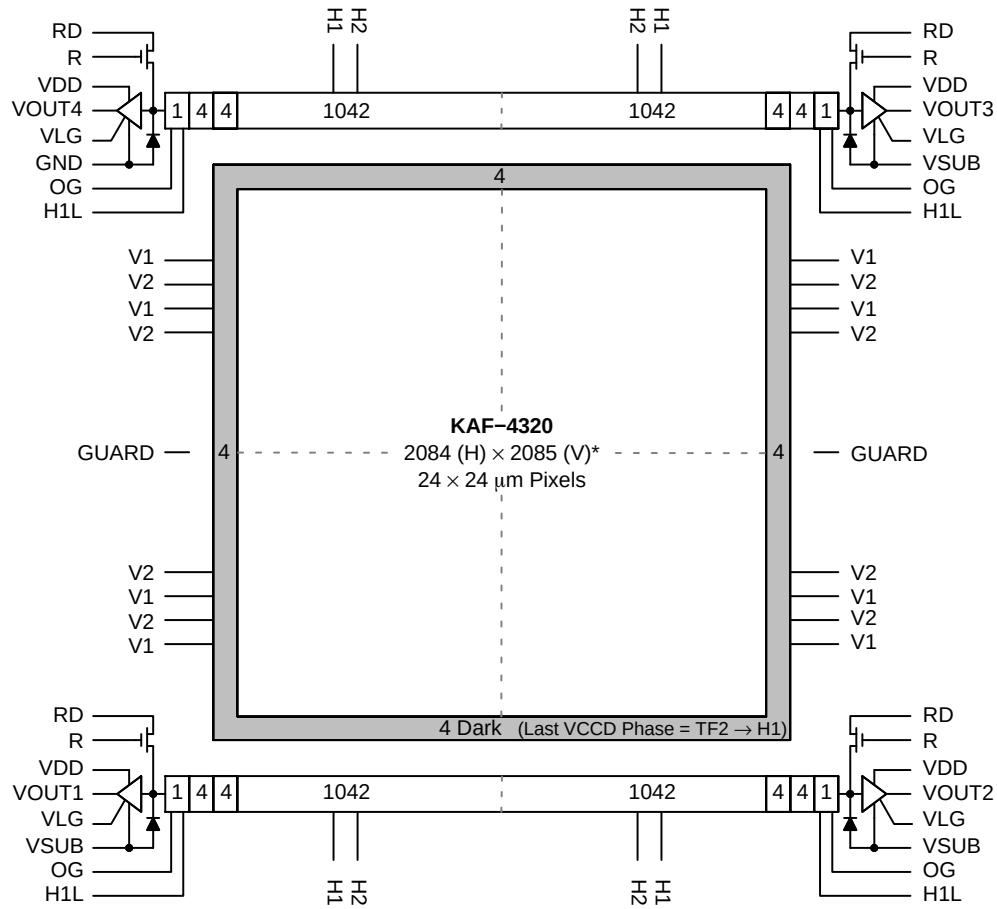
**Table 3. ORDERING INFORMATION – EVALUATION SUPPORT**

| Part Number         | Description                     |
|---------------------|---------------------------------|
| KAF-4320-16-3-A-EVK | Evaluation Board (Complete Kit) |

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.onsemi.com](http://www.onsemi.com).

## DEVICE DESCRIPTION

### Architecture



\*The center row is predominately a  $24\ \mu\text{m} \times 25\ \mu\text{m}$  polysilicon pixel that splits evenly into each half of the array. Thus, each quadrant will consist of  $1046\ (\text{H}) \times 1047\ (\text{V})$  rows where the last row will contain roughly half the signal.

Figure 2. Block Diagram

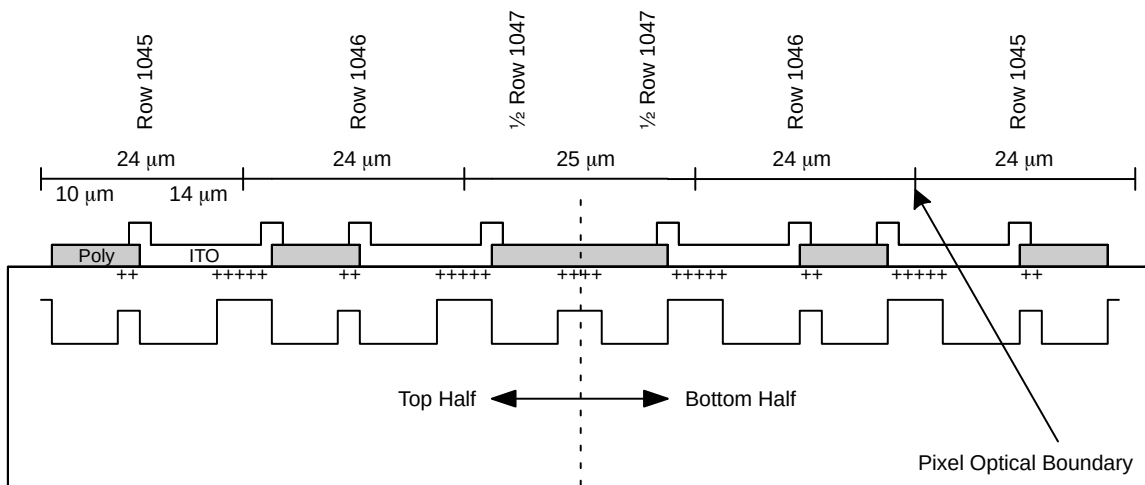


Figure 3. Horizontal Seam Cross-Section

### Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the  $\phi V1$  and  $\phi V2$  register clocks are held at a constant (low) level. See Figure 17.

### Charge Transport

Referring again to Figure 17, the integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD to the horizontal CCD register using the  $\phi V1$  and  $\phi V2$  register clocks. The horizontal CCD is presented a new line on the falling edge of  $\phi V2$  while  $\phi H1$  is held high. The horizontal CCD then transports each line, pixel by pixel, to the output structure by alternately clocking the  $\phi H1$  and  $\phi H2$  pins in a complementary fashion. On each falling edge of  $\phi H1L$  a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

### Output Structure

Charge presented to the floating diffusion is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the

floating diffusion. Once the signal has been sampled by the system electronics, the reset gate ( $\phi R$ ) is clocked to remove the signal and the floating diffusion is reset to the potential applied by  $V_{RD}$ . (See Figure 4). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the  $V_{OUT}$  pin of the device such as shown in Figure 6.

If charge binning is desired, the charge can be combined at the output node or it can be combined in the  $\phi H1L$  gate and then presented to the output node.

### Dark Reference Pixels

There are 4 light shielded pixels at the beginning of each line. There are 4 dark lines at the start of every frame and 4 dark lines at the end of each frame. Since there are outputs at each of the four corners, the light shield will affect the beginning of each line from each output, and for the first four lines from each of the outputs. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

### Dummy Pixels

Within the horizontal shift register are 4-1/2 leading pixels that are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

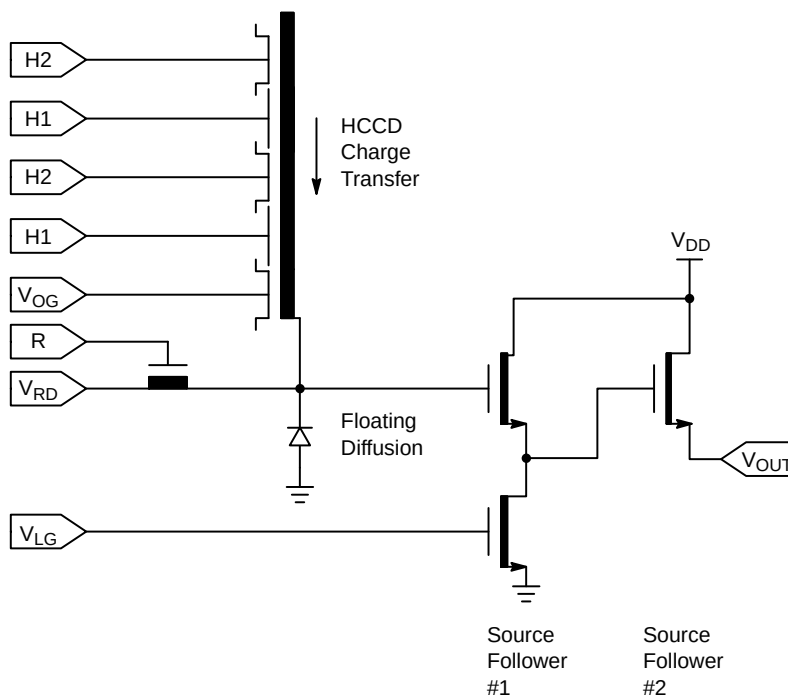


Figure 4. Output Architecture

# KAF-4320

## Physical Description

### Pin Description and Device Orientation

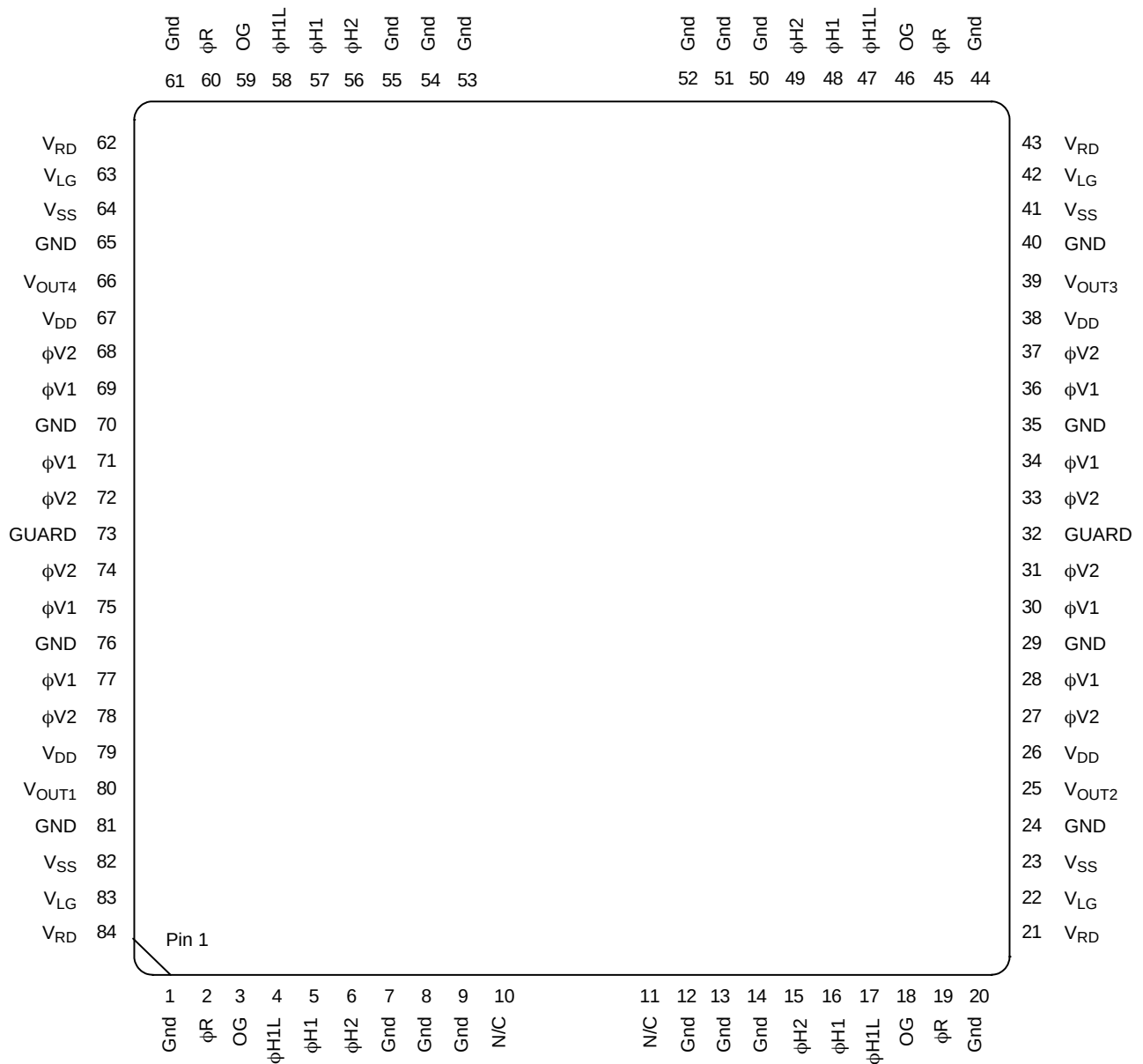


Figure 5. Pinout Diagram

Table 4. PIN DESCRIPTION

| Pin | Name       | Description                       |
|-----|------------|-----------------------------------|
| 1   | GND        | Substrate (Ground)                |
| 2   | $\phi R$   | Reset Clock                       |
| 3   | VOG        | Output Gate Bias                  |
| 4   | $\phi H1L$ | Horizontal CCD Clock – Last Phase |
| 5   | $\phi H1$  | Horizontal CCD Clock – Phase 1    |
| 6   | $\phi H2$  | Horizontal CCD Clock – Phase 2    |
| 7   | GND        | Substrate (Ground)                |
| 8   | GND        | Substrate (Ground)                |
| 9   | GND        | Substrate (Ground)                |
| 10  | N/C        | No Connect                        |
| 11  | N/C        | No Connect                        |
| 12  | GND        | Substrate (Ground)                |
| 13  | GND        | Substrate (Ground)                |
| 14  | GND        | Substrate (Ground)                |
| 15  | $\phi H2$  | Horizontal CCD Clock – Phase 2    |
| 16  | $\phi H1$  | Horizontal CCD Clock – Phase 1    |
| 17  | $\phi H1L$ | Horizontal CCD Clock – Last Phase |
| 18  | VOG        | Output Gate Bias                  |
| 19  | $\phi R$   | Reset Clock                       |
| 20  | GND        | Substrate (Ground)                |
| 21  | VRD        | Reset Drain                       |
| 22  | VLG        | Source Follower Load Gate Bias    |
| 23  | VSS        | Amplifier Supply Return           |
| 24  | GND        | Substrate (Ground)                |
| 25  | VOUT2      | Amplifier Output                  |
| 26  | VDD        | Amplifier Supply                  |
| 27  | $\phi V2$  | Vertical CCD Clock – Phase 2      |
| 28  | $\phi V1$  | Vertical CCD Clock – Phase 1      |
| 29  | GND        | Substrate (Ground)                |
| 30  | $\phi V1$  | Vertical CCD Clock – Phase 1      |
| 31  | $\phi V2$  | Vertical CCD Clock – Phase 2      |
| 32  | GUARD      | Guard Ring                        |
| 33  | $\phi V2$  | Vertical CCD Clock – Phase 2      |
| 34  | $\phi V1$  | Vertical CCD Clock – Phase 1      |
| 35  | GND        | Substrate (Ground)                |
| 36  | $\phi V1$  | Vertical CCD Clock – Phase 1      |
| 37  | $\phi V2$  | Vertical CCD Clock – Phase 2      |
| 38  | VDD        | Amplifier Supply                  |
| 39  | VOUT3      | Amplifier Output                  |
| 40  | GND        | Substrate (Ground)                |
| 41  | VSS        | Amplifier Supply Return           |
| 42  | VLG        | Source Follower Load Gate Bias    |

| Pin | Name       | Description                       |
|-----|------------|-----------------------------------|
| 43  | VRD        | Reset Drain                       |
| 44  | GND        | Substrate (Ground)                |
| 45  | $\phi R$   | Reset Clock                       |
| 46  | VOG        | Output Gate Bias                  |
| 47  | $\phi H1L$ | Horizontal CCD Clock – Last Phase |
| 48  | $\phi H1$  | Horizontal CCD Clock – Phase 1    |
| 49  | $\phi H2$  | Horizontal CCD Clock – Phase 2    |
| 50  | GND        | Substrate (Ground)                |
| 51  | GND        | Substrate (Ground)                |
| 52  | GND        | Substrate (Ground)                |
| 53  | GND        | Substrate (Ground)                |
| 54  | GND        | Substrate (Ground)                |
| 55  | GND        | Substrate (Ground)                |
| 56  | $\phi H2$  | Horizontal CCD Clock – Phase 2    |
| 57  | $\phi H1$  | Horizontal CCD Clock – Phase 1    |
| 58  | $\phi H1L$ | Horizontal CCD Clock – Last Phase |
| 59  | VOG        | Output Gate Bias                  |
| 60  | $\phi R$   | Reset Clock                       |
| 61  | GND        | Substrate (Ground)                |
| 62  | VRD        | Reset Drain                       |
| 63  | VLG        | Source Follower Load Gate Bias    |
| 64  | VSS        | Amplifier Supply Return           |
| 65  | GND        | Substrate (Ground)                |
| 66  | VOUT4      | Amplifier Output                  |
| 67  | VDD        | Amplifier Supply                  |
| 68  | $\phi V2$  | Vertical CCD Clock – Phase 2      |
| 69  | $\phi V1$  | Vertical CCD Clock – Phase 1      |
| 70  | GND        | Substrate (Ground)                |
| 71  | $\phi V1$  | Vertical CCD Clock – Phase 1      |
| 72  | $\phi V2$  | Vertical CCD Clock – Phase 2      |
| 73  | GUARD      | Guard Ring                        |
| 74  | $\phi V2$  | Vertical CCD Clock – Phase 2      |
| 75  | $\phi V1$  | Vertical CCD Clock – Phase 1      |
| 76  | GND        | Substrate (Ground)                |
| 77  | $\phi V1$  | Vertical CCD Clock – Phase 1      |
| 78  | $\phi V2$  | Vertical CCD Clock – Phase 2      |
| 79  | VDD        | Amplifier Supply                  |
| 80  | VOUT1      | Amplifier Output                  |
| 81  | GND        | Substrate (Ground)                |
| 82  | VSS        | Amplifier Supply Return           |
| 83  | VLG        | Source Follower Load Gate Bias    |
| 84  | VRD        | Reset Drain                       |

1. Like named pins (e.g. VSS) should be connected to the same supply.

## IMAGING PERFORMANCE

## Electro-Optical Specifications

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

Table 5. SPECIFICATIONS

| Description                                                                                   | Symbol            | Min.              | Nom.                          | Max.         | Units         | Notes | Verification Plan    |
|-----------------------------------------------------------------------------------------------|-------------------|-------------------|-------------------------------|--------------|---------------|-------|----------------------|
| Saturation Signal<br>Vertical CCD Capacity<br>Horizontal CCD Capacity<br>Output Node Capacity | $N_{SAT}$         | –<br>–<br>500,000 | 650,000<br>850,000<br>550,000 | –<br>–<br>–  | $e^-/pix$     | 1     | Design <sup>10</sup> |
| Quantum Efficiency (see Figure 6)                                                             |                   | –                 | –                             | –            |               |       | Design <sup>10</sup> |
| Photoresponse Non-Linearity                                                                   | PRNL              | –                 | < 1.0                         | 2.0          | %             | 2     | Design <sup>10</sup> |
| Photoresponse Non-Uniformity                                                                  | PRNU              | –                 | 0.8                           | 2.0          | %             | 3     | Design <sup>10</sup> |
| Channel to Channel Gain Difference                                                            | G                 | –                 | 0.2                           | 5            | %             | 8     | Die <sup>9</sup>     |
| Dark Signal                                                                                   | $J_{DARK}$        | –                 | 2,507                         | 54,015       | $e^-/pix/sec$ | 4     | Die <sup>9</sup>     |
| Dark Signal Doubling Temperature                                                              |                   | –                 | 6.3                           | 7            | °C            |       | Design <sup>10</sup> |
| Dark Signal Non-Uniformity                                                                    | DSNU              | –                 | 300                           | 540          | $e^-/pix/sec$ | 5     | Die <sup>9</sup>     |
| Dynamic Range                                                                                 | DR                | 86                | 87.5                          | –            | dB            | 6     | Design <sup>10</sup> |
| Output Amplifier DC Offset                                                                    | $V_{ODC}$         | $V_{RD} - 4$      | $V_{RD} - 3$                  | $V_{RD} - 2$ | V             |       | Die <sup>9</sup>     |
| Output Amplifier Sensitivity                                                                  | $V_{OUT}/N_{e^-}$ | 9                 | 10                            | 11           | $\mu V/e^-$   |       | Design <sup>10</sup> |
| Output Amplifier Output Impedance                                                             | $Z_{OUT}$         | –                 | 150                           | –            | $\Omega$      |       | Die <sup>9</sup>     |
| Noise Floor                                                                                   | $n_{e^-}$         | –                 | 17                            | 24           | electrons     | 7     | Design <sup>10</sup> |

1. The maximum output video amplitude limits the charge capacity and dynamic range. The maximum charge capacity is determined from a photon transfer measurement and is defined as the point where the mean-variance fails to demonstrate the theoretical behavior.
2. Worst case deviation from straight line fit, between 0.1% and 95% of  $V_{SAT}$ .
3. One Sigma deviation of a  $1042 \times 1042$  sample (data from one output) when the CCD is illuminated uniformly at half of saturation, excluding defective pixels.  $[100 \cdot (\text{Std Deviation} / \text{Average})]$
4. Average of all pixels with no illumination at 25°C.
5. Average dark signal of any of  $16 \times 16$  blocks within the sensor (each block is  $130 \times 130$  pixels).
6. The dynamic range limited by the noise of the output amplifier (i.e. at temperatures less than  $-10^\circ\text{C}$ ), pixel frequency = 3 MHz, and bandwidth = 10 MHz.
7. Noise floor of the CCD amplifier assuming correlated double sampling, pixel frequency = 3 MHz, and bandwidth = 10 MHz.
8.  $\Delta G = \text{abs} (100 \cdot (1 - [\text{response of a channel}] / [\text{average response of all four channels}]))$ . The specified gain difference is the combination of all the gain errors on the CCD sensor and the analog signal processing in the test system.
9. A parameter that is measured on every sensor during production testing.
10. A parameter that is quantified during the design verification activity.



TYPICAL PERFORMANCE CURVES

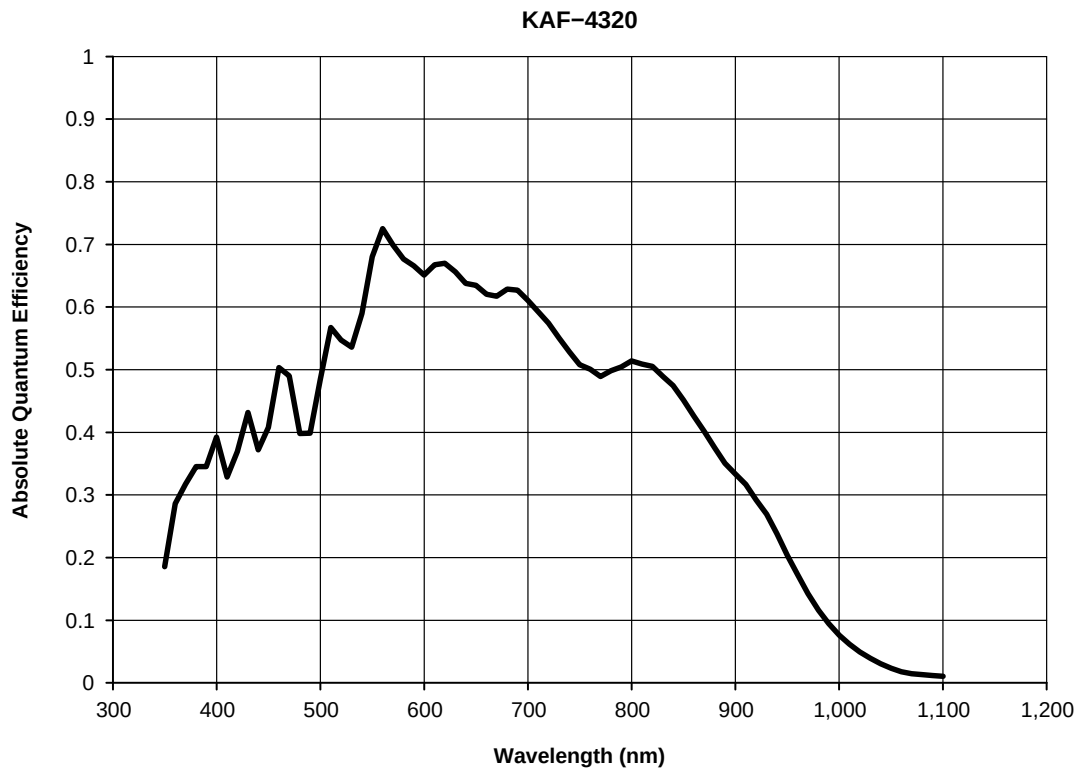


Figure 6. Typical Spectral Response

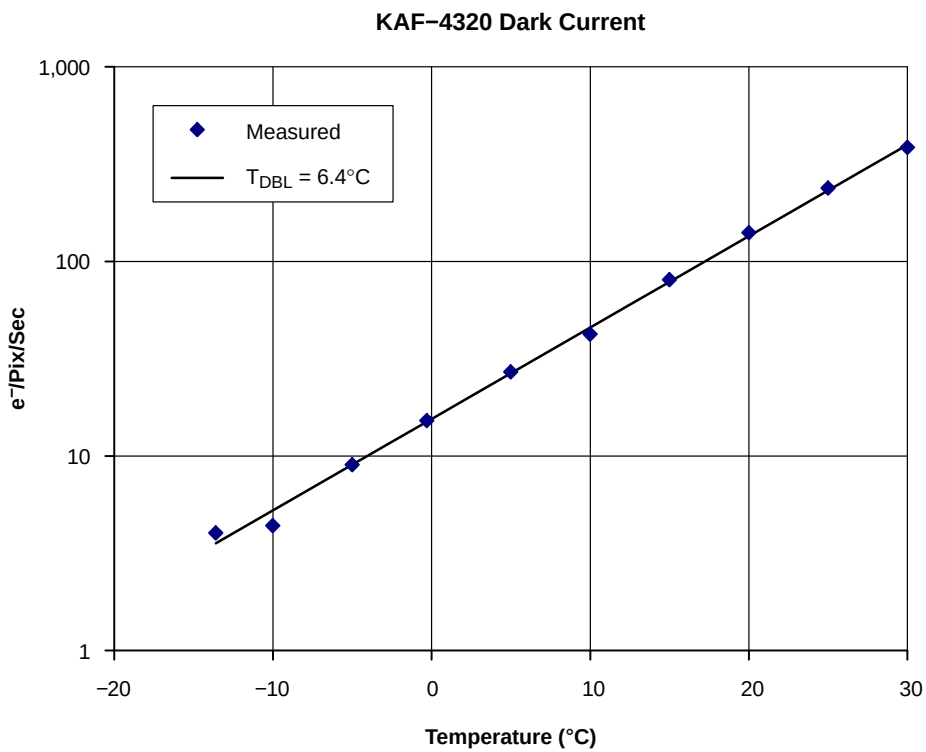


Figure 7. Dark Current Temperature Dependence

### Linearity

Figure 8 shows a typical result from measuring the signal response as a function of integration time, while the illumination level is constant. The data is fit in log space to give equal weighting between low and high signal levels. A perfectly linear system would have a slope of 1.00 in log

space. The slope in the fit is allowed to deviate from the ideal by a small amount. Typical values of the slope are between 1.00 and 1.02. The deviation from linear is defined as:

$$\% \text{ Dev} = \left| 100 \cdot \frac{[\text{Measured Value} - \text{Fit Value}]}{\text{Fit Value}} \right|$$

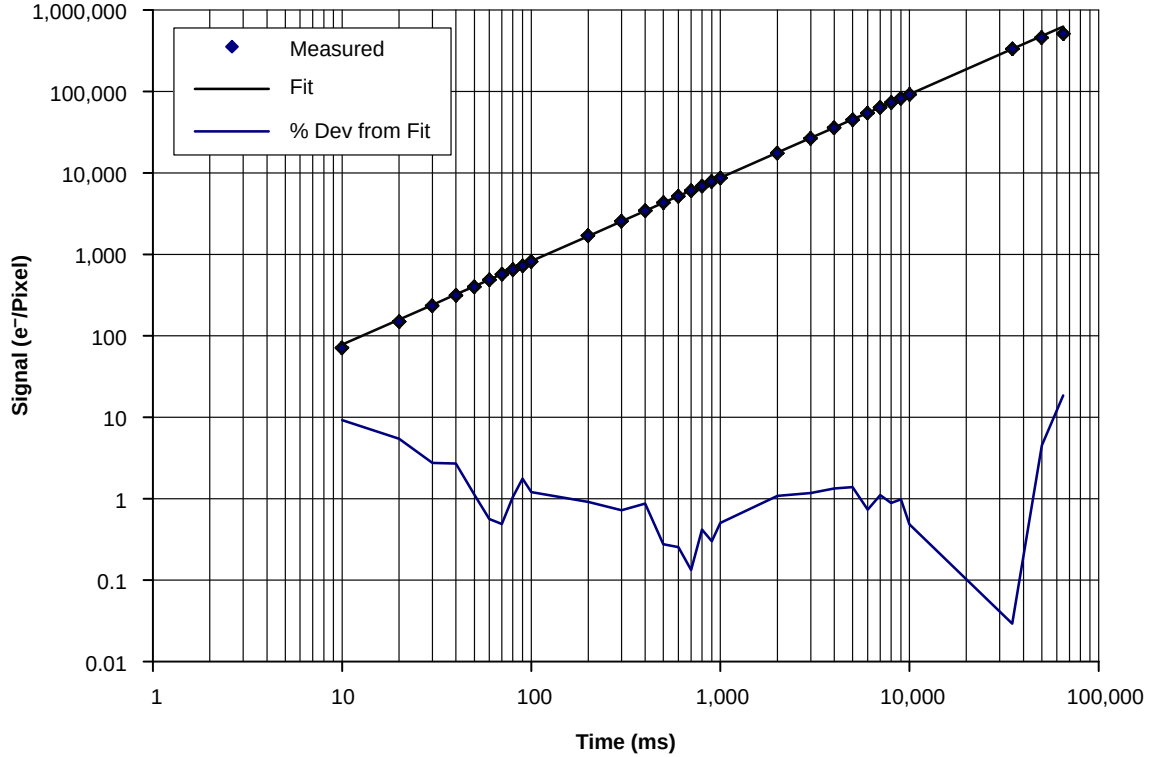


Figure 8. Linearity

### CCD Output

The following figures show typical CCD video at the output of the CCD and at the input of the analog to digital

converter (A/D) in the test system. Bandwidth limiting is applied at the A/D input to minimize the noise floor.

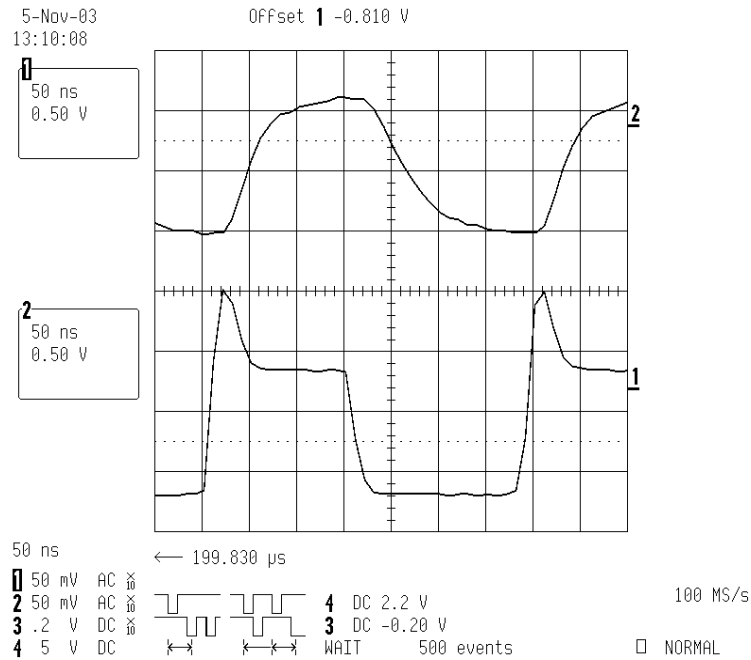


Figure 9. CCD Output: Small Signal

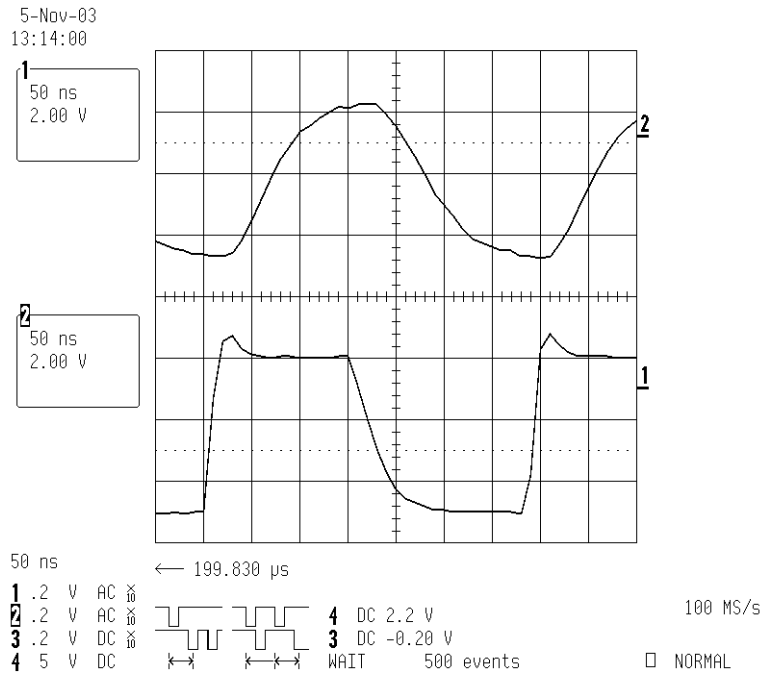


Figure 10. CCD Output: Large Signal

## Noise

The CCD amplifier noise floor, the CCD dark current during readout, and other system components such as the analog-digital converter dictate the total system noise.

### CCD Amplifier

The noise contributed by the output amplifier is determined from the amplifier's noise power spectrum, the system bandwidth, and any other analog processing. Correlated double sampling is a standard analog processing technique used with CCDs and it is assumed that it is used for all of the rest of the calculations and results in this document.

### System Noise

The total noise will be the combination of the CCD noise and the noise contributed by other components in the processing circuitry. The total noise, dominated by the CCD and the A/D converter is also shown in Figure 11. The measured values were obtained using a system that employed Datal 16 bit analog to digital converters, the ADS931 and ADS933. The system noise obtained matched the Datal specifications exactly and was similar and slightly lower than the CCD noise contribution. The table below shows the results and good agreement

between the expected and measured results for the CCD alone and the CCD in the system at 1 MHz and 3 MHz. The values in the table are in electrons referred to the CCD amplifier input.

**Table 6.**

| Frequency | CCD Measured Noise | CCD + System Datal ADS93x Measured |
|-----------|--------------------|------------------------------------|
| 1.00E+06  | 12                 | 16.2                               |
| 3.00E+06  | 17.3               | 22.6                               |

### Temperature Dependence of the Noise Floor

The temperature dependence of the noise floor is dictated primarily by the dark current generated during the readout time for the CCD. Figure 12 and Figure 13 show the expected dynamic range as a function of temperature for two pixel rates, 3 MHz and 1 MHz. The dynamic range was calculated using the measured amplifier and system noise values, the expected dark current performance, and the saturation signal. At 25°C, the dark current shot noise can contribute from 12 to 50 electrons and dominate the noise floor. The maximum dynamic range can be achieved at temperatures < -10°C for these read out frequencies.

# KAF-4320

## Noise vs. Frequency

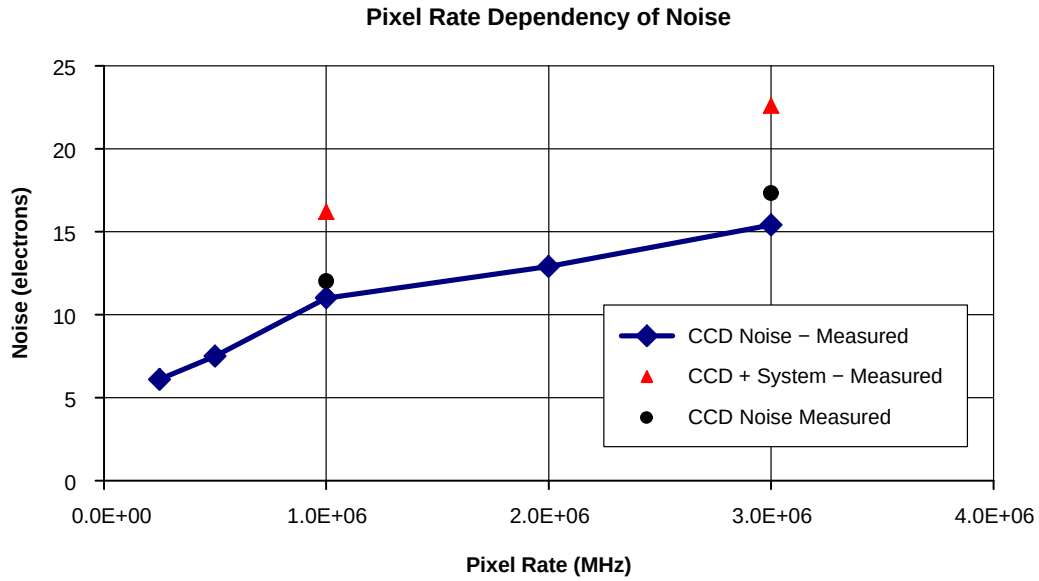
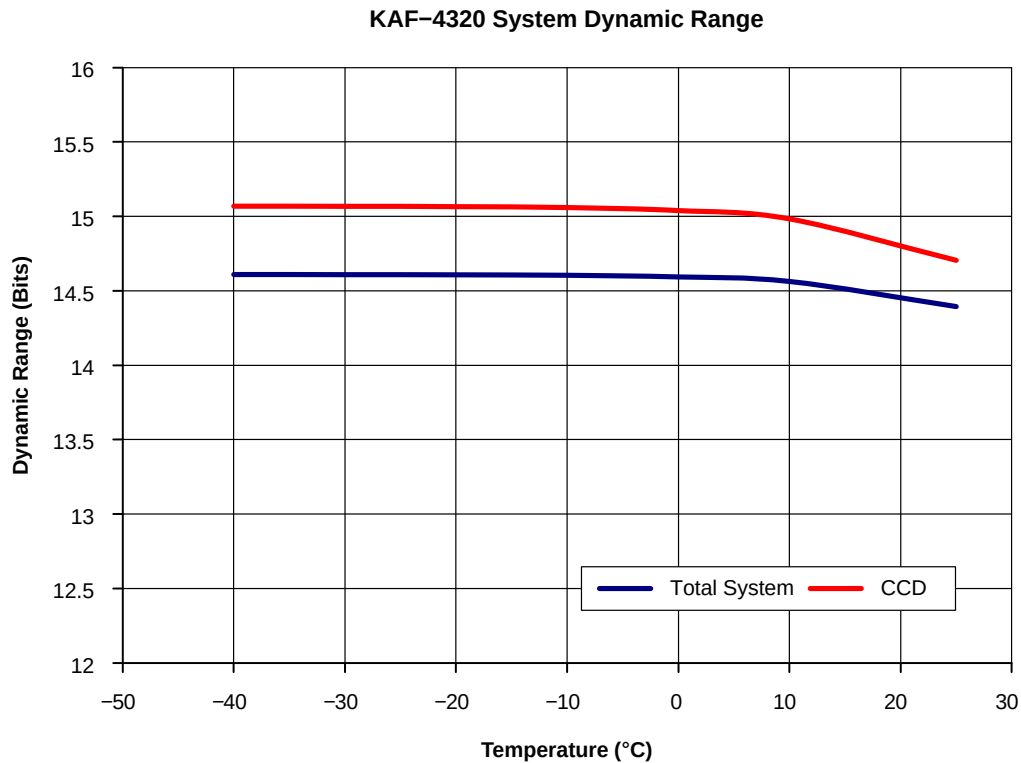


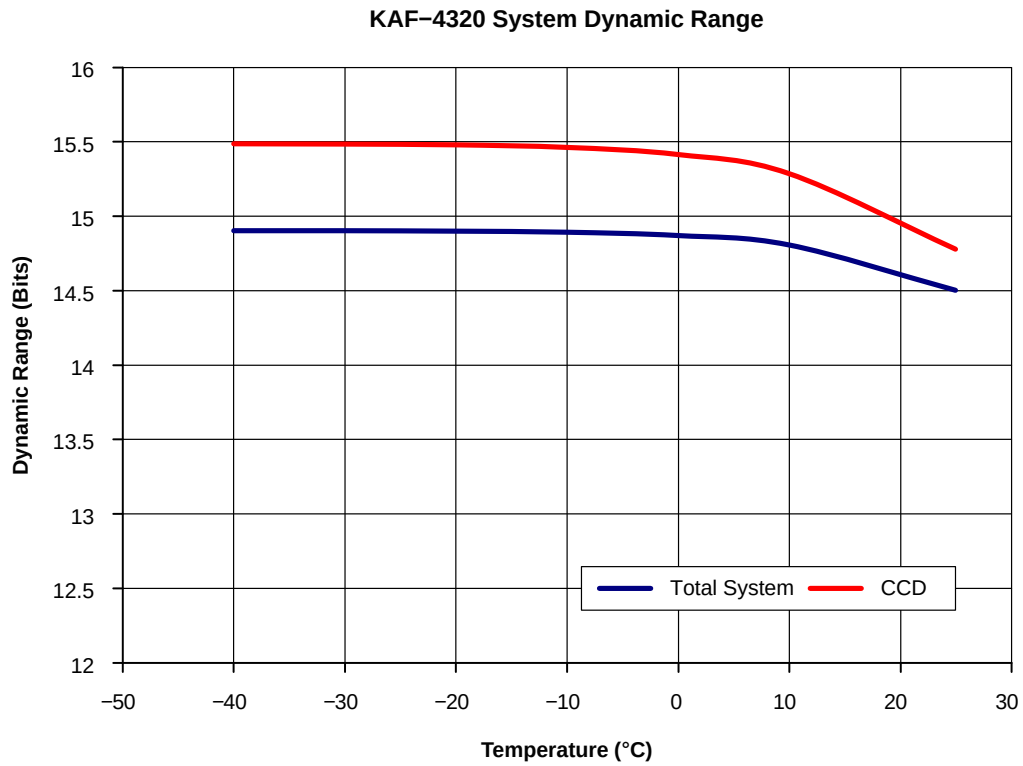
Figure 11. Noise vs. Pixel Rate

## Performance vs. Temperature



Total System Noise: CCD Readout Dark Current + CCD Amplifier + A/D Converter  
(Datel 933 16 Bit Converter)

Figure 12. Noise vs. Temperature – 3 MHz Pixel Rate



Total System Noise: CCD Readout Dark Current + CCD Amplifier + A/D Converter  
(Datel 933 16 Bit Converter)

**Figure 13. Noise vs. Temperature – 1 MHz Pixel Rate**

## DEFECT DEFINITIONS

Table 7. SPECIFICATIONS (Cosmetic tests performed at T = 25°C)

| Grade | Point Defects | Cluster Defects | Columns | Double Columns |
|-------|---------------|-----------------|---------|----------------|
| C1    | < 50          | < 20            | 0       | 0              |
| C2    | < 100         | < 20            | < 4     | 0              |

*Point Defects*

Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation.

Bright: A pixel with a dark current greater than 5,000 e<sup>-</sup>/pixel/sec at 25°C.

*Cluster Defect*

A grouping of not more than 5 adjacent point defects.

*Column Defect*

A grouping of > 5 contiguous point defects along a single column.

A column containing a pixel with dark current > 100,000 e<sup>-</sup>/pix/sec (Bright column).

A column that does not meet the minimum vertical CCD charge capacity (Low charge capacity column).

A column that loses > 3,500 e<sup>-</sup> under 2 ke<sup>-</sup> illumination (Trap defect).

*Neighboring Pixels*

The surrounding 128 × 128 pixels or ±64 columns/rows.

*Defect Separation*

Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).

Cluster defects are separated by no less than 2 pixels from other column and cluster defects.

Column defects are separated by no less than 5 pixels from other column defects.

## OPERATION

**Table 8. ABSOLUTE MAXIMUM RATINGS**

| Description                | Symbol             | Minimum | Maximum | Units | Notes   |
|----------------------------|--------------------|---------|---------|-------|---------|
| Diode Pin Voltages         | $V_{\text{DIODE}}$ | 0       | 25      | V     | 1, 2    |
| Gate Pin Voltages – Type 1 | $V_{\text{GATE1}}$ | -17     | 17      | V     | 1, 3, 6 |
| Gate Pin Voltages – Type 2 | $V_{\text{GATE2}}$ | 0       | 17      | V     | 1, 4, 6 |
| Output Bias Current        | $I_{\text{OUT}}$   | –       | -10     | mA    | 5       |
| Output Load Capacitance    | $C_{\text{LOAD}}$  | –       | 15      | pF    | 5       |

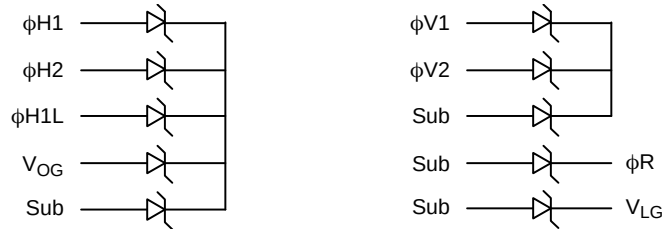
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin VSUB or between each pin in this group.
2. Includes pins: VRD, VDD, VSS, VOUT.
3. Includes pins:  $\phi V1$ ,  $\phi V2$ ,  $\phi H1$ ,  $\phi H2$ ,  $\phi H1L$ .
4. Includes pins: VOG, VLG,  $\phi R$ .
5. Avoid shorting output pins to ground or any low impedance source during operation.
6. This sensor contains gate protection circuits to provide protection against ESD events. The circuits will turn on when greater than 18 volts appears between any two gate pins. Permanent damage can result if excessive current is allowed to flow under these conditions.

### Equivalent Input Circuits

Many of the pins contain a form of gate protection to prevent damage from electrostatic discharge. These take the form of zener diodes that prevent the voltage differences

between gates from becoming large enough to damage the sensor. Isolated gates such as  $\phi R$  and  $V_{LG}$  require only protection between the gate and the sensor substrate.



**Figure 14. Equivalent Input Circuits**



Table 9. DC BIAS OPERATING CONDITIONS

| Description                | Symbol    | Minimum  | Nominal        | Maximum        | Units | Maximum DC Current (mA) | Notes |
|----------------------------|-----------|----------|----------------|----------------|-------|-------------------------|-------|
| Reset Drain                | $V_{RD}$  | –        | 18.5           | –              | V     | 0.01                    | 2     |
| Output Amplifier Return    | $V_{SS}$  | –        | 2.0            | –              | V     | 1                       | 3     |
| Output Amplifier Supply    | $V_{DD}$  | –        | 21             | –              | V     | $I_{OUT}$               | 2     |
| Substrate                  | GND       | –        | 0              | –              | V     | –                       |       |
| Output Gate                | $V_{OG}$  | –        | 0              | –              | V     | 0.01                    | 3     |
| Output Amplifier Load Gate | $V_{LG}$  | $V_{SS}$ | $V_{SS} + 1.0$ | $V_{SS} + 1.2$ | V     | 0.01                    |       |
| Guard Ring                 | GUARD     | –        | 10             | –              | V     | –                       | 3     |
| Amplifier Output Current   | $I_{OUT}$ | –        | –5             | –10            | mA    | –                       | 1     |

1. An output load sink must be applied to  $V_{OUT}$  to provide a constant current source and activate the output amplifier – see Figure 15.
2. Voltage tolerance is 2% (actual voltage should be nominal  $\pm$  tolerance).
3. Voltage tolerance is 5% (actual voltage should be nominal  $\pm$  tolerance).

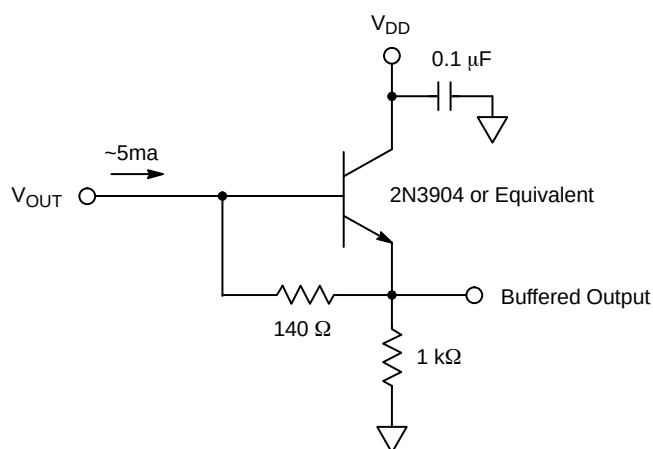


Figure 15. Example Output Structure Load Diagram

## AC Operating Conditions

Table 10. CLOCK LEVELS

| Description                      | Symbol     | Level           | Nominal | Units | Effective Capacitance                            | Notes |
|----------------------------------|------------|-----------------|---------|-------|--------------------------------------------------|-------|
| Vertical CCD Clock – Phase 1     | $\phi V1$  | Low             | -8.0    | V     | 75 nF<br>(Each of $\phi V1$ Pins 30, 34, 71, 75) | 4, 5  |
|                                  |            | Clock Amplitude | 8.0     |       |                                                  |       |
| Vertical CCD Clock – Phase 2     | $\phi V2$  | Low             | -8.0    | V     | 75 nF<br>(Each of $\phi V2$ Pins 31, 33, 72, 74) | 4, 5  |
|                                  |            | Clock Amplitude | 8.0     |       |                                                  |       |
| Horizontal CCD Clock – Phase 1   | $\phi H1$  | Low             | 0       | V     | 150 nF<br>(Each of $\phi H1$ Pins 5, 16, 48, 57) | 3, 6  |
|                                  |            | Clock Amplitude | 10.0    |       |                                                  |       |
| Horizontal CCD Clock – Last Gate | $\phi H1L$ | Low             | -3.0    | V     | 10 pF                                            | 3     |
|                                  |            | Clock Amplitude | 10.0    |       |                                                  |       |
| Horizontal CCD Clock – Phase 2   | $\phi H2$  | Low             | -3.0    | V     | 100 pF                                           | 3, 7  |
|                                  |            | Clock Amplitude | 10.0    |       |                                                  |       |
| Reset Clock                      | $\phi R$   | Low             | 2.0     | V     | 5 pF                                             | 3     |
|                                  |            | Clock Amplitude | 12.0    |       |                                                  |       |

1. All pins draw less than 10  $\mu A$  DC current.
2. Capacitance values relative to  $V_{SUB}$ .
3. Voltage tolerance is 2% (actual voltage should be nominal  $\pm$  tolerance).
4. Voltage tolerance is 5% (actual voltage should be nominal  $\pm$  tolerance).
5. Total clock capacitance is  $4 \cdot 75 \text{ nF} = 300 \text{ nF}$ .
6. Total clock capacitance is  $4 \cdot 150 \text{ pF} = 600 \text{ pF}$ .
7. Total clock capacitance is  $4 \cdot 100 \text{ pF} = 400 \text{ pF}$ .

## AC Timing Conditions

Table 11. AC TIMING CONDITIONS

| Description                             | Symbol        | Minimum | Nominal | Maximum | Units   | Notes   |
|-----------------------------------------|---------------|---------|---------|---------|---------|---------|
| $\phi H1$ , $\phi H2$ Clock Frequency   | $f_H$         | –       | 3       | 3       | MHz     | 1, 2, 3 |
| Pixel Period (1 Count)                  | $t_e$         | 333     | 333     | –       | ns      |         |
| $\phi H1$ , $\phi H2$ Set-up Time       | $t_{\phi HS}$ | 10      | 10      | –       | $\mu s$ |         |
| $\phi V1$ , $\phi V2$ Clock Pulse Width | $t_{\phi V}$  | 30      | 30      | –       | $\mu s$ | 2       |
| Reset Clock Pulse Width                 | $t_{\phi R}$  | –       | 20      | –       | ns      | 4       |
| Readout Time                            | $t_{READOUT}$ | 470.3   | 470.3   | –       | ms      | 5       |
| Integration Time                        | $t_{INT}$     | –       | –       | –       |         | 6       |
| Line Time                               | $t_{LINE}$    | 449.6   | 449.6   | –       | $\mu s$ | 7       |

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5–10% of clock period. Crossover of register clocks should be between 40–60% of amplitude.
4.  $\phi R$  should be clocked continuously.
5.  $t_{READOUT} = (1046 \cdot t_{LINE})$
6. Integration time ( $t_{INT}$ ) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7.  $t_{LINE} = (3 \cdot t_{\phi V}) + t_{\phi HS} + (1050 \cdot t_e)$ .
8. When combining the image from the upper half of the device with that from the lower half, line 1047 from each must be added together and gained (approx. 1.2X) to match the other 1046 lines.

### Pixel Rate Clock Waveforms

For best performance, the horizontal clocks should be damped, similar to those shown in Figure 16. The clocks in

this figure were generated using a 50  $\Omega$  output impedance clock driver. Excessively fast clocks can result in a higher noise floor.

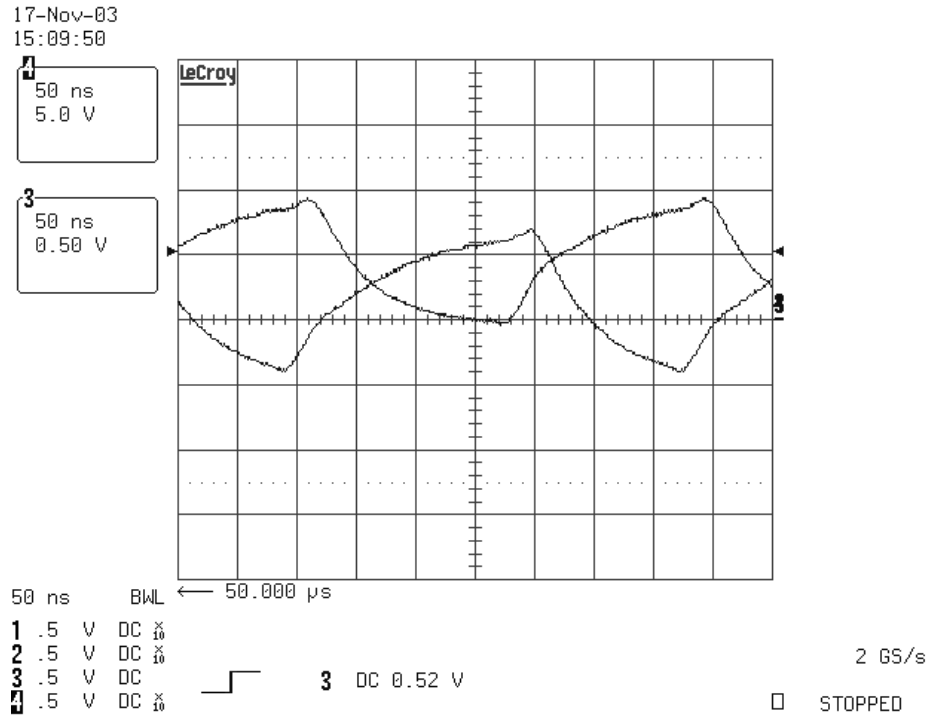


Figure 16. Clock Example

## TIMING

### Normal Read Out

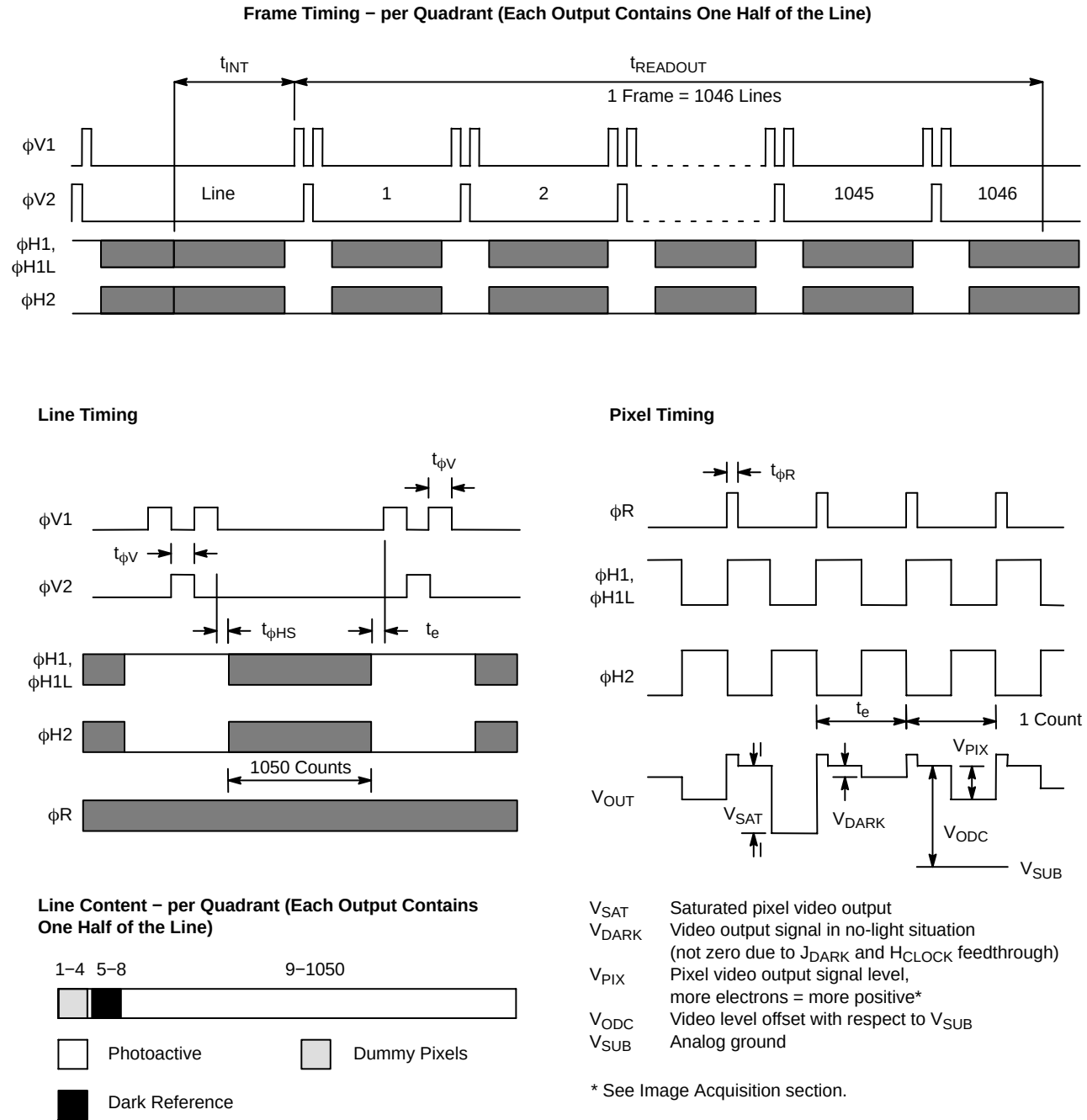


Figure 17. Timing Diagrams

### Power Dissipation

The power dissipated by the CCD clocks is calculated using the formula:

$$\text{Power} = C \cdot V^2 \cdot f$$

Where C is the capacitance in farads, V is the clock amplitude in volts, and f is the frequency in Hz.

### Amplifier Power

The power dissipated by amplifiers is calculated by  $\text{Power} = I \cdot V$  where I is the current and V is the voltage drop on the CCD. The sensor contains two stage source followers. The first stage draws approximately 250 micro amps and the

voltage drop is  $V_{DD} - V_{SS}$ . The second stage sources much more current, approximately 5 mA while the voltage drop on the sensor is much smaller,  $V_{DD} - V_{OUT}$  where  $V_{OUT} \sim V_{RD}$ .

### Total Power

The table below shows the power dissipated at three different pixel frequencies. For each of these cases the amplifier operating conditions are held constant so its contribution is not frequency dependent. The time for the vertical clock transfers is also held constant (90 microseconds per line) but the line time changes depending on the pixel rate.

**Table 12. TOTAL POWER**

| Contributor | Pixel Rate |        |        | Notes              |
|-------------|------------|--------|--------|--------------------|
|             | 500 kHz    | 1 MHz  | 3 MHz  |                    |
| Amplifiers  | 120 mW     | 120 mW | 120 mW | Total of 4 Outputs |
| HCCD        | 60 mW      | 120 mW | 360 mW |                    |
| VCCD        | 62 mW      | 121 mW | 297 mW |                    |
| Total       | 241 mW     | 361 mW | 776 mW |                    |

### CCD Surface Flatness

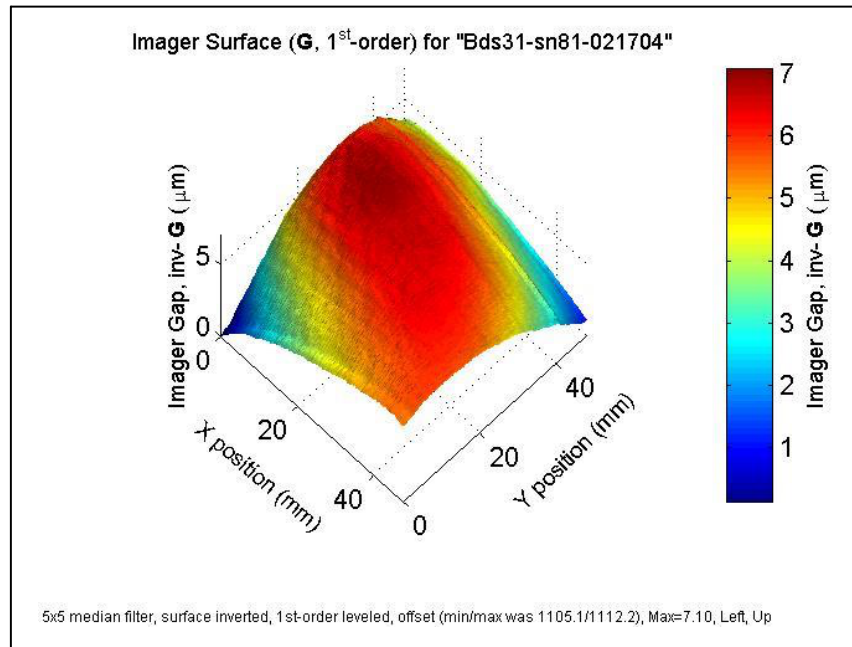
The flatness of the die is defined as a peak-to-peak distortion in the image sensor surface. The parallelism between the image sensor surface and any of the package

components is not specified or guaranteed. The non-parallelism is removed when measuring the distortion in the image sensor surface.

**Table 13.**

|              |                         | Minimum | Nominal | Maximum | Unit    |
|--------------|-------------------------|---------|---------|---------|---------|
| Die Flatness | Peak-to-Peak Distortion | –       | 8.8     | 12.0    | microns |

Some examples of profiles of some typical image sensors surfaces are shown below.



**Figure 18. Die Flatness Data**

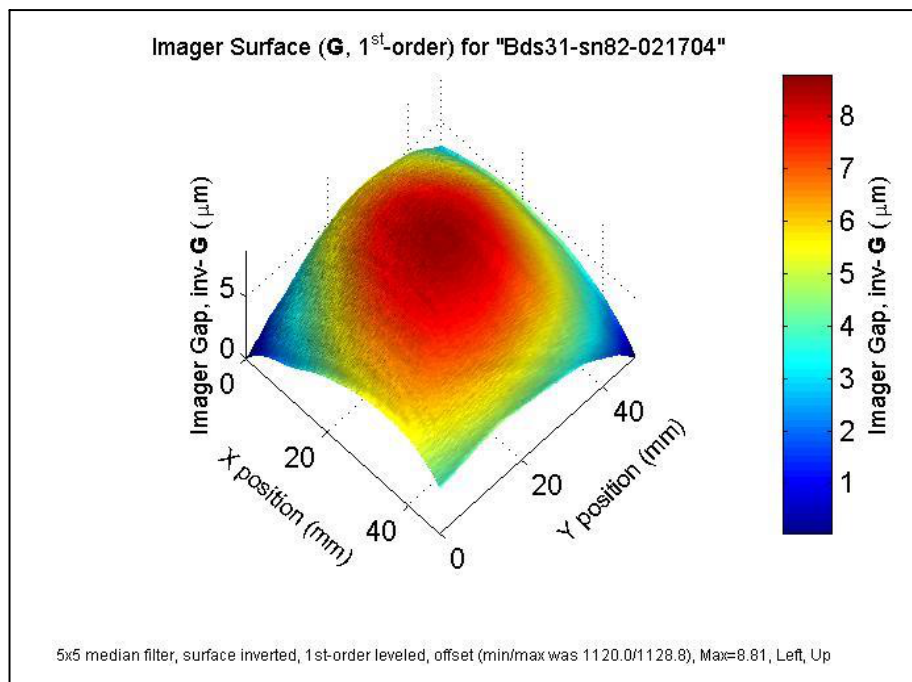


Figure 19. Die Flatness Data

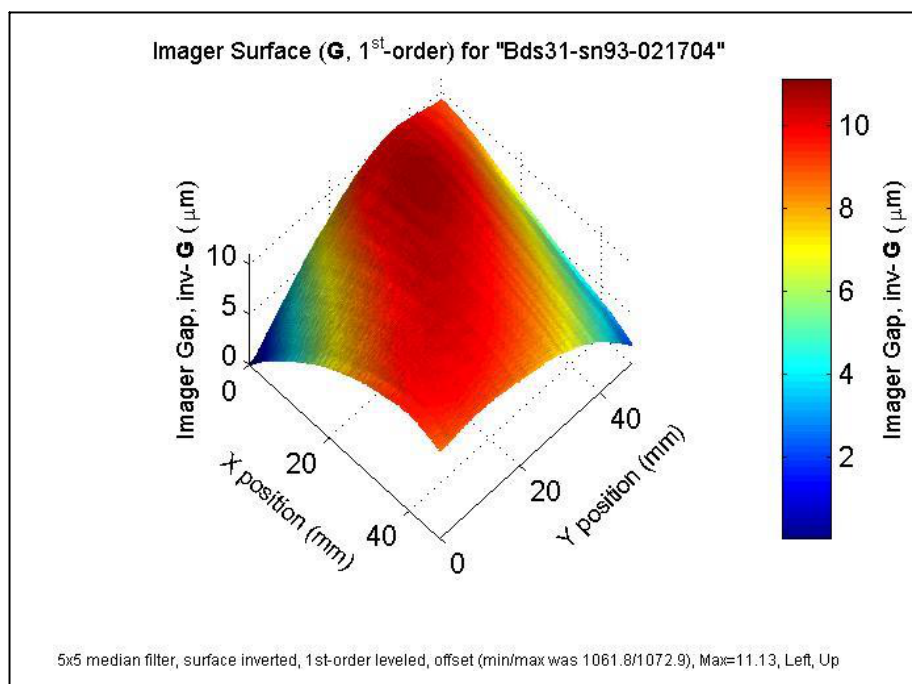


Figure 20. Die Flatness Data

## STORAGE AND HANDLING

Table 14. STORAGE CONDITIONS

| Description           | Symbol          | Minimum | Maximum | Units | Notes |
|-----------------------|-----------------|---------|---------|-------|-------|
| Storage Temperature   | T <sub>ST</sub> | -100    | 80      | °C    | 1     |
| Operating Temperature | T <sub>OP</sub> | -70     | 50      | °C    |       |

1. Image sensors with temporary cover glass should be stored at room temperature (nominally 25°C) in dry nitrogen.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from [www.onsemi.com](http://www.onsemi.com).

For information on soldering recommendations, please download the *Soldering and Mounting Techniques Reference Manual* (SOLDERRM/D) from [www.onsemi.com](http://www.onsemi.com).

For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from [www.onsemi.com](http://www.onsemi.com).

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from [www.onsemi.com](http://www.onsemi.com).

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](http://www.onsemi.com) from [www.onsemi.com](http://www.onsemi.com).

## MECHANICAL INFORMATION

## Completed Assembly

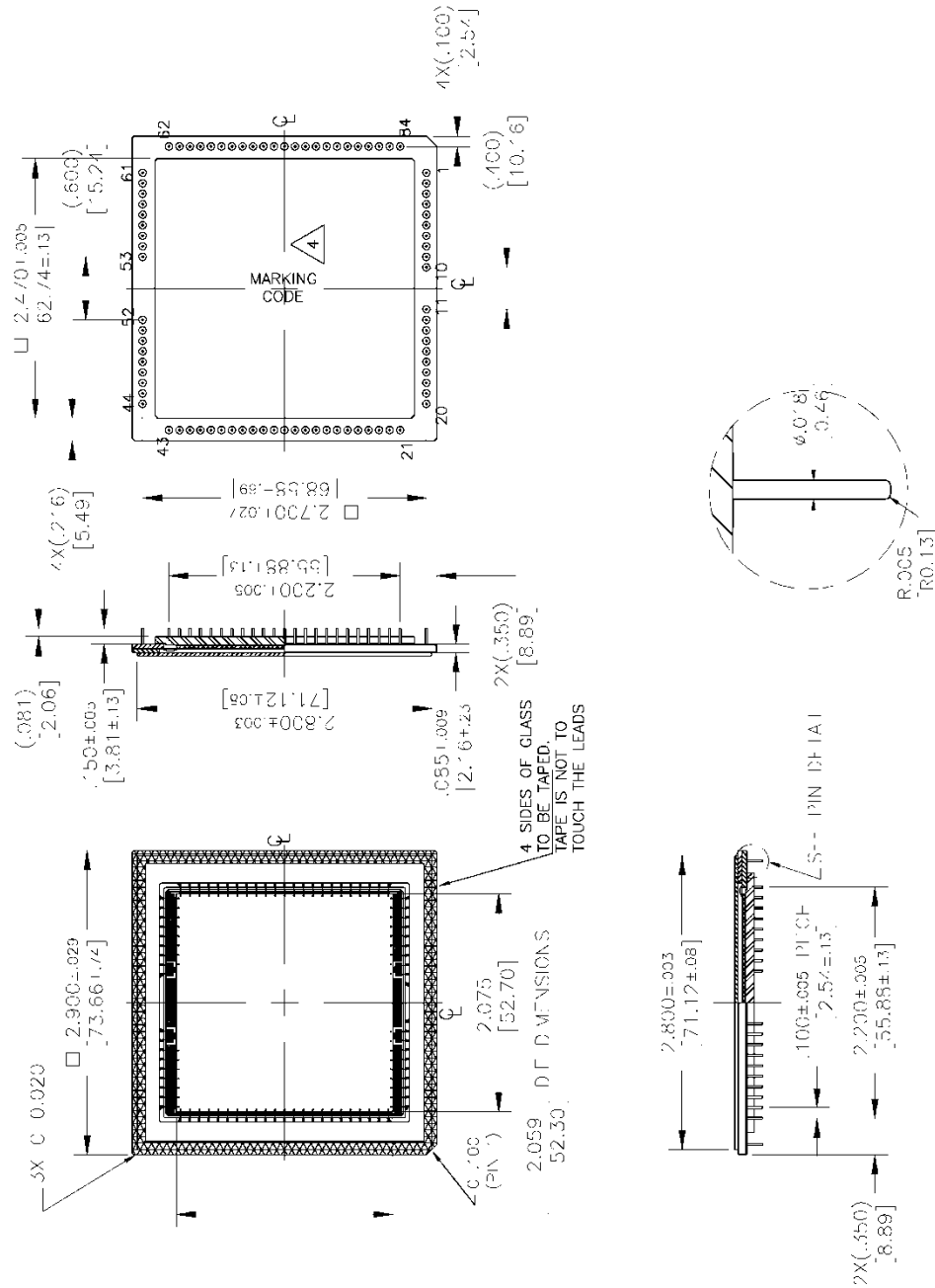


Figure 21. Completed Assembly (1 of 2)



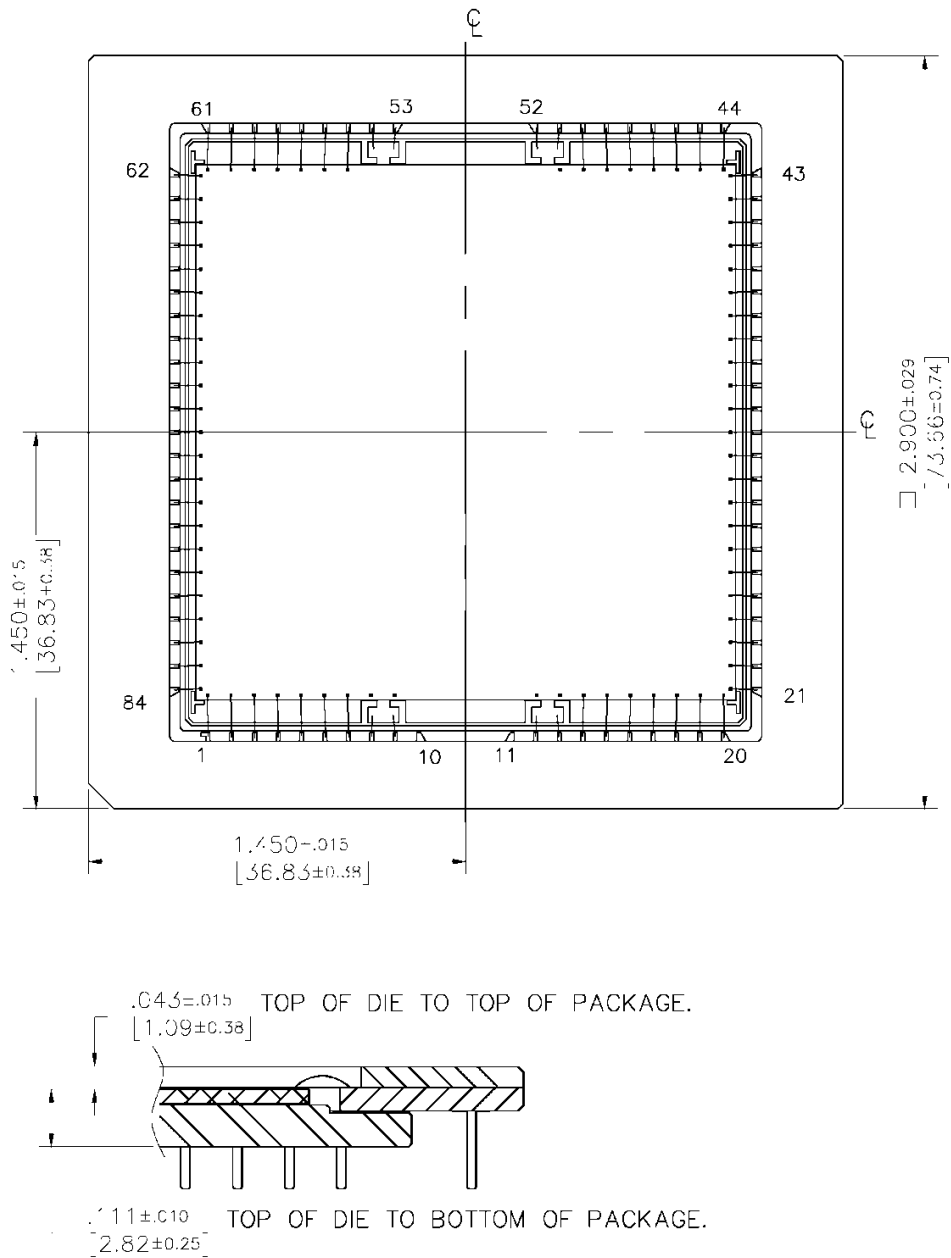


Figure 22. Completed Assembly (2 of 2)

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