



CYPRESS

ADVANCED INFORMATION

CY27C040

512K x 8 CMOS EPROM

Features

- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 70$ ns max.
- Low power
 - 140 mW max.
 - Less than 550 μ W when deselected
- Byte-wide memory organization
- 100% reprogrammable in the windowed package
- EPROM technology
- Capable of withstanding >2001V static discharge
- Available in
 - 32-pin PLCC
 - 32-pin TSOP-I
 - 32-pin, 600-mil plastic or hermetic DIP
 - 32-pin hermetic LCC

Functional Description

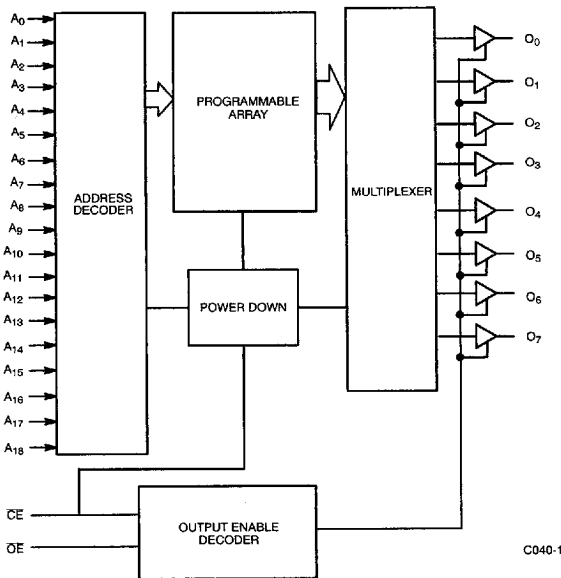
The CY27C040 is a high-performance, 4-megabit CMOS EPROM organized in 512 Kbytes. It is available in industry-standard 32-pin, 600-mil DIP, 32-pin LCC and PLCC, and 32-pin TSOP-I packages. The CY27C040 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27C040 is equipped with a power-down chip enable (\overline{CE}) input and output enable (\overline{OE}). When \overline{CE} is deasserted, the device powers down to a low-power standby mode. The \overline{OE} pin three-states the outputs without putting the device into standby mode. While \overline{CE} offers lower power, \overline{OE} provides a more rapid transition to and from three-stated outputs.

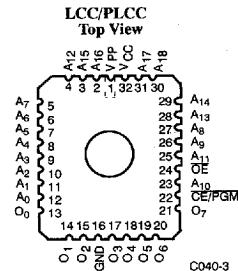
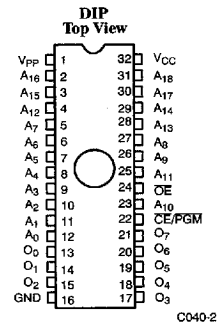
The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supravoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

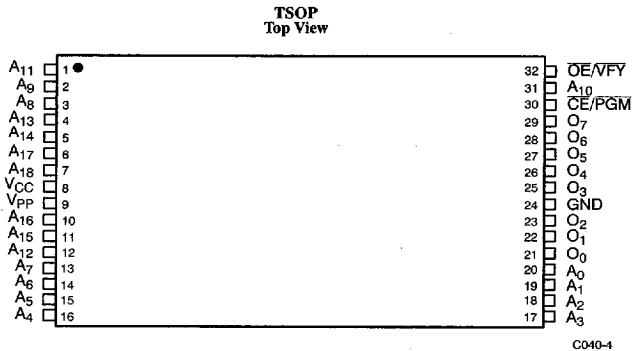
The CY27C040 is read by asserting both the \overline{CE} and the \overline{OE} inputs. The contents of the memory location selected by the address on inputs $A_{18}-A_0$ will appear at the outputs O_7-O_0 .

Logic Block Diagram



Pin Configurations



Pin Configurations (continued)

Selection Guide

		27C040-70	27C040-90	27C040-120	27C040-150	27C040-200
Maximum Access Time (ns)		70	90	120	150	200
CE Access Time (ns)		70	90	120	150	200
OE Access Time (ns)		30	35	40	50	60
I _{CC} ^[1] (mA) Power Supply Current	Com'l	25	25	25	25	25
	Mil		30	30	30	30
I _{SB} ^[2] (μA) CMOS Stand-by Current		100	100	100	100	100
I _{SB} ^[3] (mA) TTL Stand-by Current		1	1	1	1	1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State -0.5V to +5.5V
 DC Input Voltage -3.0V to +7.0V
 Transient Input Voltage -3.0V for <20 ns
 DC Program Voltage 13.0V

Notes:

1. V_{CC} = Max., I_{OUT} = 0 mA, f = 5 MHz.
2. V_{CC} = Max., CE = V_{CC} - 0.3V to V_{CC} + 1.0V.
3. V_{CC} = Max., CE = V_{IH}.

UV Erasure 7258 Wsec/cm²
 Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)
 Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial ^[4]	-40°C to +85°C	5V ± 10%
Military ^[5]	-55°C to +125°C	5V ± 10%

4. Contact a Cypress representative for industrial temperature range specification.
5. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range^[6, 7]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -400 μ A	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA		0.45	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0	V _{CC} +0.5	V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8	V
I _{IX}	Input Leakage Current	GND \leq V _{IN} \leq V _{CC}	-10	+10	μ A
I _{OZ}	Output Leakage Current	GND \leq V _{OUT} \leq V _{CC} , Output Disable	-10	+10	μ A
I _{CC}	Power Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=5 MHz	Com'l	25	mA
			Mil	30	mA
I _{SB}	Stand-By Current	V _{CC} =Max., CE = V _{IH}	Com'l	1	mA
			Mil	1	mA

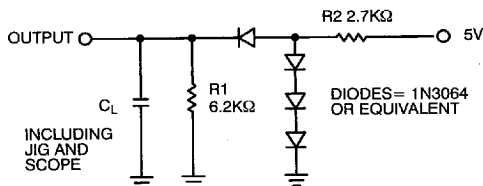
Capacitance^[7]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

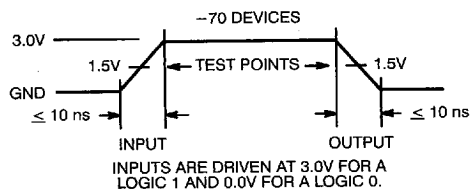
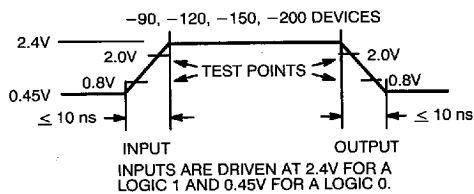
Notes:

6. See the last page of this specification for Group A subgroup testing information.

7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms


C_L = 100 pF FOR -90, -120, -150, -200 DEVICES
C_L = 30 pF FOR -70 DEVICES

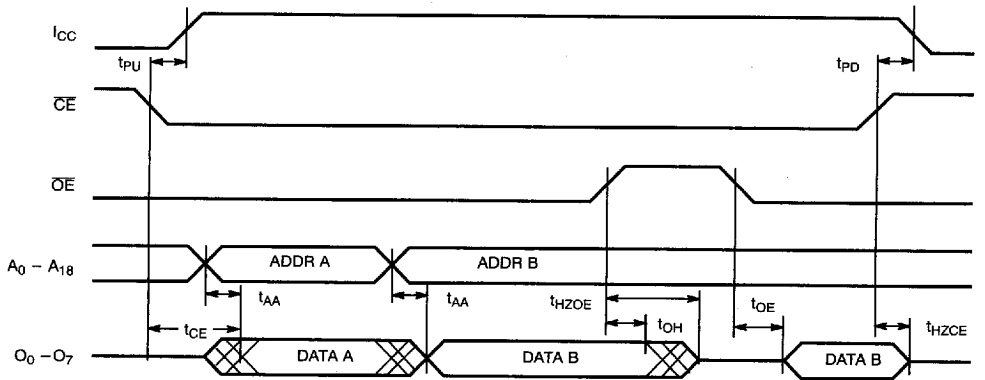


C040-5

C040-6

Switching Characteristics Over the Operating Range

Parameter	Description	27C040-70		27C040-90		27C040-120		27C040-150		27C040-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{OE}	OE Active to Output Valid		30		35		40		50		60	ns
t_{HZOE}	OE Inactive to High Z		25		25		30		30		40	ns
t_{CE}	CE Active to Output Valid		70		90		120		150		200	ns
t_{HZCE}	CE Inactive to High Z		25		25		30		30		40	ns
t_{PU}	CE Active to Power-Up	0		0		0		0		0		ns
t_{PD}	CE Inactive to Power-Down		60		65		65		65		70	ns
t_{OH}	Output Data Hold	0		0		0		0		0		ns

Switching Waveform


C040-7

Erase Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY27C040 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating, the exposure time would be approximately 35 minutes. The CY27C040 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the

EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V _{PP}	Programming Power Supply	12.5	13	V
I _{PP}	Programming Supply Current		50	mA
V _{IHP}	Programming Input Voltage HIGH	3.0	V _{CC}	V
V _{ILP}	Programming Input Voltage LOW	-0.5	0.4	V
V _{CCP}	Programming V _{CC}	6.0	6.5	V

Table 2. Mode Selection

Mode	Pin Function ^[8]					
	CE/PGM	OE	V _{PP}	A ₀	A ₉	Data
Read	V _{IL}	V _{IL}	V _{IH}	A ₀	A ₉	O ₇ - O ₀
Output Disable	V _{IL}	V _{IH}	V _{IH}	A ₀	A ₉	High Z
Stand-by (CMOS)	V _{CC} - 0.3V	X	V _{IH}	A ₀	A ₉	High Z
Stand-by (TTL)	V _{IH}	X	V _{IH}	X	X	High Z
Program	V _{ILP}	V _{IHP}	V _{PP}	A ₀	A ₉	D ₇ - D ₀
Program Verify	V _{ILP}	V _{ILP}	V _{PP}	A ₀	A ₉	O ₇ - O ₀
Program Inhibit	V _{IHP}	X	V _{PP}	A ₀	A ₉	High Z
Signature Read (MFG)	V _{IL}	V _{IL}	V _{IH}	V _{IL}	V _{HV} ^[9]	34H
Signature Read (DEV)	V _{IL}	V _{IL}	V _{IH}	V _{IH}	V _{HV} ^[9]	Note 10

Note:

8. X can be V_{IL} or V_{IH}.

9. V_{HV} = 12V ± 0.5V

10. To be determined.

Ordering Information^[11]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C040-70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040-70PC	P15	32-Lead (600-Mil) Molded DIP	
	CY27C040-70WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040-70ZC	Z32	32-Lead Thin Small Outline Package	
90	CY27C040-90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040-90PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040-90WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040-90ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040-90DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040-90LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040-90QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040-90WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
120	CY27C040-120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040-120PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040-120WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040-120ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040-120DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040-120LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040-120QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040-120WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
150	CY27C040-150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040-150PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040-150WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040-150ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040-150DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040-150LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040-150QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040-150WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
200	CY27C040-200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C040-200PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27C040-200WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27C040-200ZC	Z32	32-Lead Thin Small Outline Package	
	CY27C040-200DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27C040-200LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27C040-200QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27C040-200WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

Notes:

11. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

**MILITARY SPECIFICATIONS****Group A Subgroup Testing****DC Characteristics**

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AA}	7, 8, 9, 10, 11
t _{OE}	7, 8, 9, 10, 11
t _{CE}	7, 8, 9, 10, 11

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