

HIGH-SPEED DIFFERENTIAL LINE DRIVERS AND RECEIVERS

Check for Samples: [SN65LVDS180-Q1](#), [SN65LVDS050-Q1](#), [SN65LVDS051-Q1](#)

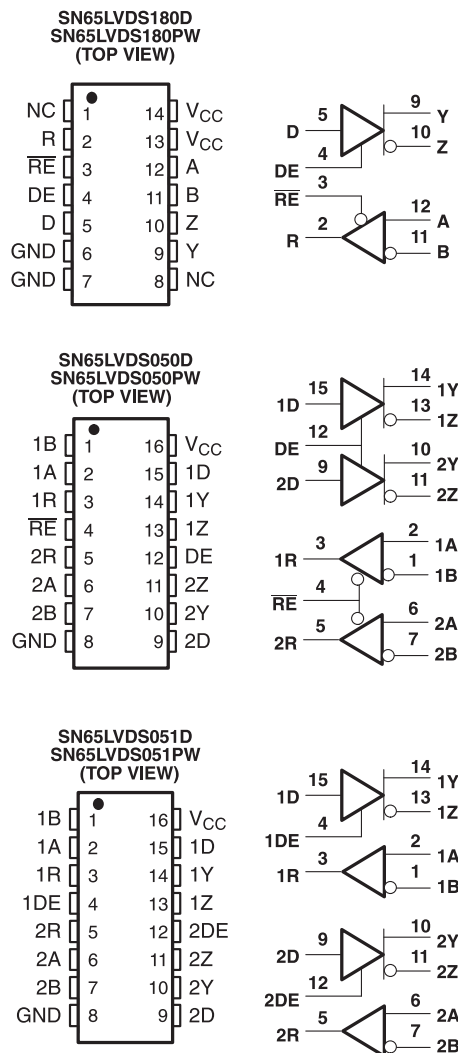
FEATURES

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995 Standard
- Signaling Rates up to 400 Mbps
- Bus-Terminal ESD Exceeds 12 kV
- Operates From a Single 3.3-V Supply
- Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV and a 100-Ω Load
- Propagation Delay Times
 - Driver: 1.7 ns Typ
 - Receiver: 3.7 ns Typ
- Power Dissipation at 200 MHz
 - Driver: 25 mW Typical
 - Receiver: 60 mW Typical
- LVTTTL Input Levels Are 5-V Tolerant
- Receiver Maintains High Input Impedance With $V_{CC} < 1.5$ V
- Receiver Has Open-Circuit Fail Safe

DESCRIPTION

The SN65LVDS180, SN65LVDS050, and SN65LVDS051 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The TIA/EIA-644 standard compliant electrical interface provides a minimum differential output voltage magnitude of 247 mV into a 100-Ω load and receipt of 50-mV signals with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The devices offer various driver, receiver, and enabling combinations in industry standard footprints. Since these devices are intended for use in simplex or distributed simplex bus structures, the driver enable function does not put the differential outputs into a high-impedance state but rather disconnects the input and reduces the quiescent power used by the device. (For these functions with a high-impedance driver output, see the SN65LVDM series of devices.) All devices are characterized for operation from -40°C to 85°C .

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC (D)	Tape and reel	SN65LVDS180DRQ1	VDS180Q
	TSSOP (PW)	Tape and reel	SN65LVDS180PWRQ1	VDS180Q
	SOIC (D)	Tape and reel	SN65LVDS050DRQ1 ⁽³⁾	VDS050Q
	TSSOP (PW)	Tape and reel	SN65LVDS050IPWRQ1	VDS050Q
	SOIC (D)	Tape and reel	SN65LVDS051DRQ1	VDS051Q
	TSSOP (PW)	Tape and reel	SN65LVDS051PWRQ1	VDS051Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) Product Preview

FUNCTION TABLES

SN65LVDS180, SN65LVDS050, and SN65LVDS051 RECEIVER⁽¹⁾

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 50\text{ mV}$	L	H
$-50\text{ mV} < V_{ID} < 50\text{ mV}$	L	?
$V_{ID} \leq -50\text{ mV}$	L	L
Open	L	H
X	H	Z

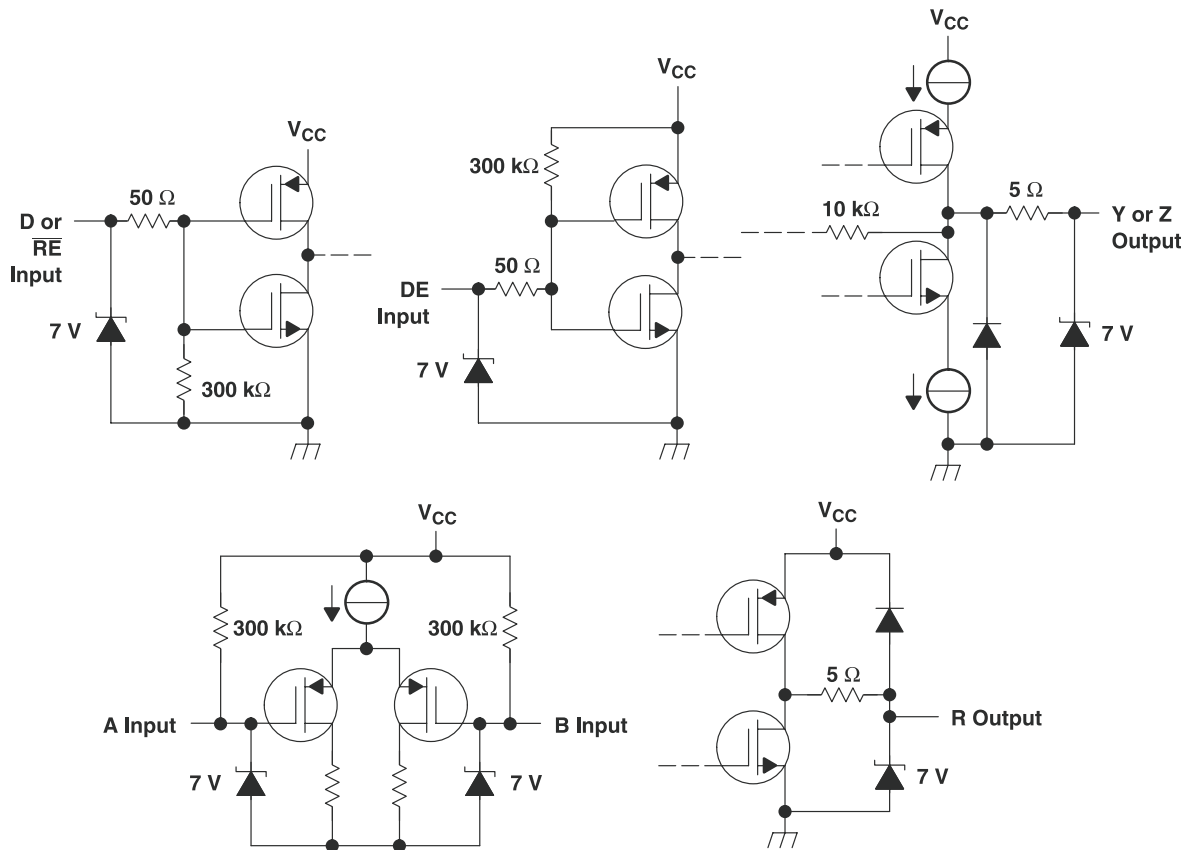
(1) H = high level, L = low level, Z = high impedance, X = don't care, ? = indeterminate

SN65LVDS180, SN65LVDS050, and SN65LVDS051 DRIVER⁽¹⁾

INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	OFF	OFF

(1) H = high level, L = low level, Z = high impedance, X = don't care, OFF = no output

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		UNIT
V _{CC}	Supply voltage range ⁽²⁾	–0.5 V to 4 V
Voltage range	D, R, DE, $\overline{RE}$	–0.5 V to 6 V
	Y, Z, A, and B	–0.5 V to 4 V
V _{OD}	Differential output voltage	1 V
Electrostatic discharge	Y, Z, A, B, and GND (see ⁽³⁾)	Class 3, A:12 kV, B:600 V
	All	Class 3, A:7 kV, B:500 V
Continuous power dissipation		See Dissipation Rating Table
Storage temperature range		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		250°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
- (3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C ⁽¹⁾	T _A = 85°C POWER RATING
PW(14)	736 mW	5.9 mW/°C	383 mW
PW(16)	839 mW	6.7 mW/°C	437 mW
D(8)	635 mW	5.1 mW/°C	330 mW/°C
D(14)	987 mW	7.9 mW/°C	513 mW/°C
D(16)	1110 mW	8.9 mW/°C	577 mW/°C

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no airflow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	3	3.3	3.6	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
V _{ID}	Magnitude of differential input voltage	0.1		0.6	V
V _{OD} (dis)	Magnitude of differential output voltage with disabled driver			520	mV
V _{OY} or V _{OZ}	Driver output voltage	0		2.4	V
V _{IC}	Common-mode input voltage (see Figure 5)	$\frac{ V_{ID} }{2}$	$2.4 - \frac{ V_{ID} }{2}$		V
				V _{CC} - 0.8	
T _A	Operating free-air temperature	–40		85	°C

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I_{CC}	Supply current	Driver and receiver enabled, no receiver load, driver $R_L = 100\ \Omega$		9	12	mA
		Driver enabled, receiver disabled, $R_L = 100\ \Omega$		5	7	
		Driver disabled, receiver enabled, no load		1.5	2	
		Disabled		0.5	1	
	SN65LVDS050	Drivers and receivers enabled, no receiver loads, driver $R_L = 100\ \Omega$		12	20	mA
		Drivers enabled, receivers disabled, $R_L = 100\ \Omega$		10	16	
		Drivers disabled, receivers enabled, no loads		3	6	
		Disabled		0.5	1	
	SN65LVDS051	Drivers enabled, No receiver loads, driver $R_L = 100\ \Omega$		12	20	mA
		Drivers disabled, no loads		3	6	

(1) All typical values are at 25°C and with a 3.3-V supply.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ V_{OD} $	Differential output voltage magnitude	$R_L = 100\ \Omega$, See Figure 3 and Figure 2	247	340	454	mV
$\Delta V_{OD} $	Change in differential output voltage magnitude between logic states		-50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{IH}	High-level input current	DE	$V_{IH} = 5\ V$	-0.5	-20	μA
		D		2	20	
I_{IL}	Low-level input current	DE	$V_{IL} = 0.8\ V$	-0.5	-10	μA
		D		2	10	
I_{OS}	Short-circuit output current	V_{OY} or $V_{OZ} = 0\ V$		3	10	mA
		$V_{OD} = 0\ V$		3	10	
$I_{O(OFF)}$	Off-state output current	DE = OV $V_{OY} = V_{OZ} = OV$	-1		1	μA
		DE = V_{CC} $V_{OY} = V_{OZ} = OV$, $V_{CC} < 1.5\ V$				
C_{IN}	Input capacitance			3		pF

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going differential input voltage threshold	See Figure 5 and			50	mV
V _{IT-}	Negative-going differential input voltage threshold		-50			
V _{OH}	High-level output voltage	I _{OH} = -8 mA	2.4			V
		I _{OH} = -4 mA	2.8			
V _{OL}	Low-level output voltage	I _{OL} = 8 mA			0.4	V
I _I	Input current (A or B inputs)	V _I = 0	-2	-11	-20	μA
		V _I = 2.4 V	-1.2	-3		
I _{I(OFF)}	Power-off input current (A or B inputs)	V _{CC} = 0			±20	μA
I _{IH}	High-level input current (enables)	V _{IH} = 5 V			±10	μA
I _{IL}	Low-level input current (enables)	V _{IL} = 0.8 V			±10	μA
I _{OZ}	High-impedance output current	V _O = 0 or 5 V			±10	μA
C _I	Input capacitance			5		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	R _L = 100 Ω, C _L = 10 pF, See Figure 2		1.7	2.7	ns
t _{PHL}	Propagation delay time, high-to-low-level output			1.7	2.7	ns
t _r	Differential output signal rise time			0.8	1	ns
t _f	Differential output signal fall time			0.8	1	ns
t _{sk(p)}	Pulse skew (t _{pHL} - t _{pLH}) ⁽²⁾			300		ps
t _{sk(o)}	Channel-to-channel output skew ⁽³⁾			150		ps
t _{en}	Enable time	See Figure 4		4.3	10	ns
t _{dis}	Disable time			3.1	10	ns

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) t_{sk(p)} is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

(3) t_{sk(o)} is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	C _L = 10 pF, See Figure 6		3.7	4.5	ns
t _{PHL}	Propagation delay time, high-to-low-level output			3.7	4.5	ns
t _{sk(p)}	Pulse skew (t _{pHL} - t _{pLH}) ⁽²⁾			0.3		ns
t _r	Output signal rise time			0.7	1.5	ns
t _f	Output signal fall time			0.9	1.5	ns
t _{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 7		2.5		ns
t _{PZL}	Propagation delay time, high-impedance-to-low-level output			2.5		ns
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output			7		ns
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			4		ns

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) t_{sk(p)} is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

PARAMETER MEASUREMENT INFORMATION

DRIVER

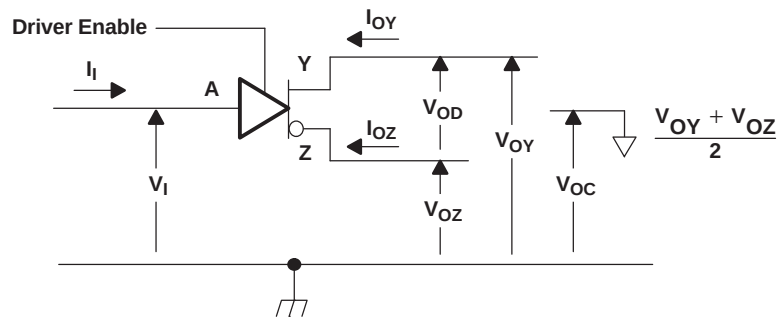
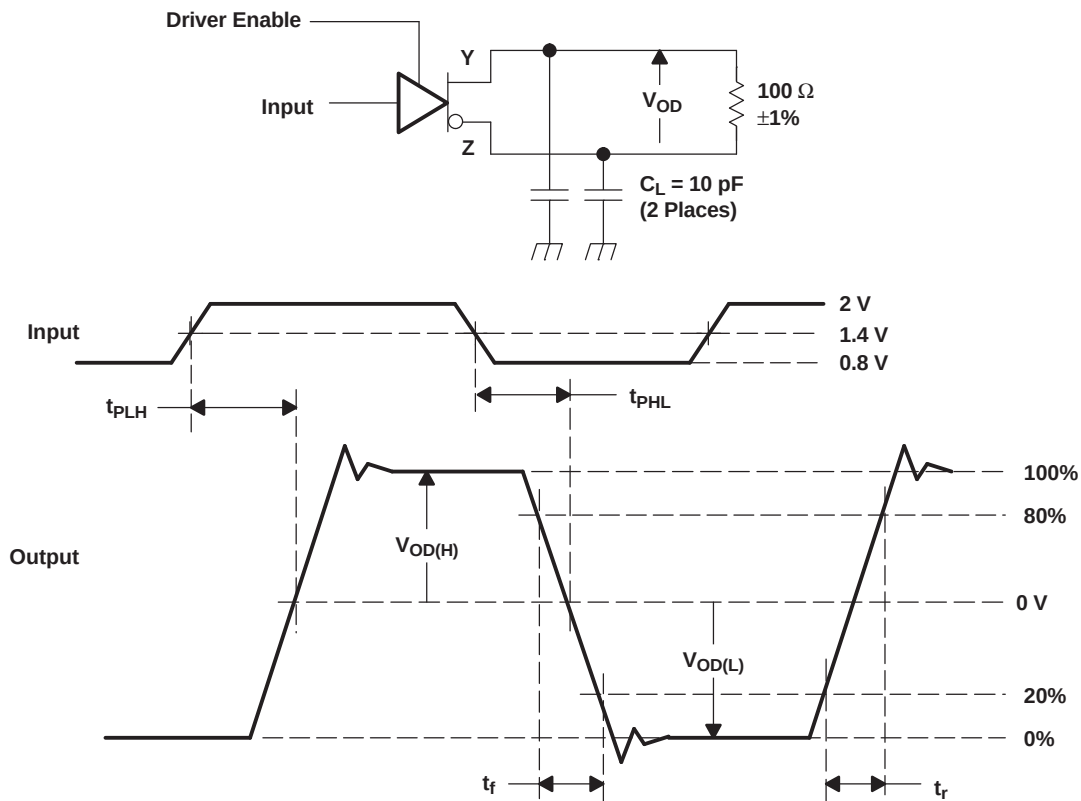


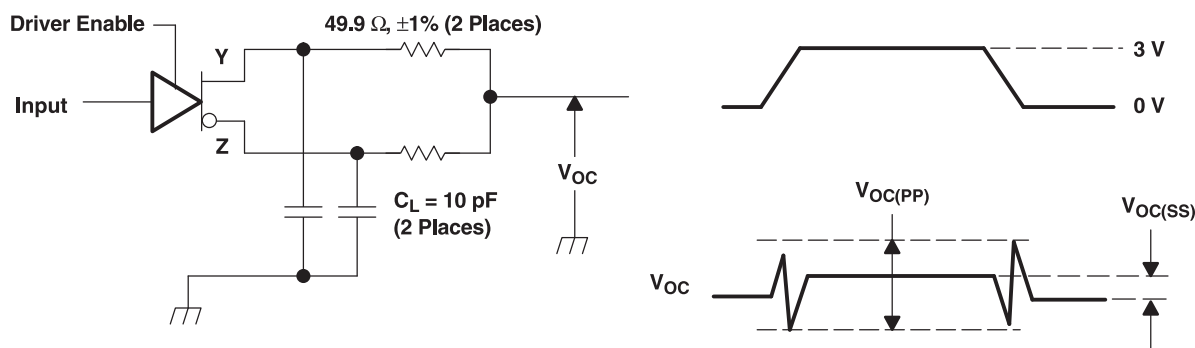
Figure 1. Driver Voltage and Current Definitions



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

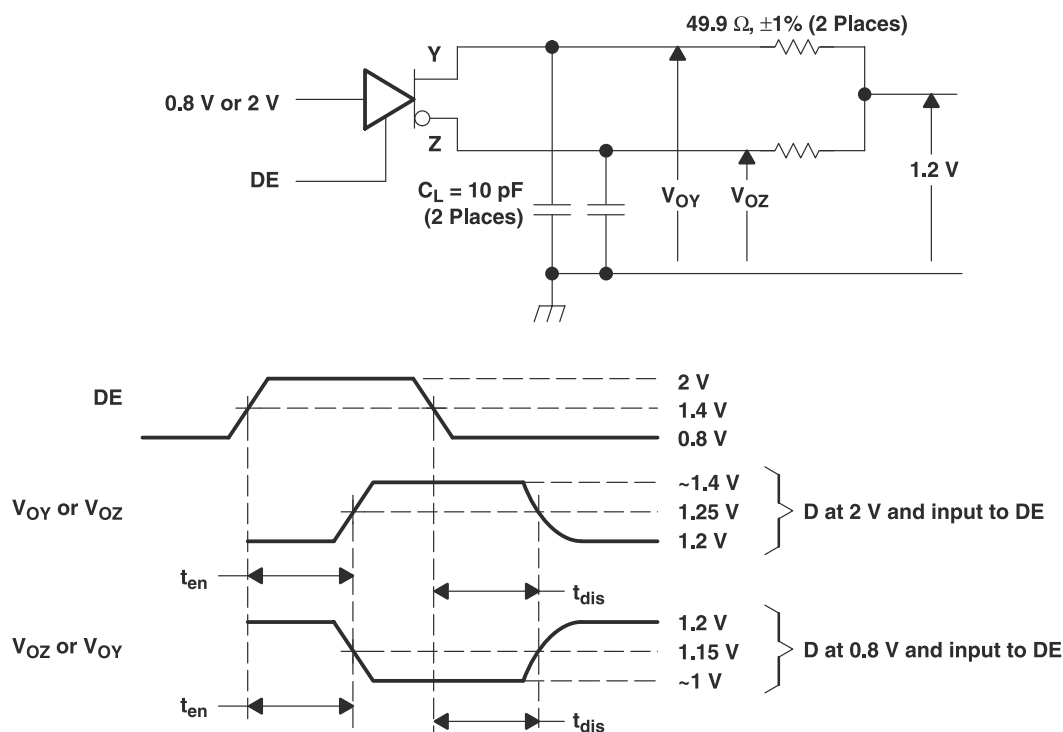
Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3-dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

RECEIVER

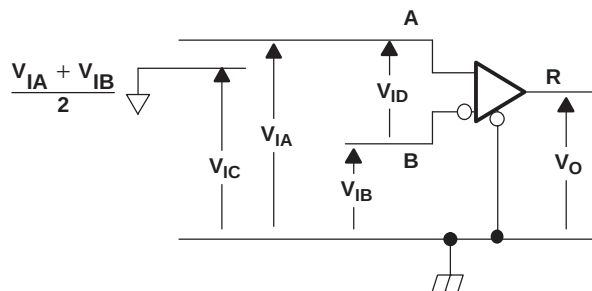
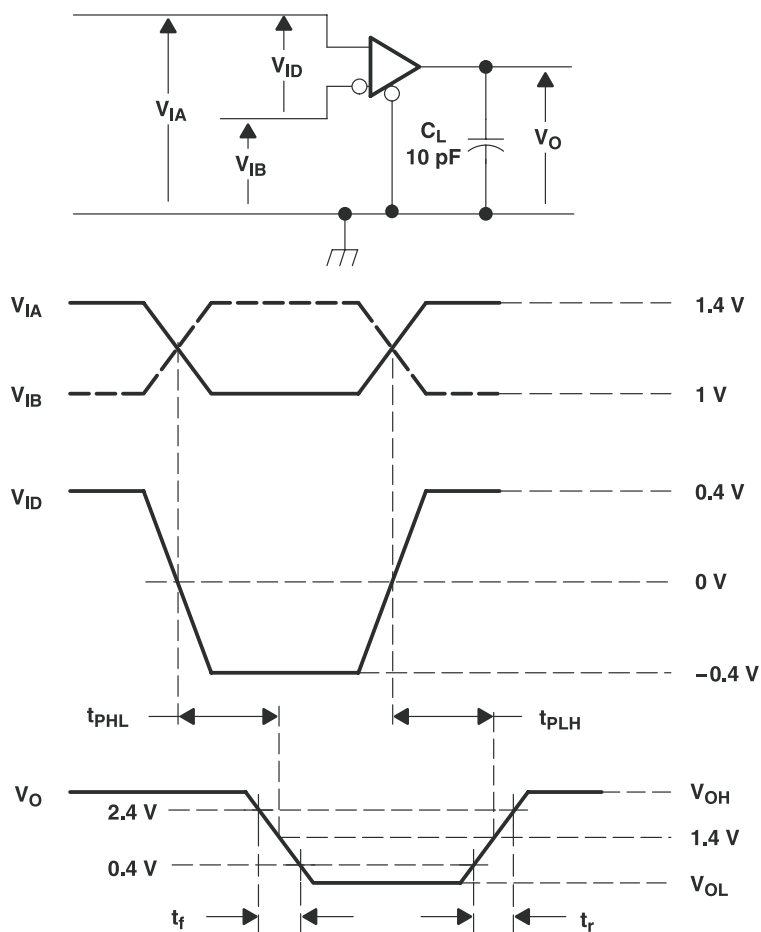


Figure 5. Receiver Voltage Definitions

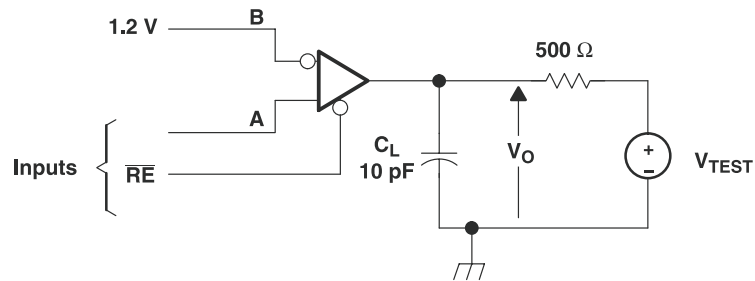
Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	-100	1.2
2.4	2.3	100	2.35
2.3	2.4	-100	2.35
0.1	0	100	0.05
0	0.1	-100	0.05
1.5	0.9	600	1.2
0.9	1.5	-600	1.2
2.4	1.8	600	2.1
1.8	2.4	-600	2.1
0.6	0	600	0.3
0	0.6	-600	0.3



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, pulse repetition rate (PRR) = 50 Mpps, pulse width = $10 \pm 0.2 \text{ ns}$. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.

Figure 6. Timing Test Circuit and Waveforms



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

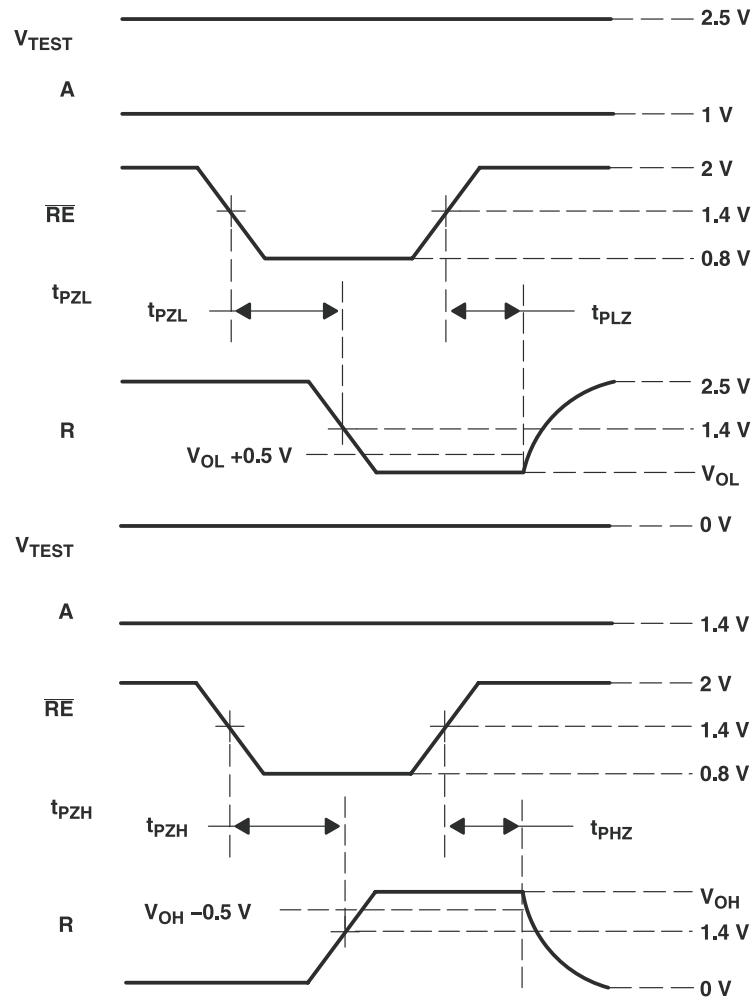


Figure 7. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

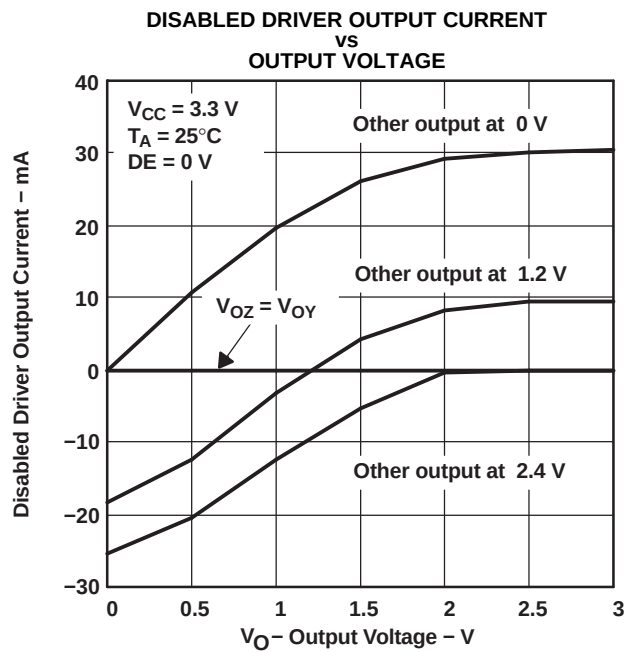


Figure 8.

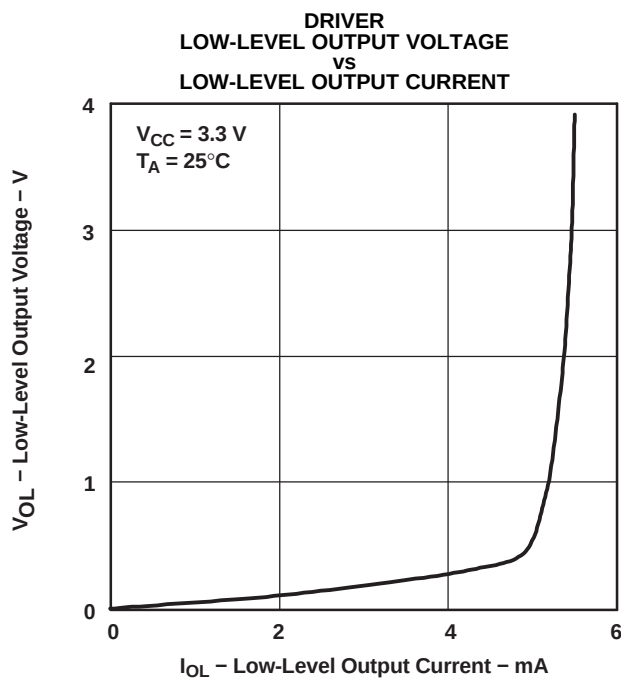


Figure 9.

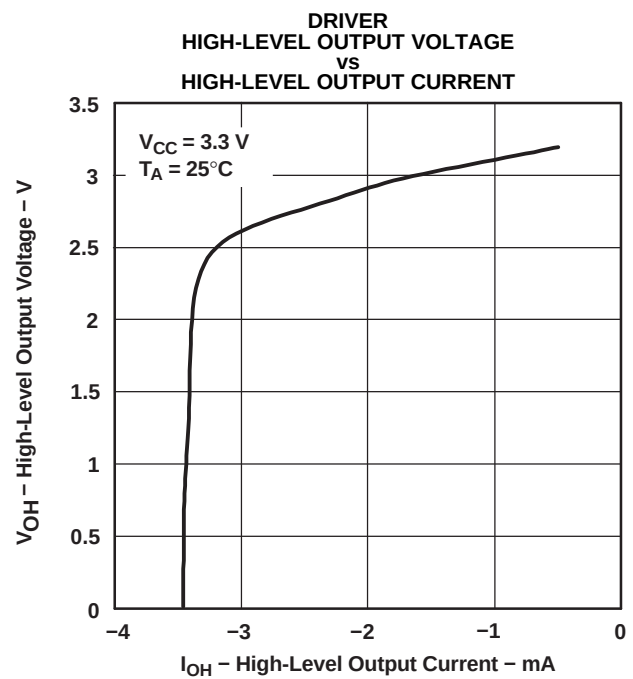


Figure 10.

TYPICAL CHARACTERISTICS (continued)

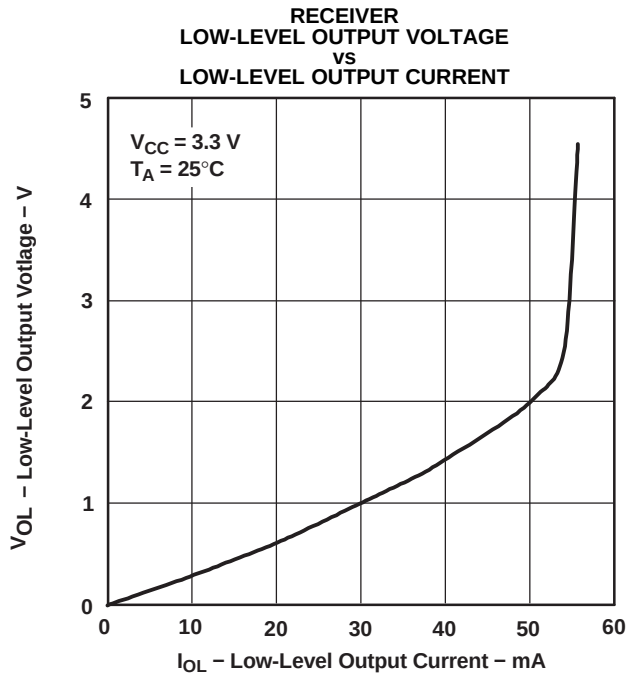


Figure 11.

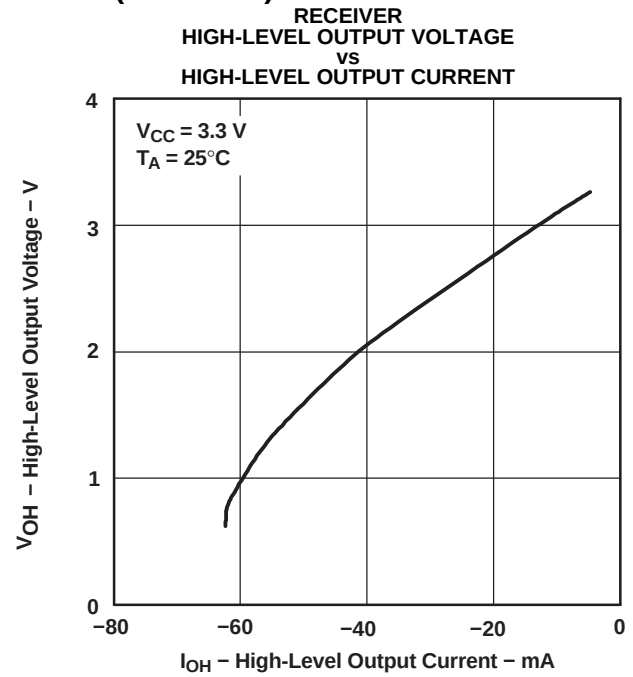


Figure 12.

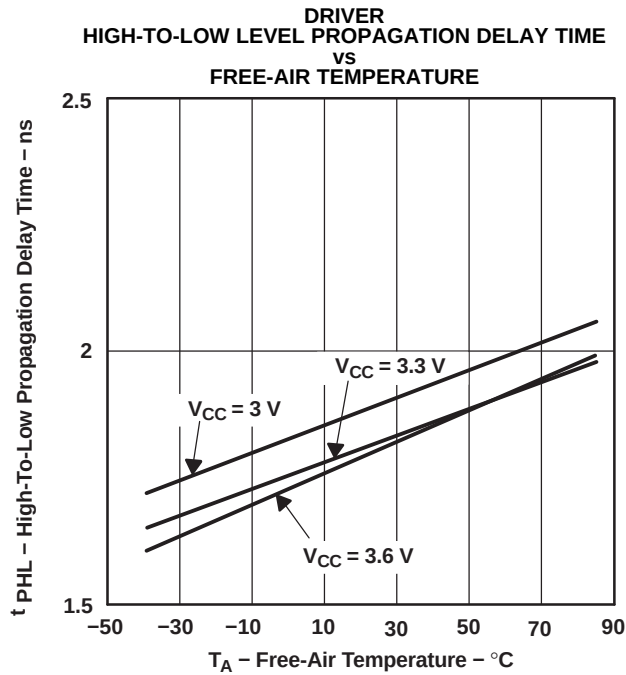


Figure 13.

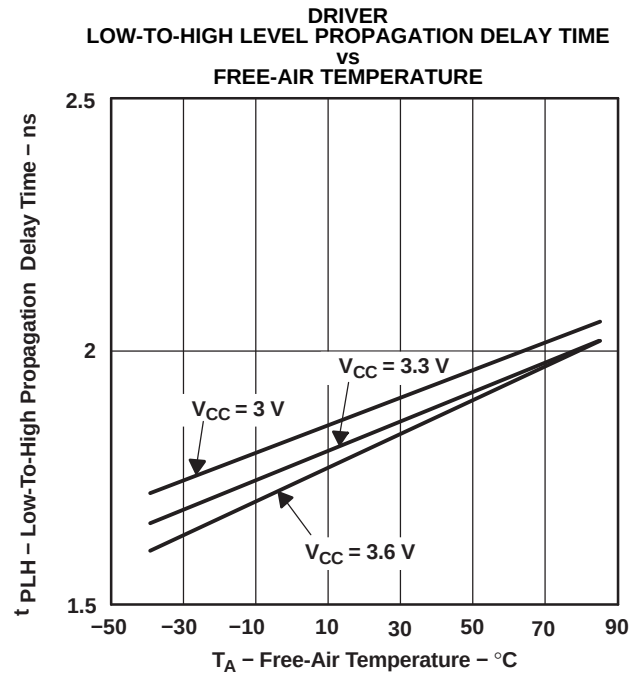


Figure 14.

TYPICAL CHARACTERISTICS (continued)

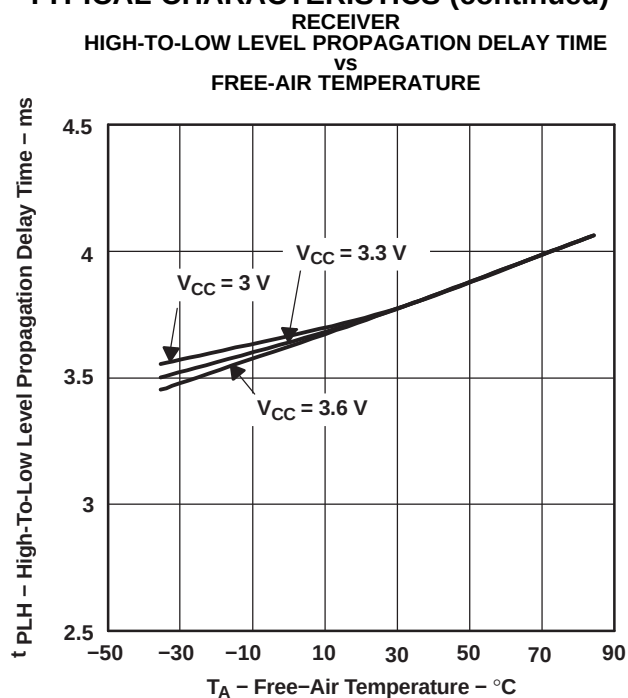


Figure 15.

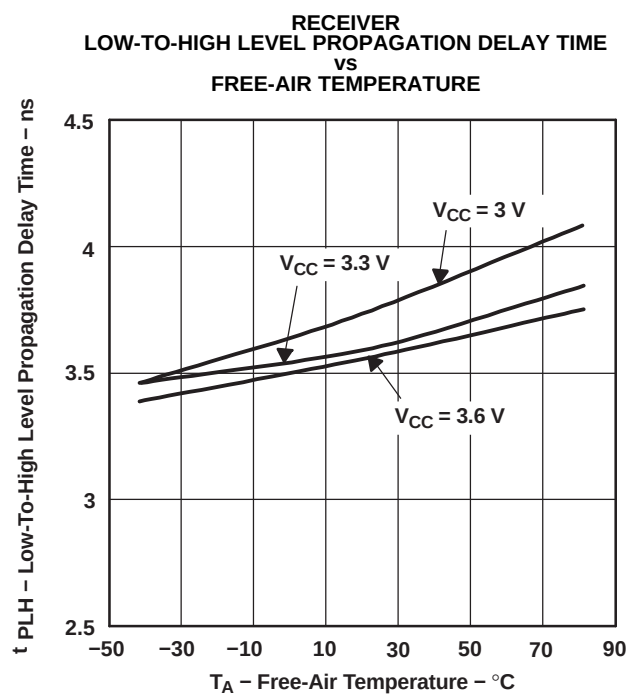


Figure 16.

APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common-mode output and balanced interface for low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers maintain ECL speeds without the power and dual supply requirements.

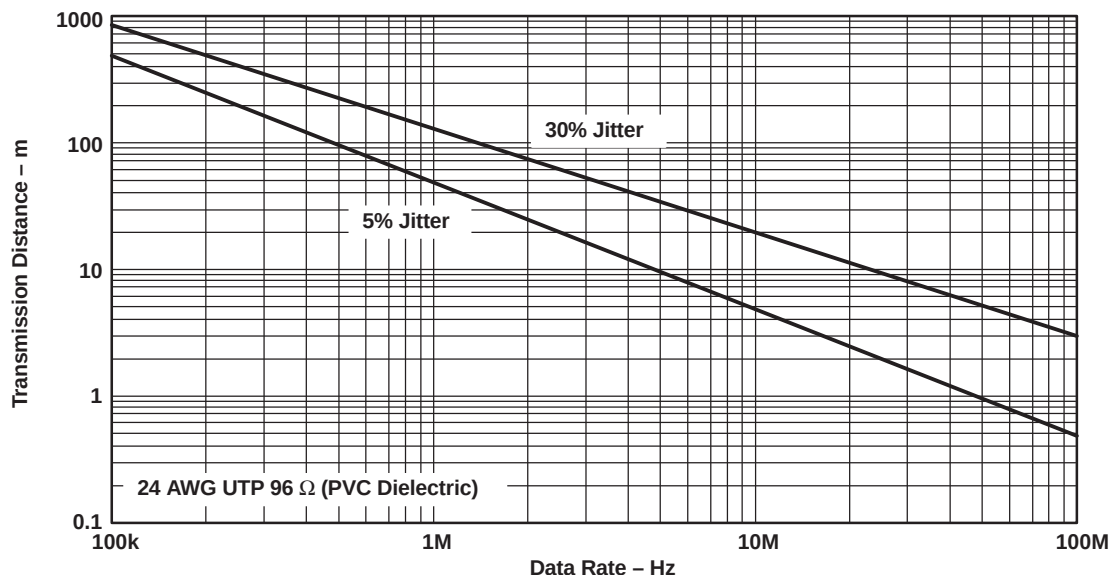


Figure 17. Data Transmission Distance Versus Rate

FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between -100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through 300-k Ω resistors as shown in Figure 11. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to $V_{CC} - 0.4$ V to detect this condition and force the output to a high-level regardless of the differential input voltage.

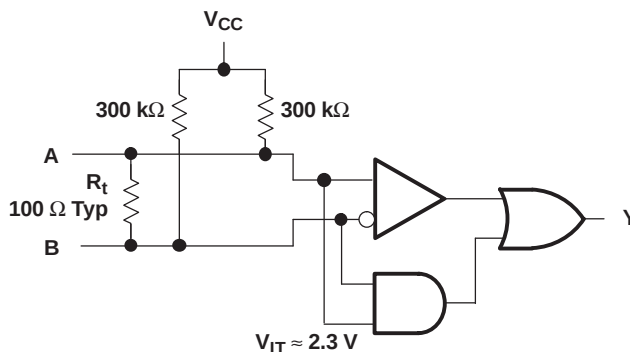


Figure 18. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, R_t , does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

REVISION HISTORY

Changes from Original (September 2003) to Revision A Page

- Deleted Feature: "Qualification in Accordance With AEC-Q100†" [1](#)
 - Deleted Feature: "Customer-Specific Configuration Control..." [1](#)
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Changes from Revision A (April 2008) to Revision B Page

- Changed device number From: SN65LVDS050PWRQ1 To: SN65LVDS050IPWRQ1. Changed the device status to Production [2](#)
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Changes from Revision B (November 2011) to Revision C Page

- Deleted device SN65LVDS179-Q1 [1](#)
-

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65LVDS050IPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VDS050Q	Samples
SN65LVDS051DRG4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VDS051Q	Samples
SN65LVDS051DRQ1	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	VDS051Q	
SN65LVDS051PWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VDS051Q	Samples
SN65LVDS051PWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VDS051Q	Samples
SN65LVDS180DRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VDS180Q	Samples
SN65LVDS180DRQ1	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	VDS180Q	
SN65LVDS180PWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VDS180Q	Samples
SN65LVDS180PWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VDS180Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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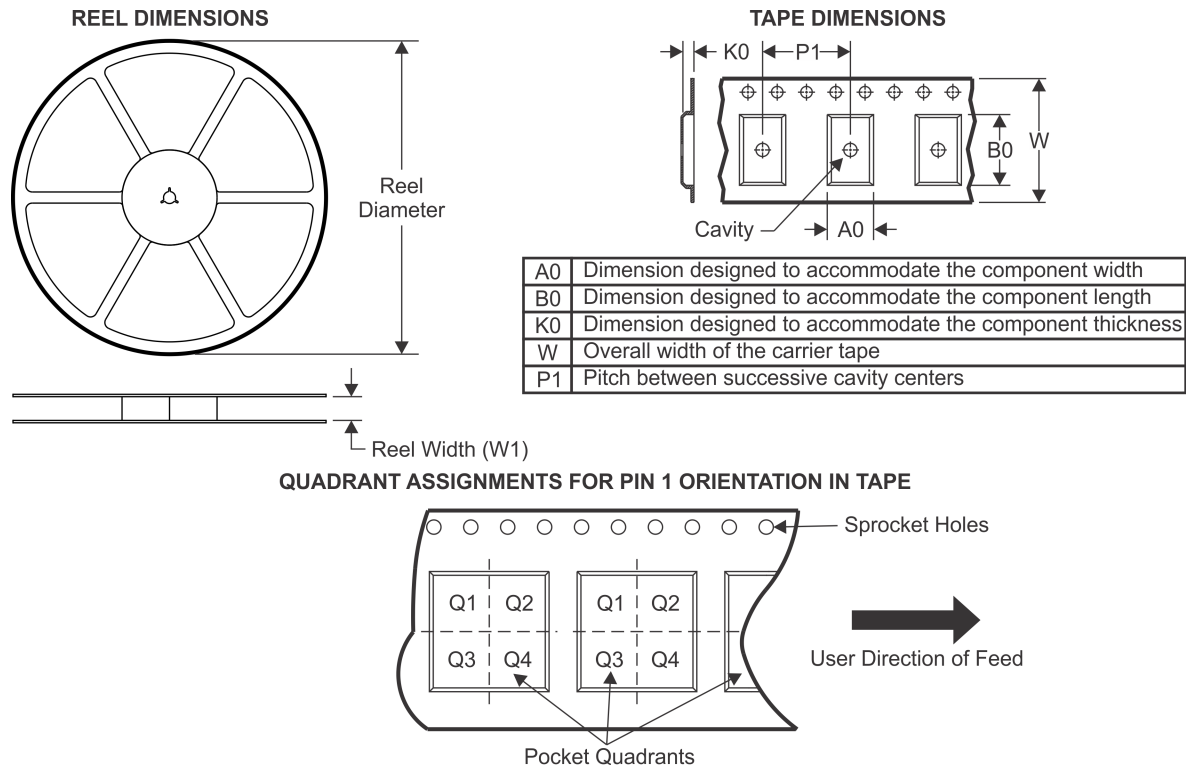
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LVDS050-Q1, SN65LVDS051-Q1, SN65LVDS180-Q1 :

- Catalog: [SN65LVDS050](#), [SN65LVDS051](#), [SN65LVDS180](#)

NOTE: Qualified Version Definitions:

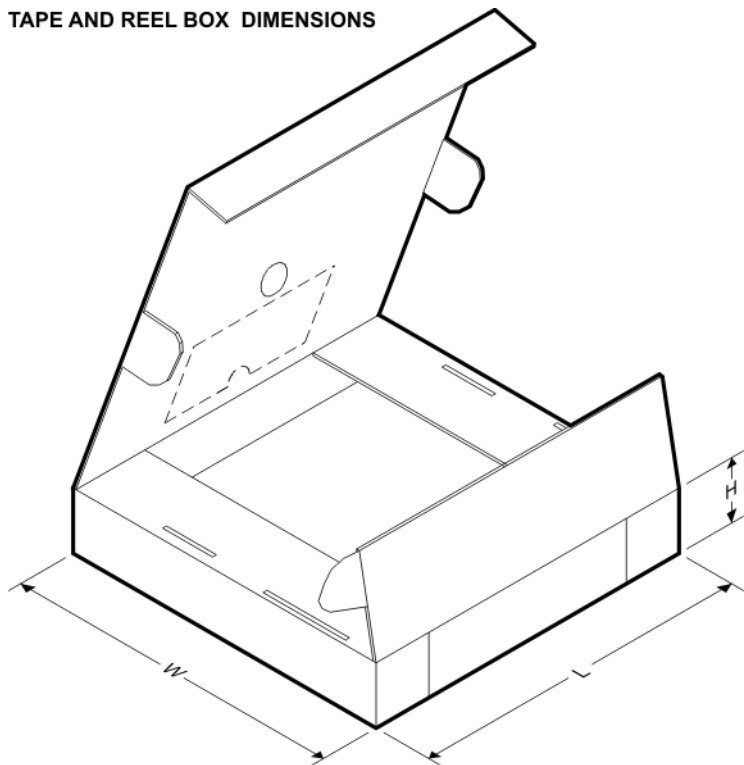
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS051PWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS051PWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS180PWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS180PWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

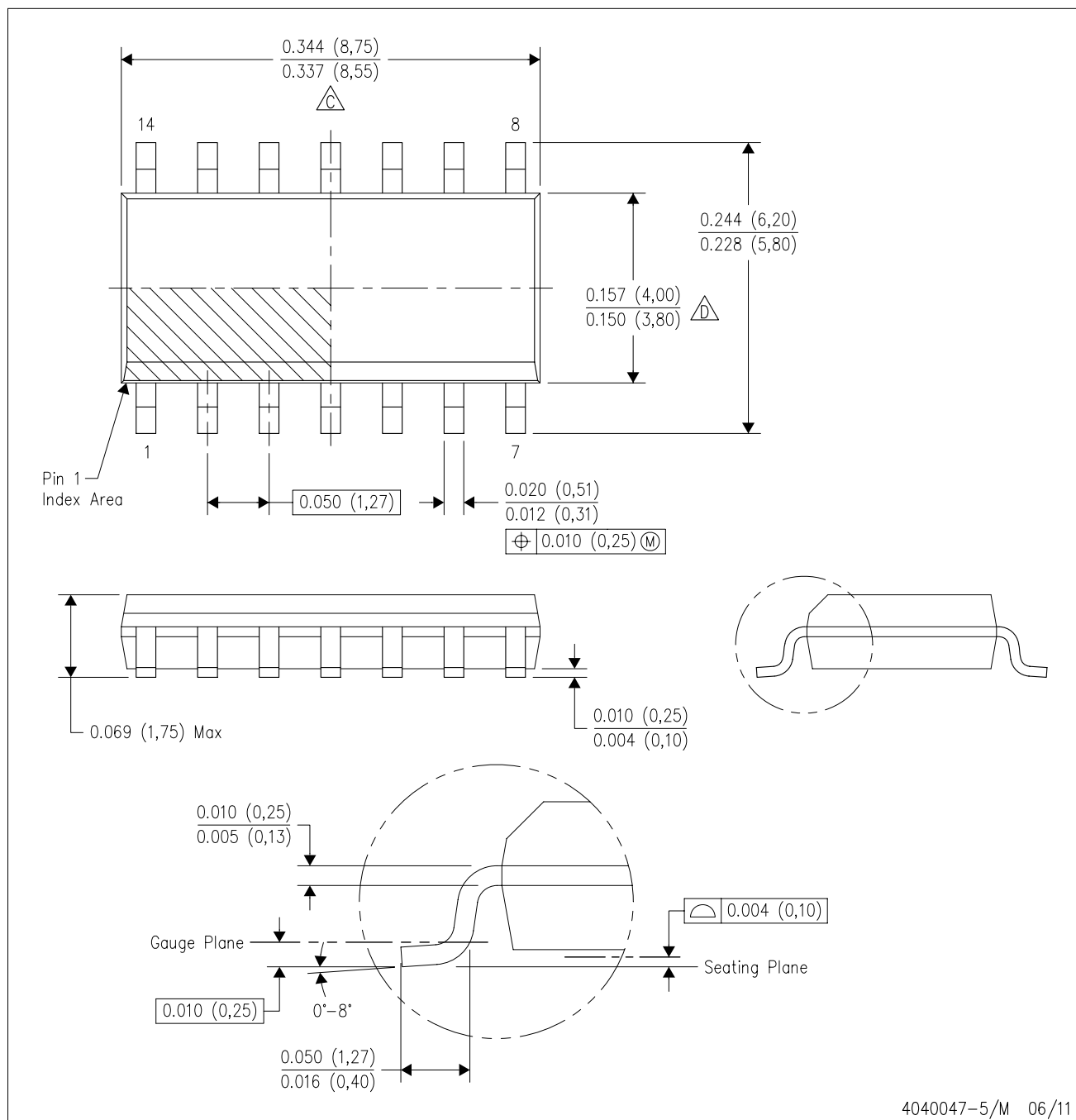


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS051PWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65LVDS051PWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65LVDS180PWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
SN65LVDS180PWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



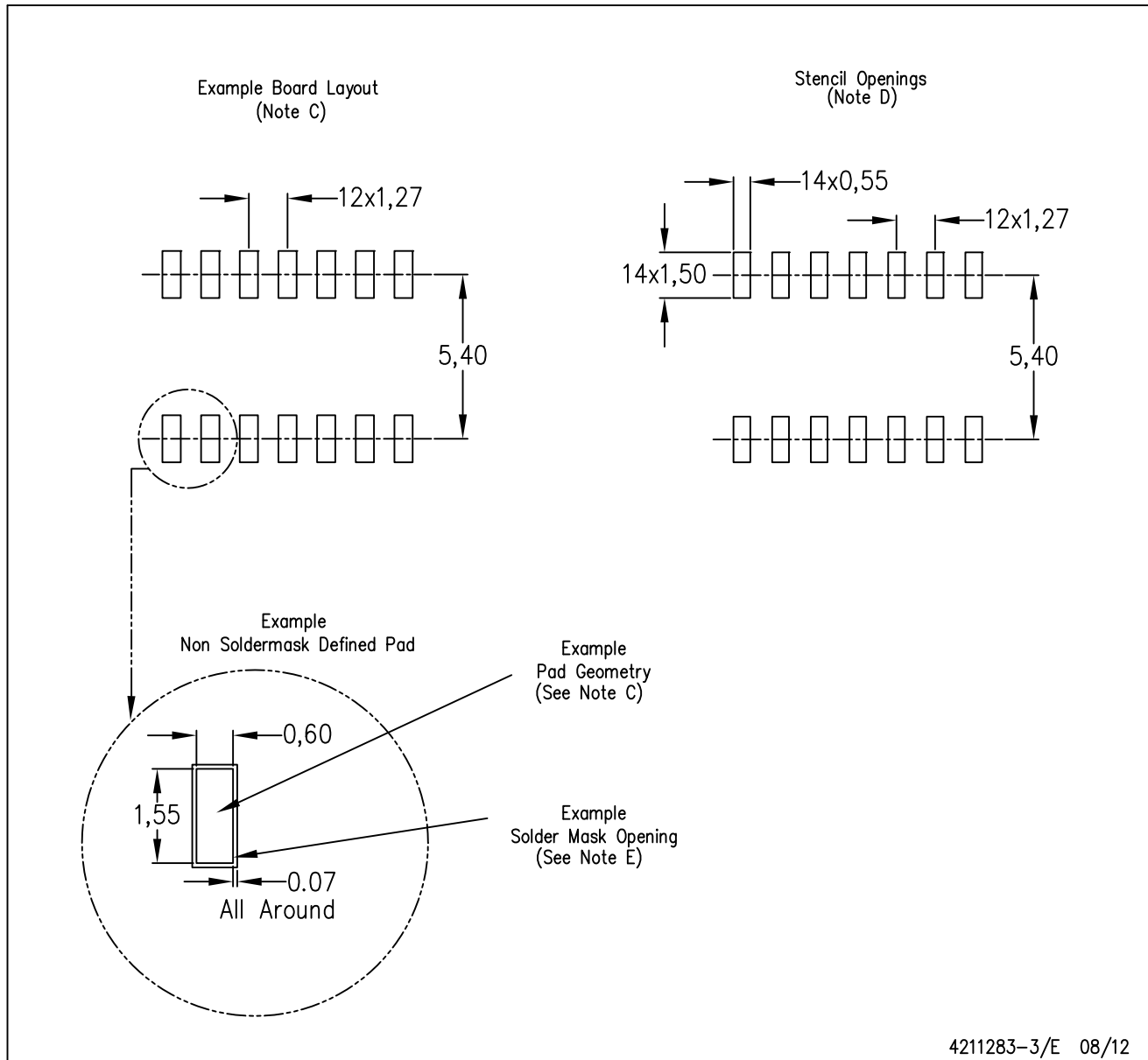
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

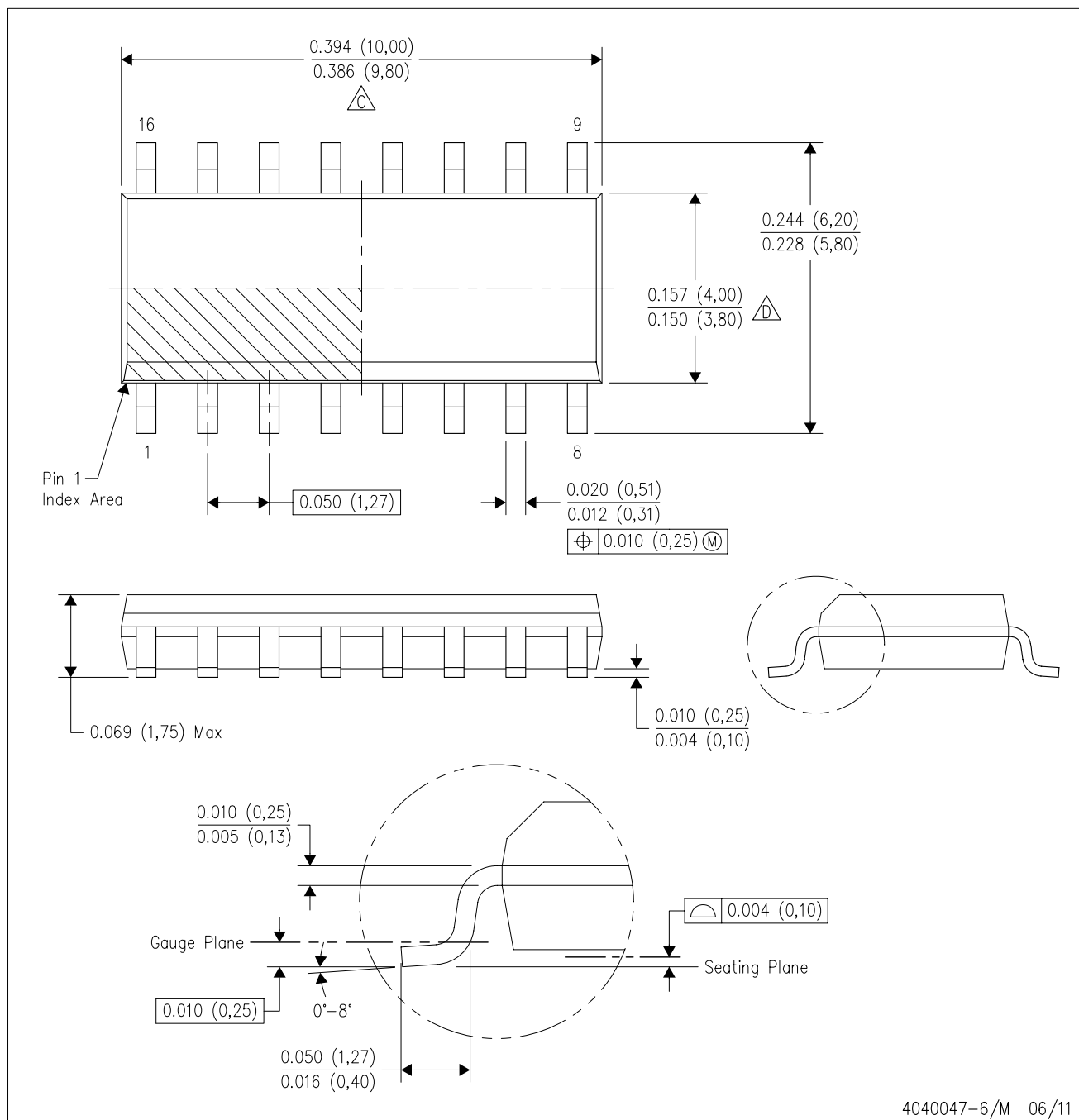
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G16)

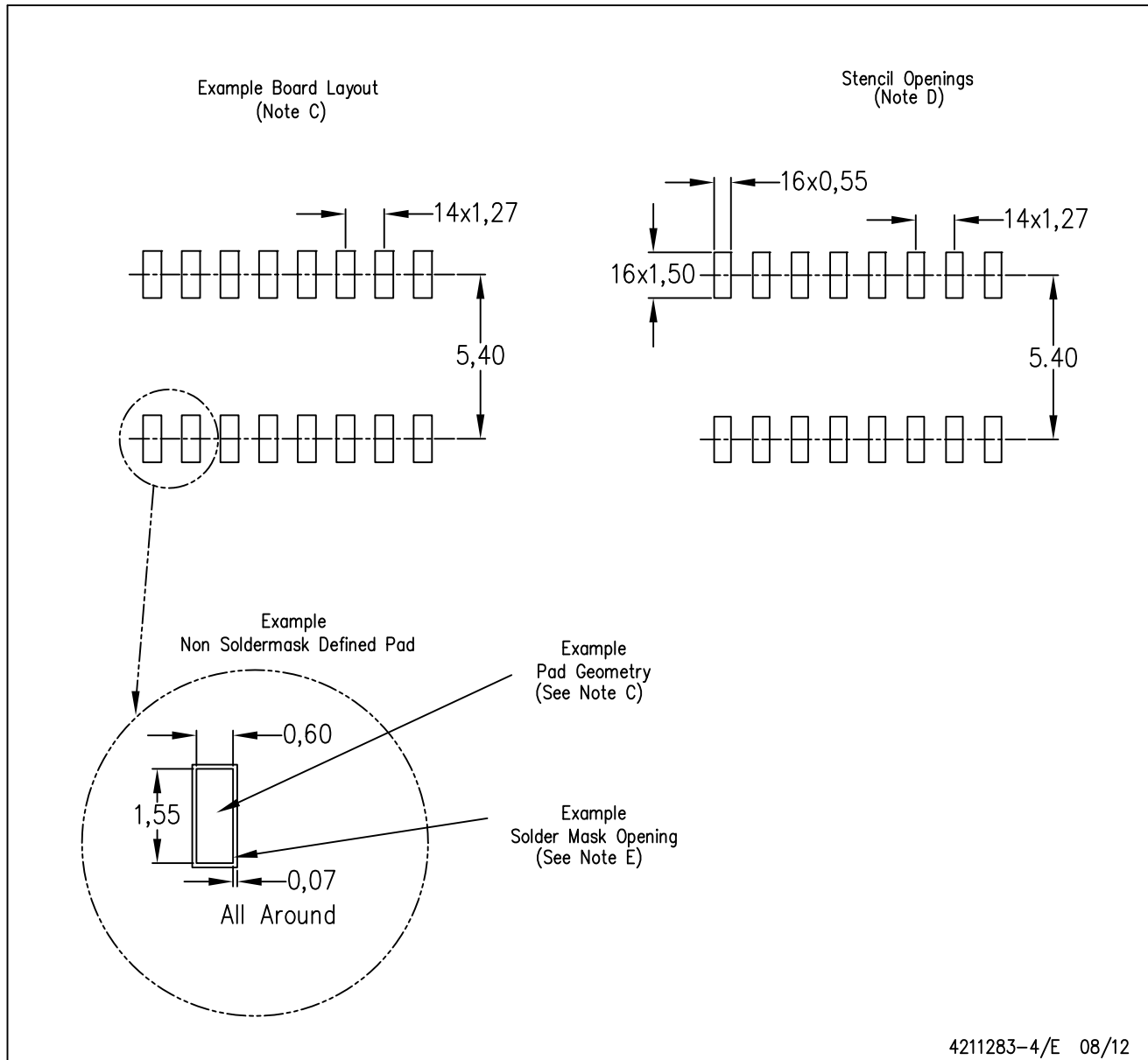
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

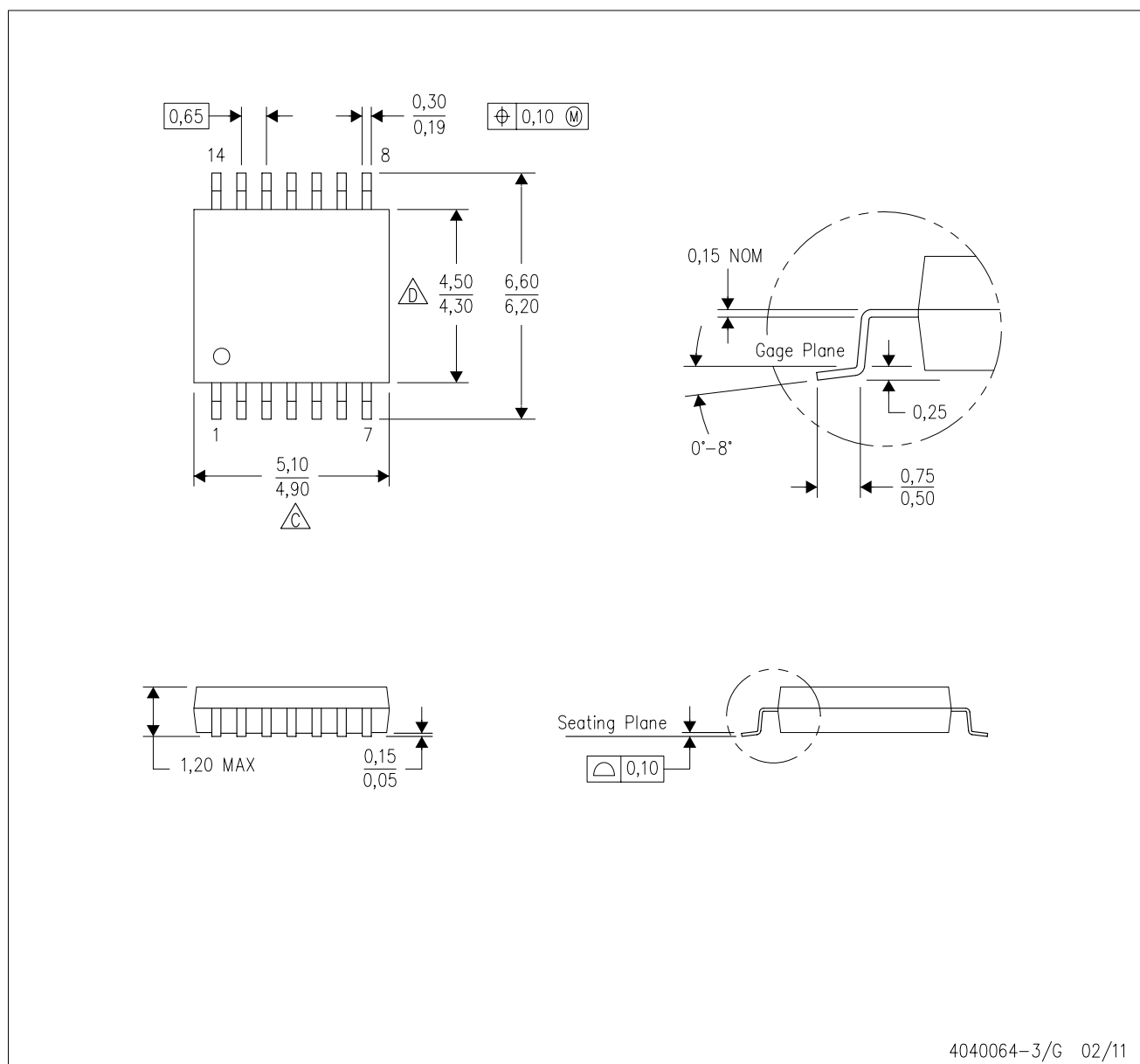
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

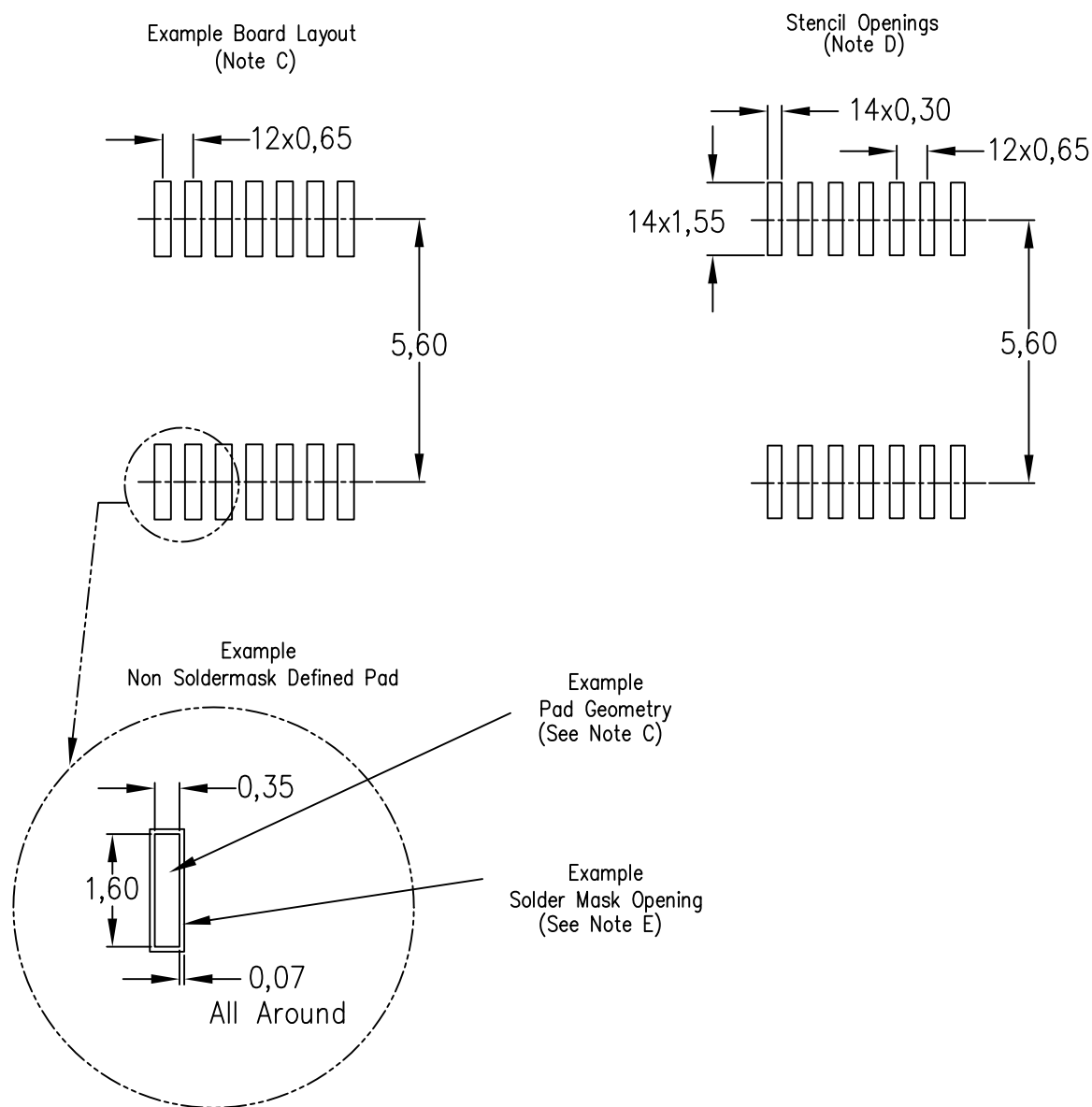


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

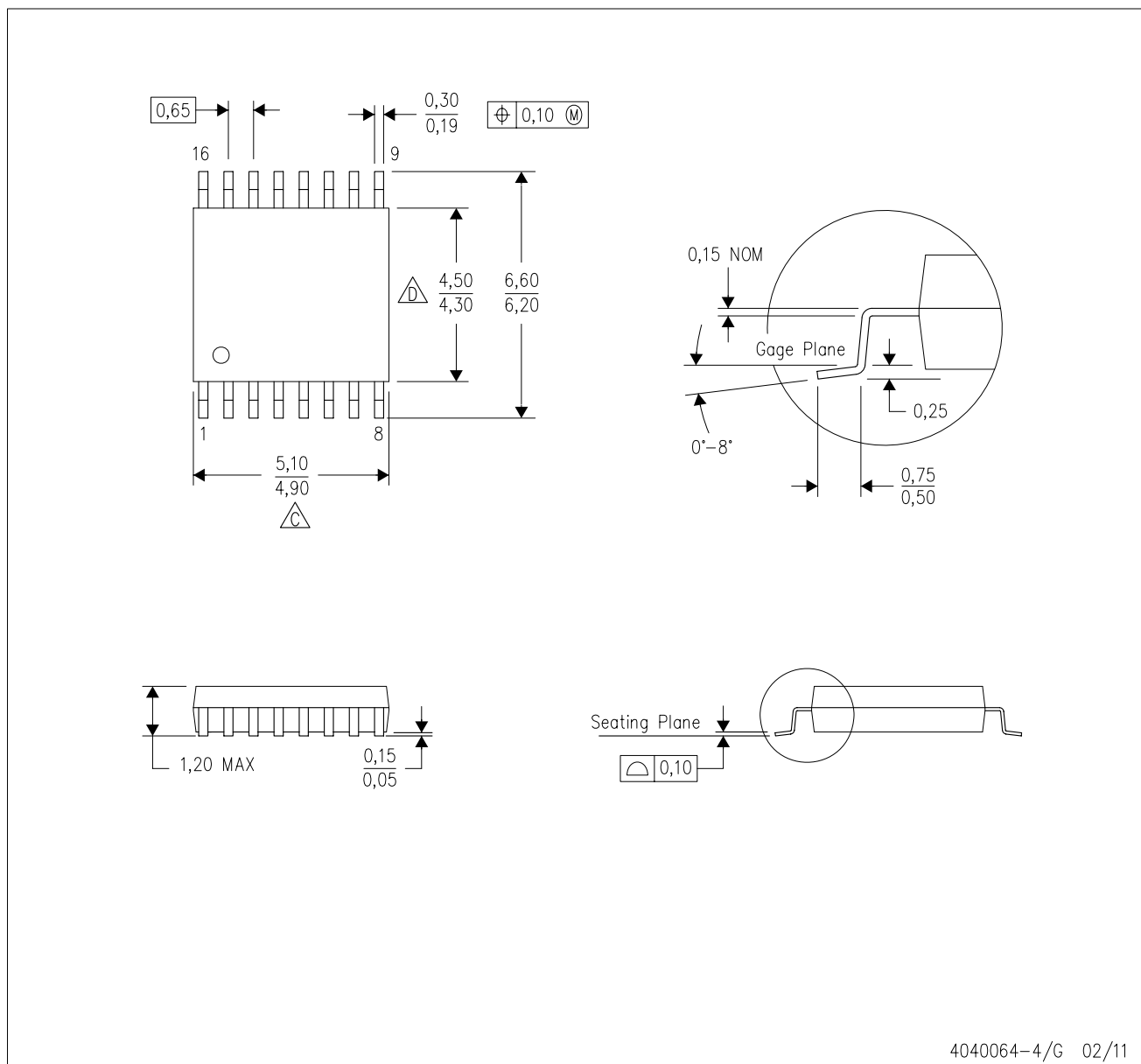


4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

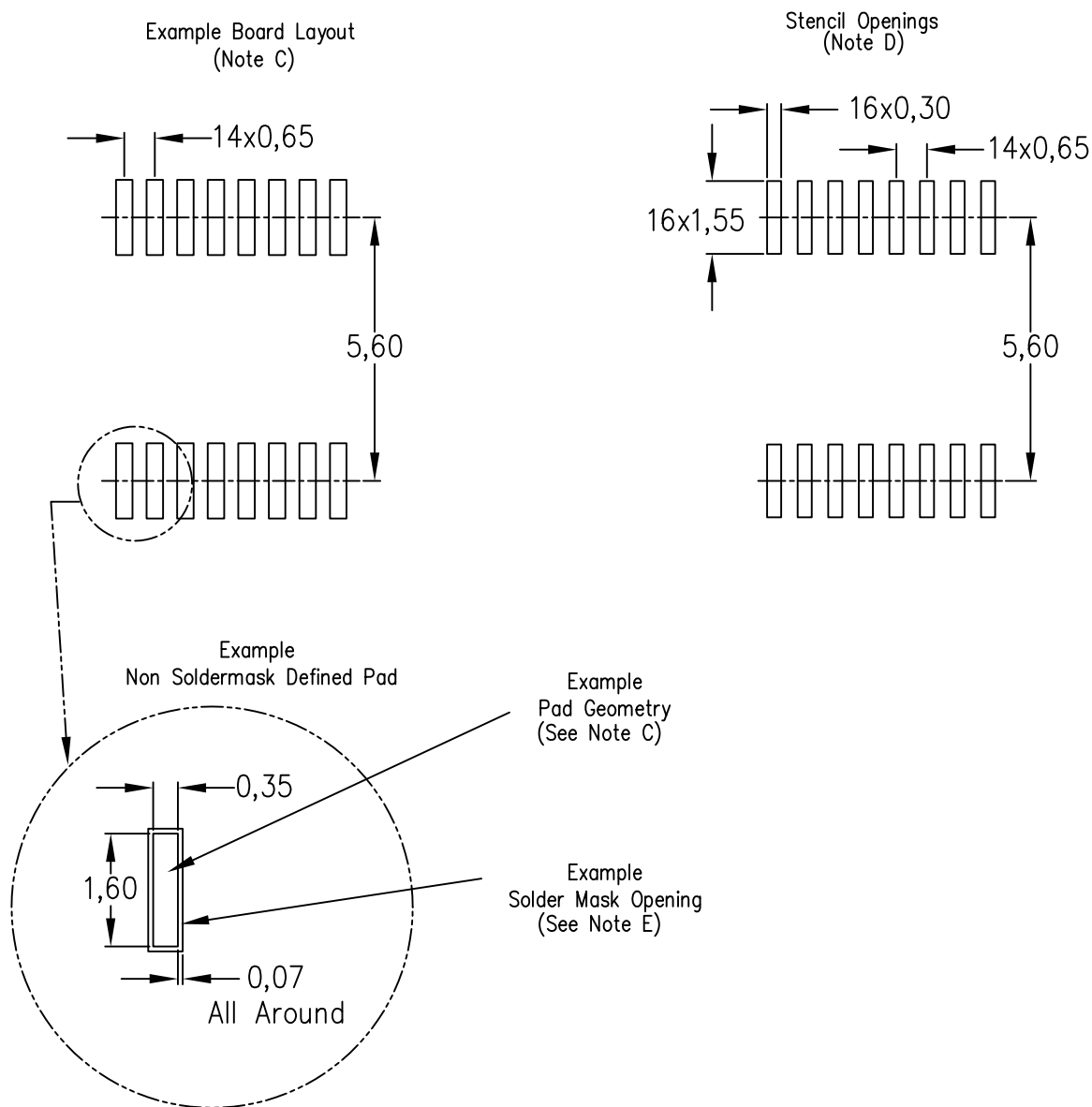
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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