

Operational Amplifiers

Low Supply Current Input/Output Full Swing Operational Amplifier

BD12730G BD12732xxx BD12734xxx

General Description

BD12730G/BD12732xxx/BD12734xxx are input/output full swing operational amplifiers. They have the features of low operating supply voltage, low supply current, low input referred noise voltage and high phase margin. These are suitable for audio applications and battery management.

Features

- Low Operating Supply Voltage
- Input/Output Full Swing
- Low Supply Current
- High Phase Margin
- Low Input Referred Noise Voltage

Applications

- Audio Application
- Battery Management
- General Purpose

Key Specifications

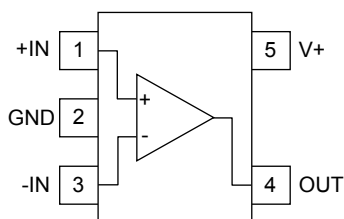
- Operating Supply Voltage (Single Supply): +1.8V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Input Offset Voltage: 5mV (Max)
- Supply Current:
 - BD12730G(Single) 550μA (Max)
 - BD12732xxx(Dual) 900μA (Max)
 - BD12734xxx(Quad) 1800μA (Max)
- Input Referred Noise Voltage: 10 nV/√Hz (Typ)
- Adequate Phase Margin: 75°(Typ)

Packages

	W(Typ) x D(Typ) x H(Max)
SSOP5	2.90mm x 2.80mm x 1.25mm
SOP8	5.00mm x 6.20mm x 1.71mm
SOP-J8	4.90mm x 6.00mm x 1.65mm
SSOP-B8	3.00mm x 6.40mm x 1.35mm
TSSOP-B8	3.00mm x 6.40mm x 1.20mm
MSOP8	2.90mm x 4.00mm x 0.90mm
TSSOP-B8J	3.00mm x 4.90mm x 1.10mm
SOP14	8.70mm x 6.20mm x 1.71mm
SOP-J14	8.65mm x 6.00mm x 1.65mm
SSOP-B14	5.00mm x 6.40mm x 1.35mm
TSSOP-B14J	5.00mm x 6.40mm x 1.20mm

Pin Configuration

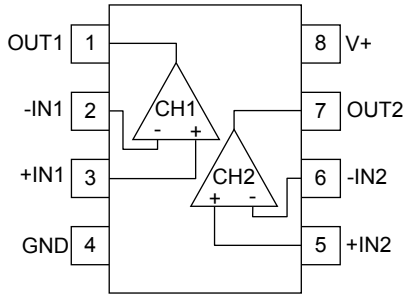
BD12730G : SSOP5



Pin No.	Pin Name
1	+IN
2	GND
3	-IN
4	OUT
5	V+

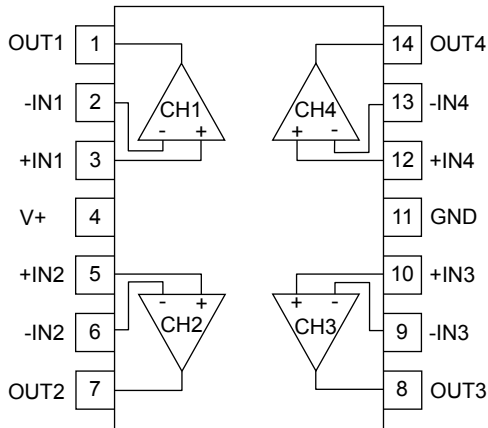
○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

BD12732F : SOP8
BD12732FJ : SOP-J8
BD12732FV : SSOP-B8
BD12732FVT : TSSOP-B8
BD12732FVM : MSOP8
BD12732FVJ : TSSOP-B8J



Pin No.	Pin Name
1	OUT1
2	-IN1
3	+IN1
4	GND
5	+IN2
6	-IN2
7	OUT2
8	V+

BD12734F : SOP14
BD12734FJ : SOP-J14
BD12734FV : SSOP-B14
BD12734FVJ : TSSOP-B14J



Pin No.	Pin Name
1	OUT1
2	-IN1
3	+IN1
4	V+
5	+IN2
6	-IN2
7	OUT2
8	OUT3
9	-IN3
10	+IN3
11	GND
12	+IN4
13	-IN4
14	OUT4

Ordering Information

B	D	1	2	7	3	x	x	x	x
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-	x	x
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Part Number	Package
BD12730G	G : SSOP5
BD12732xxx	F : SOP8
BD12734xxx	FJ : SOP-J8
	FV : SSOP-B8
	FVT : TSSOP-B8
	FVM : MSOP8
	FVJ : TSSOP-B8J
	F : SOP14
	FJ : SOP-J14
	FV : SSOP-B14
	FVJ : TSSOP-B14J

Packaging and Forming Specification
TR: Embossed tape and reel (SSOP5/MSOP8)
E2: Embossed tape and reel (SOP8/SOP-J8/SSOP-B8/TSSOP-B8/ TSSOP-B8J/SOP14/SOP-J14/SSOP-B14/ TSSOP-B14J)

Line-up

Operating Temperature	Channels	Package		Orderable Part Number
-40°C to +85°C	1ch	SSOP5	Reel of 3000	BD12730G-TR
	2ch	SOP8	Reel of 2500	BD12732F-E2
		SOP-J8	Reel of 2500	BD12732FJ-E2
		SSOP-B8	Reel of 2500	BD12732FV-E2
		TSSOP-B8	Reel of 3000	BD12732FVT-E2
		MSOP8	Reel of 3000	BD12732FVM-TR
		TSSOP-B8J	Reel of 2500	BD12732FVJ-E2
	4ch	SOP14	Reel of 2500	BD12734F-E2
		SOP-J14	Reel of 2500	BD12734FJ-E2
		SSOP-B14	Reel of 2500	BD12734FV-E2
		TSSOP-B14J	Reel of 2500	BD12734FVJ-E2

Absolute Maximum Ratings (T_A=25°C)

Parameter	Symbol	Rating			Unit
		BD12730G	BD12732xxx	BD12734xxx	
Supply Voltage	V+	+7.0			V
Power Dissipation	P _D	SSOP5	0.67 (Note 1,9)	-	W
		SOP8	-	0.68 (Note 2,9)	
		SOP-J8	-	0.67 (Note 1,9)	
		SSOP-B8	-	0.62 (Note 3,9)	
		TSSOP-B8	-	0.62 (Note 3,9)	
		MSOP8	-	0.58 (Note 4,9)	
		TSSOP-B8J	-	0.58 (Note 4,9)	
		SOP14	-	-	0.56 (Note 5,9)
		SOP-J14	-	-	1.02 (Note 6,9)
		SSOP-B14	-	-	0.87 (Note 7,9)
		TSSOP-B14J	-	-	0.85 (Note 8,9)
Differential Input Voltage (Note 10)	V _{ID}	±3.0			V
Input Common-mode Voltage Range	V _{ICM}	GND to V+			V
Input Current (Note 11)	I _I	±10			mA
Operating Supply Voltage	V _{opr}	+1.8 to +5.5			V
Operating Temperature	T _{opr}	- 40 to +85			°C
Storage Temperature	T _{stg}	- 55 to +150			°C
Maximum Junction Temperature	T _{Jmax}	+150			°C

(Note 1) To use at temperature above T_A=25°C, reduce by 5.4mW/°C.(Note 2) To use at temperature above T_A=25°C, reduce by 5.5mW/°C.(Note 3) To use at temperature above T_A=25°C, reduce by 5.0mW/°C.(Note 4) To use at temperature above T_A=25°C, reduce by 4.7mW/°C.(Note 5) To use at temperature above T_A=25°C, reduce by 4.5mW/°C.(Note 6) To use at temperature above T_A=25°C, reduce by 8.2mW/°C.(Note 7) To use at temperature above T_A=25°C, reduce by 7.0mW/°C.(Note 8) To use at temperature above T_A=25°C, reduce by 6.8mW/°C.

(Note 9) Mounted on a FR4 glass epoxy PCB 70mm×70mm×1.6mm (Copper foil area less than 3%).

(Note 10) Differential Input Voltage is the voltage difference between the inverting and non-inverting inputs.

The input pin voltage is set to more than GND.

(Note 11) An excessive input current will flow when input voltages of more than Supply Voltage(V₊)+0.6V or less than GND-0.6V are applied.

The input current can be set to less than the rated current by adding a limiting resistor.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Electrical Characteristics

OBD12730G (Unless otherwise specified V+=+5V, GND=0V, T_A=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply Current	I _{DD}	-	320	550	μA	R _L =∞, +IN=2.5V
Input Offset Voltage ^(Note 12)	V _{IO}	-	1	5	mV	-
Input Bias Current ^(Note 12)	I _B	-	50	250	nA	-
Input Offset Current ^(Note 12)	I _{IO}	-	5	100	nA	-
Large Signal Voltage Gain	A _V	60	85	-	dB	R _L =2kΩ ^(Note 13)
Common-mode Rejection Ratio	CMRR	55	70	-	dB	-
Power Supply Rejection Ratio	PSRR	70	85	-	dB	-
Maximum Output Voltage (High)	V _{OH1}	4.9	4.95	-	V	R _L =20kΩ ^(Note 13)
	V _{OH2}	4.75	4.85	-	V	R _L =2kΩ ^(Note 13)
Maximum Output Voltage (Low)	V _{OL1}	-	0.05	0.1	V	R _L =20kΩ ^(Note 13)
	V _{OL2}	-	0.15	0.25	V	R _L =2kΩ ^(Note 13)
Output Source Current	I _{SOURCE}	-	12	-	mA	OUT=0V
Output Sink Current	I _{SINK}	-	5	-	mA	OUT=5V
Input Common-mode Voltage Range	V _{ICM}	0	-	5	V	CMRR>55dB
Gain Bandwidth	GBW	-	1	-	MHz	f=10kHz
Unity Gain Frequency	f _T	-	1	-	MHz	R _L =2kΩ ^(Note 13)
Phase Margin	θ	-	75	-	deg	R _L =2kΩ ^(Note 13)
Input Referred Noise Voltage	V _N	-	10	-	nV/√Hz	f=1kHz
		-	1.2	-	μVrms	R _S =100Ω, DIN-AUDIO
Slew Rate	SR	-	0.4	-	V/μS	R _L =2kΩ ^(Note 13)

(Note 12) Absolute value

(Note 13) Output load resistance connect to a half of V+

Electrical Characteristics – continued

OBD12732xxx (Unless otherwise specified V+=+5V, GND=0V, T_A=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply Current	I _{DD}	-	580	900	μA	R _L =∞, +IN=2.5V All Op-Amps
Input Offset Voltage ^(Note 14)	V _{IO}	-	1	5	mV	-
Input Bias Current ^(Note 14)	I _B	-	50	250	nA	-
Input Offset Current ^(Note 14)	I _{IO}	-	5	100	nA	-
Large Signal Voltage Gain	A _V	60	85	-	dB	R _L =2kΩ ^(Note 15)
Common-mode Rejection Ratio	CMRR	55	70	-	dB	-
Power Supply Rejection Ratio	PSRR	70	85	-	dB	-
Maximum Output Voltage (High)	V _{OH1}	4.9	4.95	-	V	R _L =20kΩ ^(Note 15)
	V _{OH2}	4.75	4.85	-	V	R _L =2kΩ ^(Note 15)
Maximum Output Voltage (Low)	V _{OL1}	-	0.05	0.1	V	R _L =20kΩ ^(Note 15)
	V _{OL2}	-	0.15	0.25	V	R _L =2kΩ ^(Note 15)
Output Source Current	I _{SOURCE}	-	12	-	mA	OUT=0V
Output Sink Current	I _{SINK}	-	5	-	mA	OUT=5V
Input Common-mode Voltage Range	V _{ICM}	0	-	5	V	CMRR>55dB
Gain Bandwidth	GBW	-	1	-	MHz	f=10kHz
Unity Gain Frequency	f _T	-	1	-	MHz	R _L =2kΩ ^(Note 15)
Phase Margin	θ	-	75	-	deg	R _L =2kΩ ^(Note 15)
Input Referred Noise Voltage	V _N	-	10	-	nV/√Hz	f=1kHz
		-	1.2	-	μVrms	R _S =100Ω, DIN-AUDIO
Slew Rate	SR	-	0.4	-	V/μS	R _L =2kΩ ^(Note 15)
Channel Separation	CS	-	90	-	dB	f=1kHz, R _L =2kΩ ^(Note 15) OUT=1.2Vrms

(Note 14) Absolute value

(Note 15) Output load resistance connect to a half of V+

Electrical Characteristics – continued

OBD12734xxx (Unless otherwise specified V+=+5V, GND=0V, T_A=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply Current	I _{DD}	-	1200	1800	μA	R _L =∞, +IN=2.5V All Op-Amps
Input Offset Voltage ^(Note 16)	V _{IO}	-	1	5	mV	-
Input Bias Current ^(Note 16)	I _B	-	50	250	nA	-
Input Offset Current ^(Note 16)	I _{IO}	-	5	100	nA	-
Large Signal Voltage Gain	A _V	60	85	-	dB	R _L =2kΩ ^(Note 17)
Common-mode Rejection Ratio	CMRR	55	70	-	dB	-
Power Supply Rejection Ratio	PSRR	70	85	-	dB	-
Maximum Output Voltage (High)	V _{OH1}	4.9	4.95	-	V	R _L =20kΩ ^(Note 17)
	V _{OH2}	4.75	4.85	-	V	R _L =2kΩ ^(Note 17)
Maximum Output Voltage (Low)	V _{OL1}	-	0.05	0.1	V	R _L =20kΩ ^(Note 17)
	V _{OL2}	-	0.15	0.25	V	R _L =2kΩ ^(Note 17)
Output Source Current	I _{SOURCE}	-	12	-	mA	OUT=0V
Output Sink Current	I _{SINK}	-	5	-	mA	OUT=5V
Input Common-mode Voltage Range	V _{ICM}	0	-	5	V	CMRR>55dB
Gain Bandwidth	GBW	-	1	-	MHz	f=10kHz
Unity Gain Frequency	f _T	-	1	-	MHz	R _L =2kΩ ^(Note 17)
Phase Margin	θ	-	75	-	deg	R _L =2kΩ ^(Note 17)
		-	10	-	nV/√Hz	f=1kHz
Input Referred Noise Voltage	V _N	-	1.2	-	μVrms	R _S =100Ω, DIN-AUDIO
		-	0.4	-	V/μS	R _L =2kΩ ^(Note 17)
Slew Rate	SR	-	0.4	-	V/μS	R _L =2kΩ ^(Note 17)
Channel Separation	CS	-	133	-	dB	f=1kHz, R _L =2kΩ ^(Note 17) OUT=1.2Vrms

(Note 16) Absolute value

(Note 17) Output load resistance connect to a half of V+

Description of electrical characteristics

Described here are the terms of electric characteristics used in this datasheet. Items and symbols used are also shown. Note that item name, symbol and their meaning may differ from those on other manufacturer's document or general documents.

1. Absolute maximum ratings

Absolute maximum rating items indicate the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

- (1) Supply Voltage (V_{+}/GND)
Indicates the maximum voltage that can be applied between the V_{+} terminal and GND terminal without deterioration or destruction of characteristics of internal circuit.
- (2) Differential Input Voltage (V_{ID})
Indicates the maximum voltage that can be applied between non-inverting and inverting terminals without damaging the IC.
- (3) Input Common-mode Voltage Range (V_{ICM})
Indicates the maximum voltage that can be applied to the non-inverting and inverting terminals without deterioration or destruction of electrical characteristics. Input common-mode voltage range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the input common-mode voltage range characteristics.
- (4) Power Dissipation (P_D)
Indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25°C (normal temperature). As for package product, P_D is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

2. Electrical characteristics

- (1) Supply Current (I_{DD})
Indicates the current that flows within the IC under specified no-load conditions.
- (2) Input Offset Voltage (V_{IO})
Indicates the voltage difference between non-inverting terminal and inverting terminals. It can be translated into the input voltage difference required for setting the output voltage at 0 V.
- (3) Input Bias Current (I_B)
Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias currents at the non-inverting and inverting terminals.
- (4) Input Offset Current (I_{IO})
Indicates the difference of input bias current between the non-inverting and inverting terminals.
- (5) Large Signal Voltage Gain (A_V)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
 $A_V = (\text{Output voltage}) / (\text{Differential Input voltage})$
- (6) Common-mode Rejection Ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when the input common mode voltage is changed. It is normally the fluctuation of DC.
 $CMRR = (\text{Change of Input common-mode voltage}) / (\text{Input offset fluctuation})$
- (7) Power Supply Rejection Ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed.
It is normally the fluctuation of DC.
 $PSRR = (\text{Change of power supply voltage}) / (\text{Input offset fluctuation})$
- (8) Maximum Output Voltage (High/Low Level Output Voltage) (V_{OH}/V_{OL})
Indicates the voltage range of the output under specified load condition. It is typically divided into maximum output voltage high and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.
- (9) Output Source Current/ Output Sink Current (I_{SOURCE} / I_{SINK})
The maximum current that can be output from the IC under specific output conditions. The output source current indicates the current flowing out from the IC, and the output sink current indicates the current flowing into the IC.
- (10) Input Common-mode Voltage Range (V_{ICM})
Indicates the input voltage range where IC normally operates.
- (11) Gain Bandwidth (GBW)
The product of the open-loop voltage gain and the frequency at which the voltage gain decreases 6dB/octave.
- (12) Unity Gain Frequency (f_T)
Indicates a frequency where the voltage gain of operational amplifier is 1.
- (13) Phase Margin (θ)
Indicates the margin of phase from 180 degree phase lag at unity gain frequency.
- (14) Input Referred Noise Voltage (V_N)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.
- (15) Slew Rate (SR)
Indicates the ratio of the change in output voltage with time when a step input signal is applied.
- (16) Channel Separation (CS)
Indicates the fluctuation in the output voltage of the driven channel with reference to the change of output voltage of the channel which is not driven.

Typical Performance Curves
OBD12730G

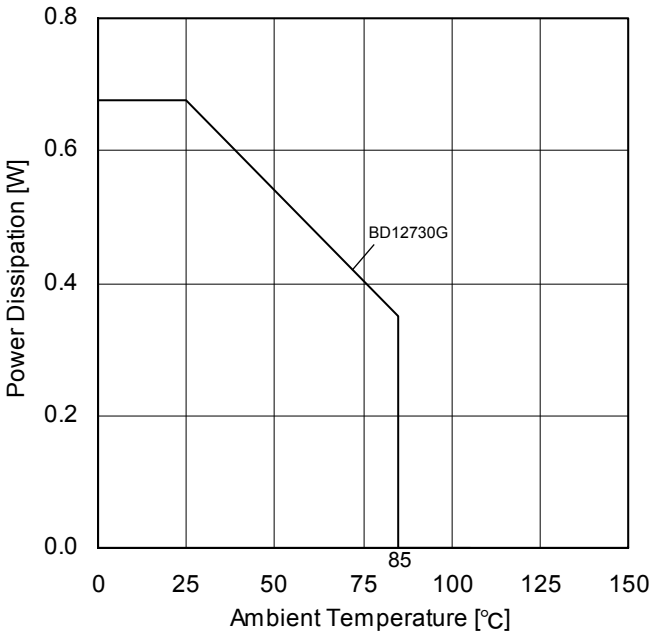


Figure 1.
Power Dissipation vs Ambient Temperature
(Derating Curve)

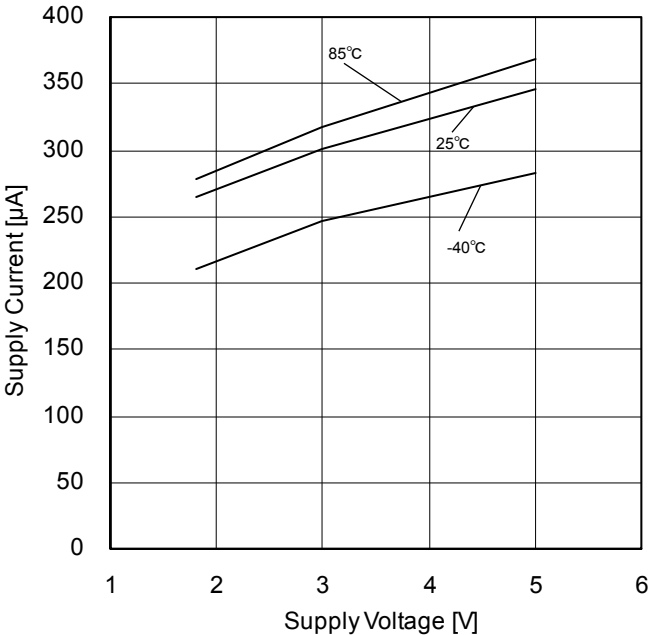


Figure 2.
Supply Current vs Supply Voltage

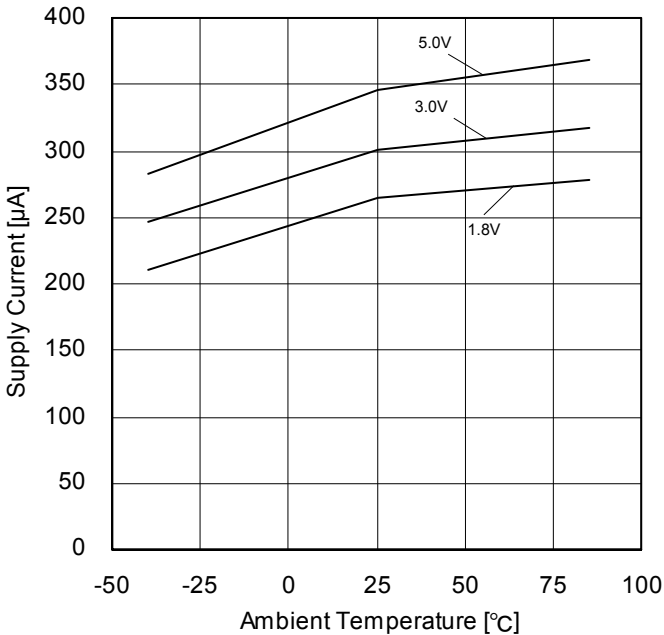


Figure 3.
Supply Current vs Ambient Temperature

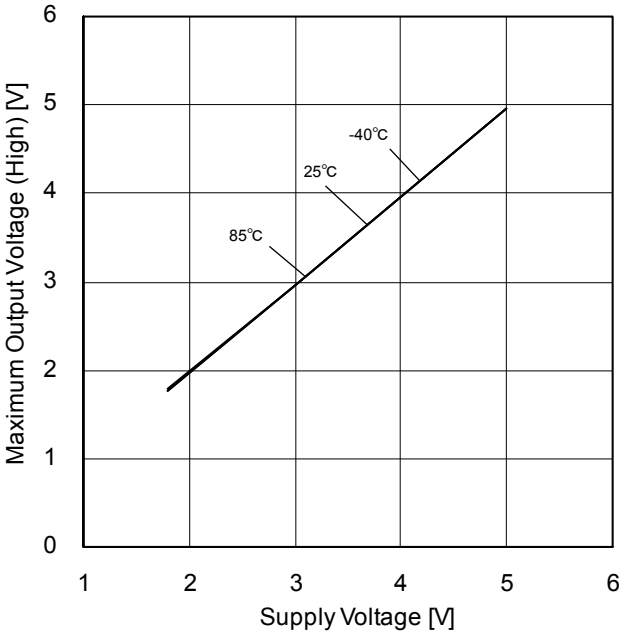


Figure 4.
Maximum Output Voltage (High) vs Supply Voltage
($R_L=20k\Omega$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12730G

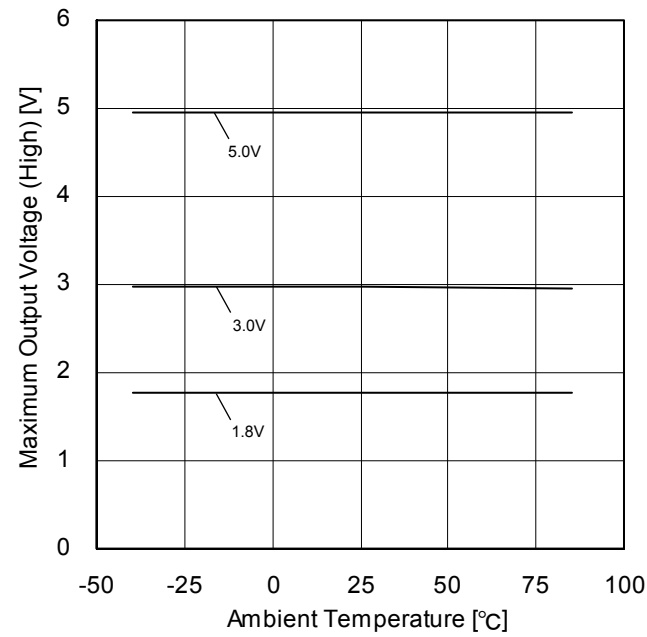


Figure 5.
Maximum Output Voltage (High) vs Ambient Temperature
($R_L=20k\Omega$)

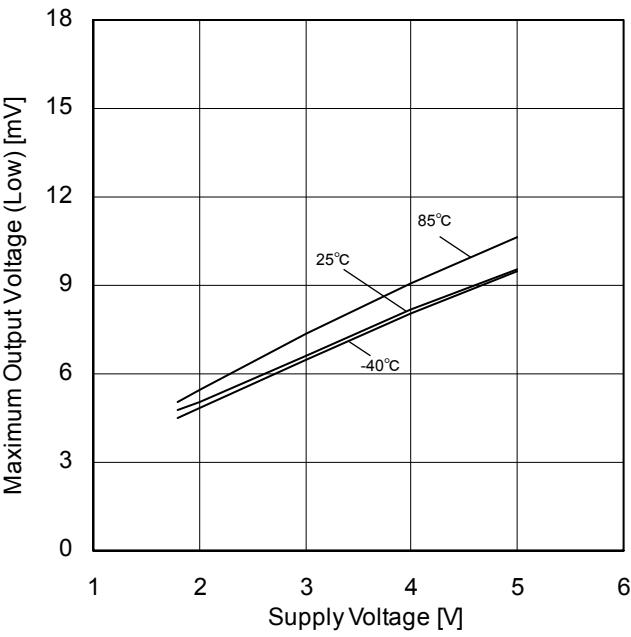


Figure 6.
Maximum Output Voltage (Low) vs Supply Voltage
($R_L=20k\Omega$)

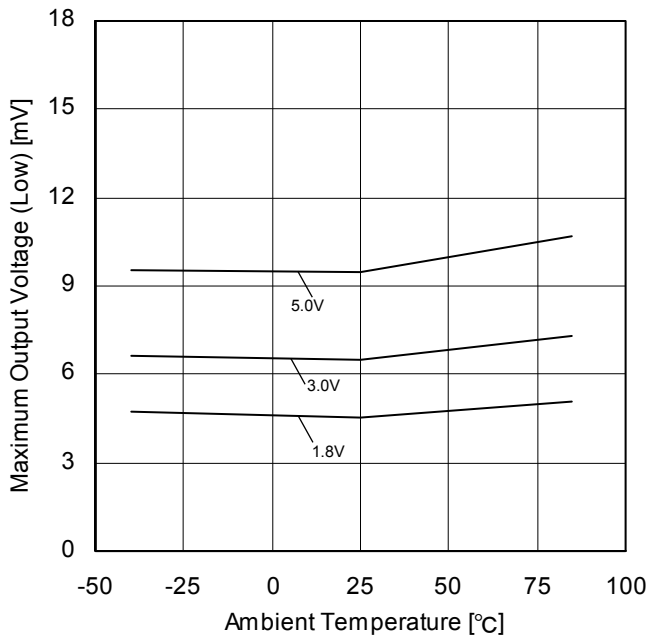


Figure 7.
Maximum Output Voltage (Low) vs Ambient Temperature
($R_L=20k\Omega$)

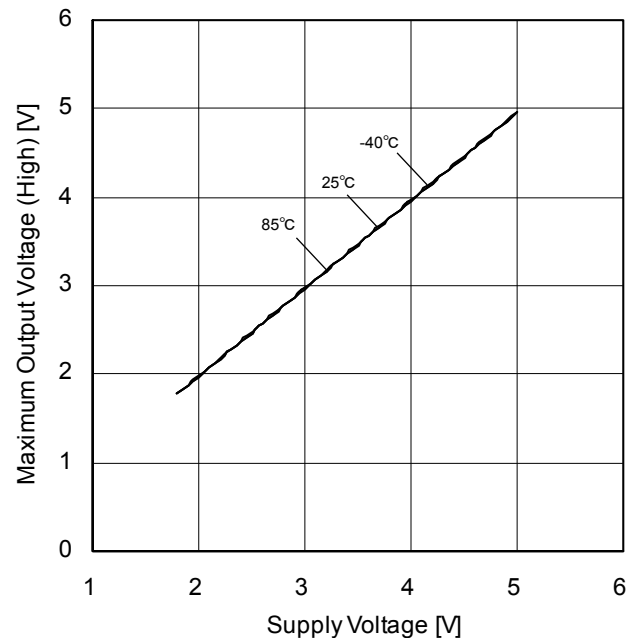


Figure 8.
Maximum Output Voltage (High) vs Supply Voltage
($R_L=2k\Omega$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued

OBD12730G

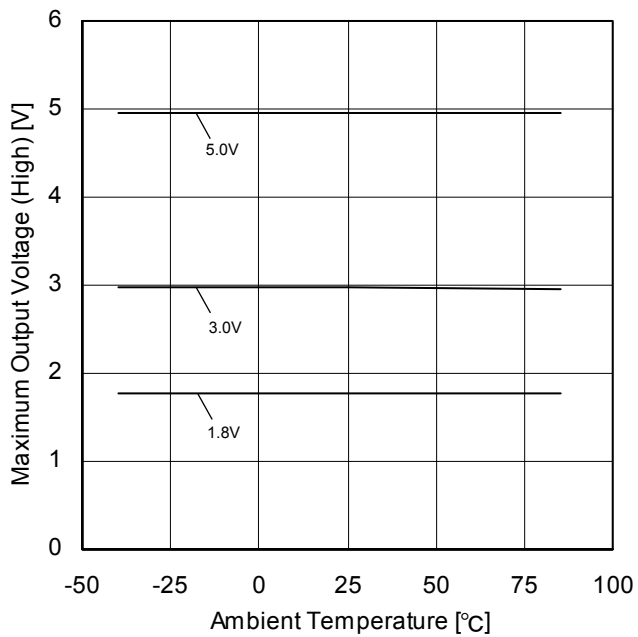


Figure 9.
Maximum Output Voltage (High) vs Ambient Temperature
($R_L=2k\Omega$)

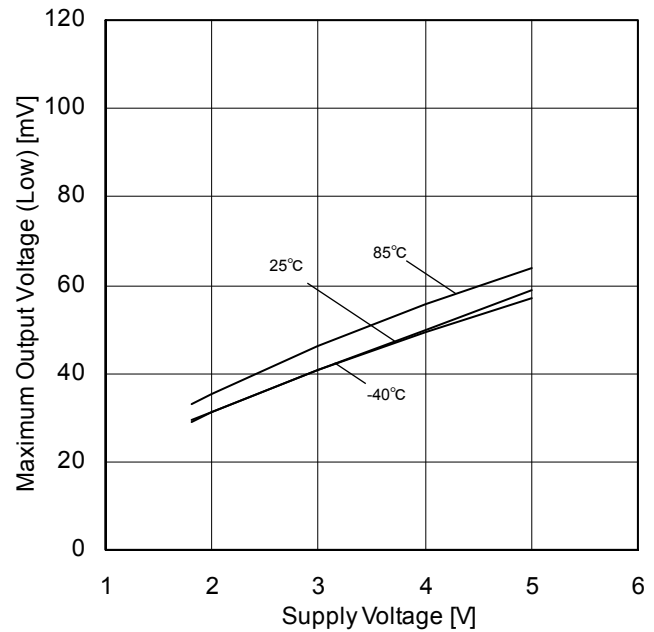


Figure 10.
Maximum Output Voltage (Low) vs Supply Voltage
($R_L=2k\Omega$)

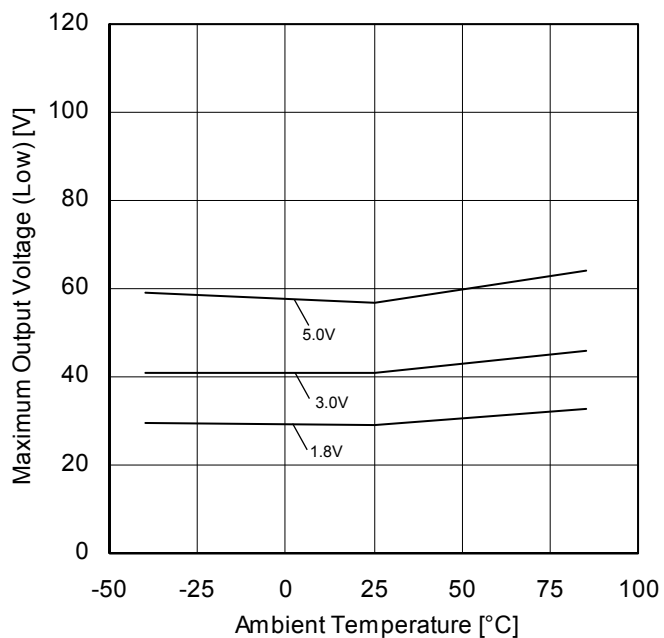


Figure 11.
Maximum Output Voltage (Low) vs Ambient Temperature
($R_L=2k\Omega$)

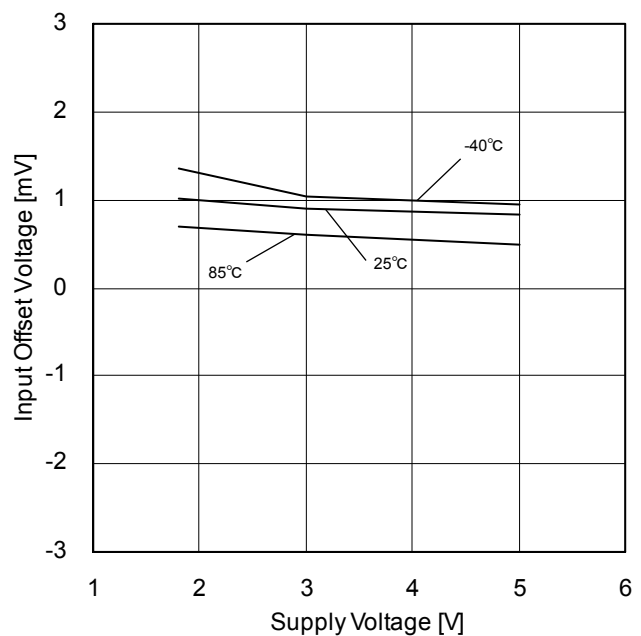


Figure 12.
Input Offset Voltage vs Supply Voltage

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued

OBD12730G

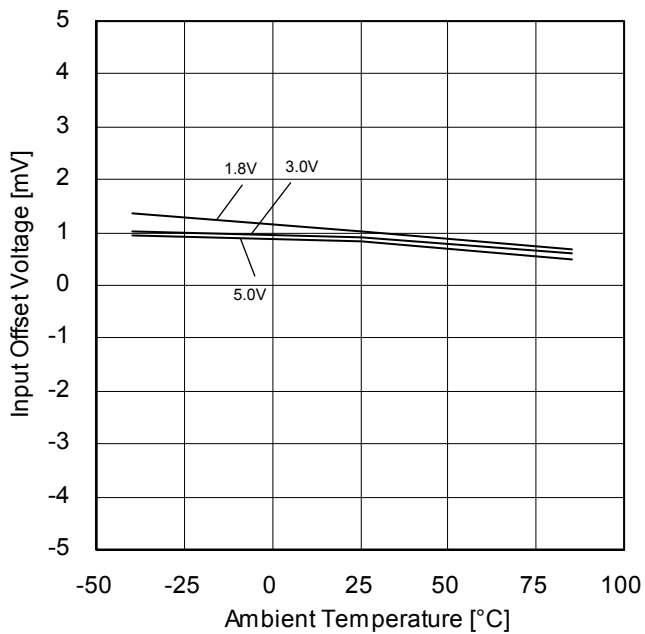


Figure 13.
Input Offset Voltage vs Ambient Temperature

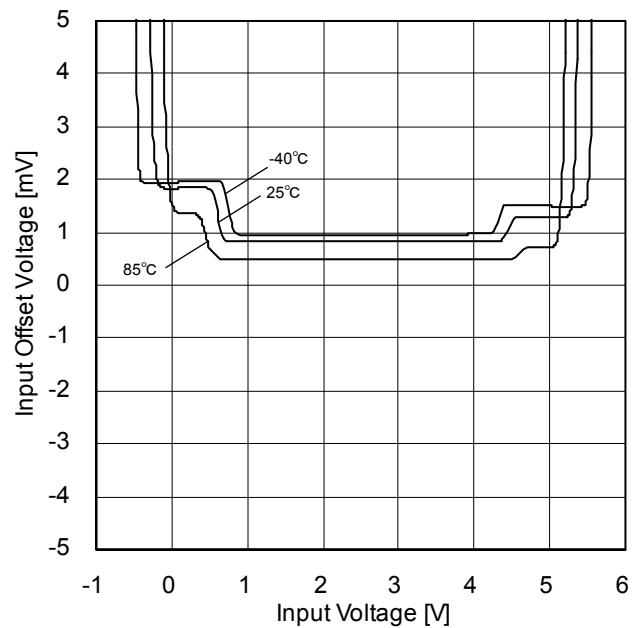


Figure 14.
Input Common Mode Voltage Range
($V^+=5V$)

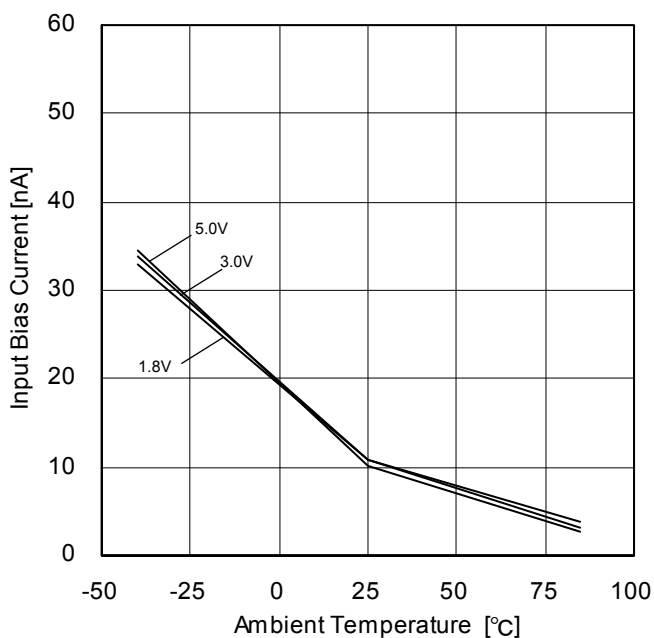


Figure 15.
Input Bias Current vs Ambient Temperature

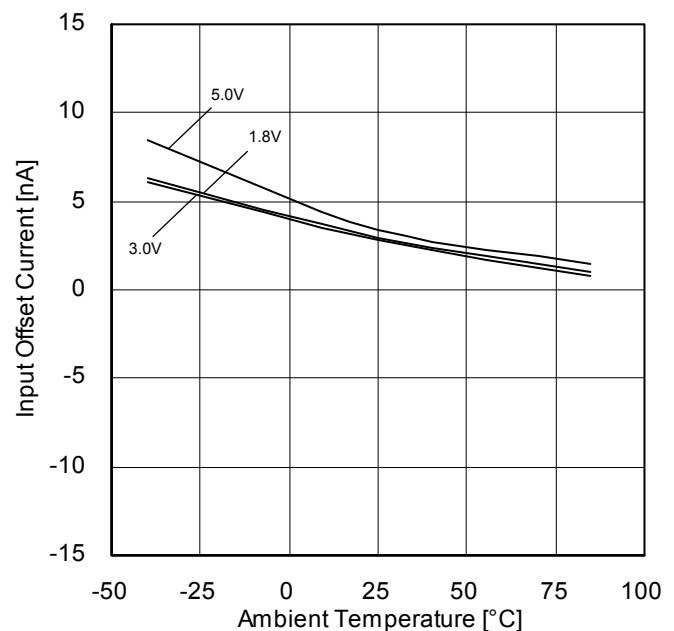


Figure 16.
Input Offset Current vs Ambient Temperature

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued

OBD12730G

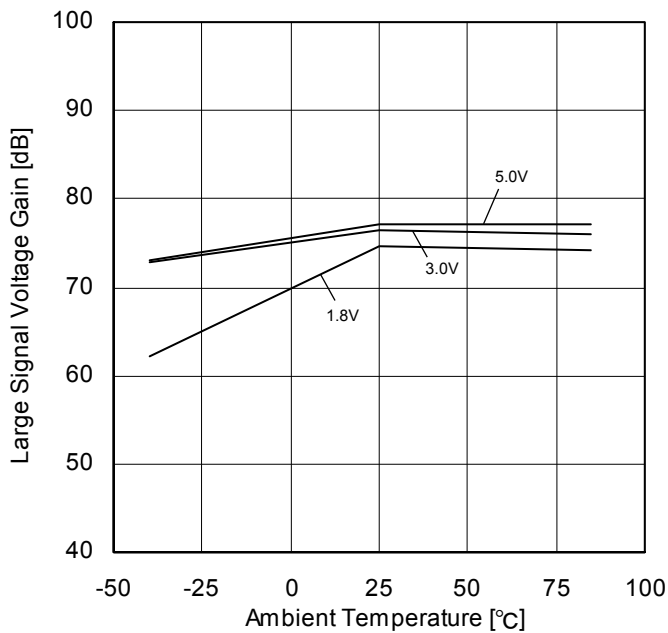


Figure 17.
Large Signal Voltage Gain vs Ambient Temperature
($R_L=2k\Omega$)

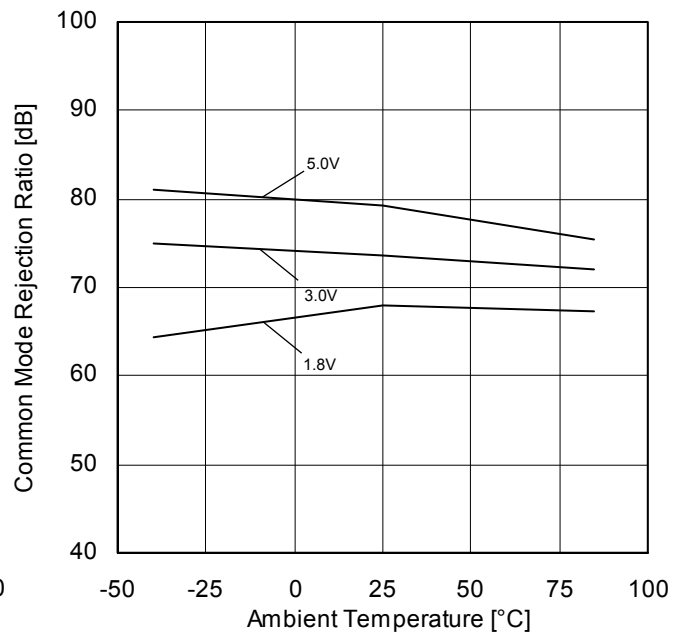


Figure 18.
Common Mode Rejection Ratio vs Ambient Temperature

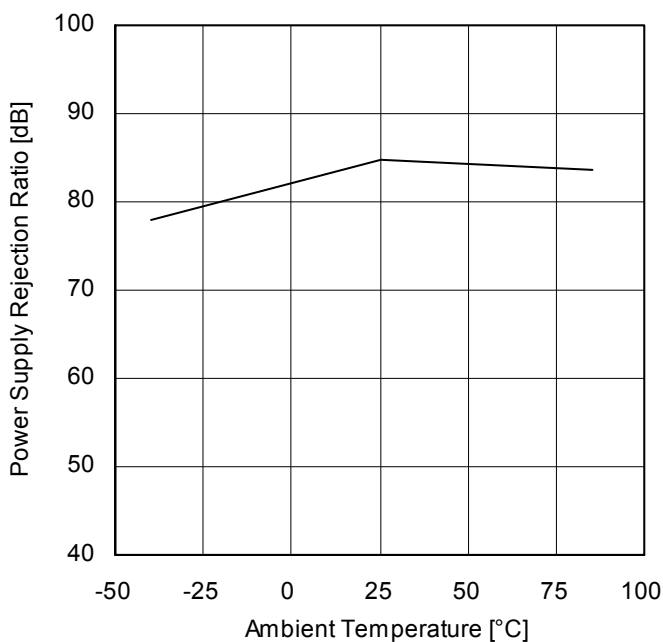


Figure 19.
Power Supply Rejection Ratio vs Ambient Temperature
($V+=1.8V$ to $5.0V$)

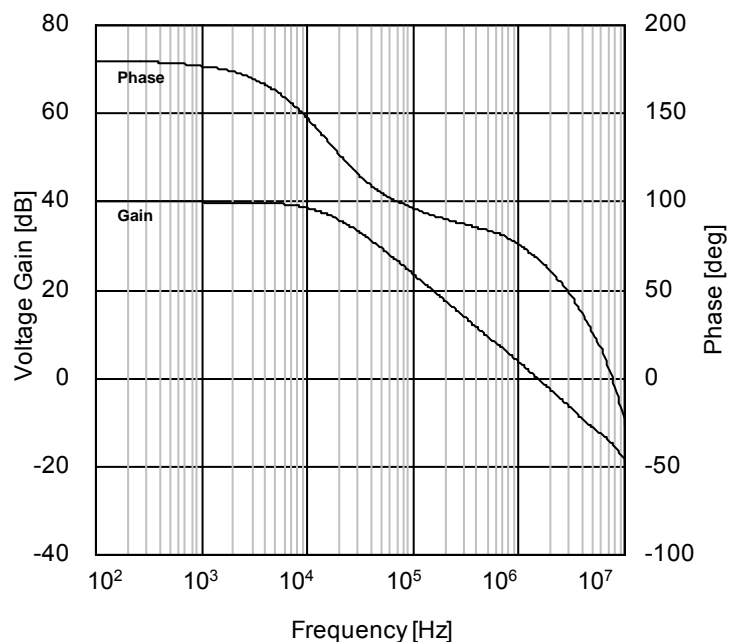


Figure 20.
Voltage Gain · Phase vs Frequency
($V+=5V$, $R_L=2k\Omega$, $T_A=25^\circ\text{C}$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12730G

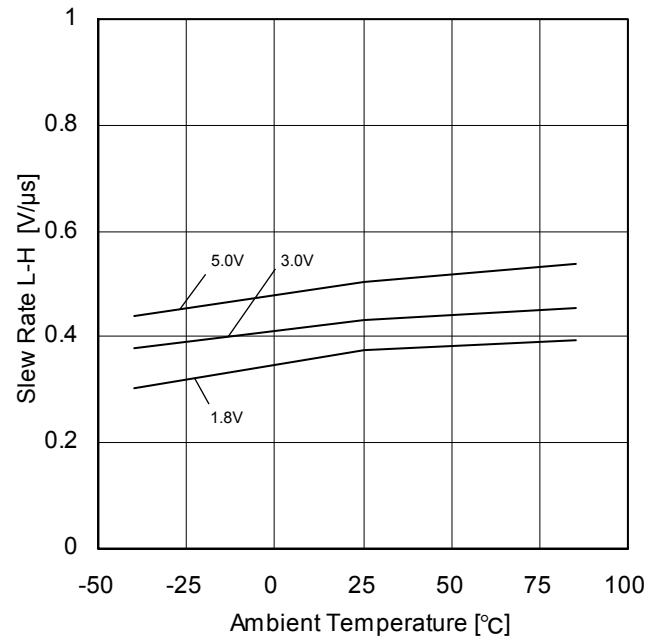


Figure 21.
Slew Rate L-H vs Ambient Temperature
($R_L=2k\Omega$)

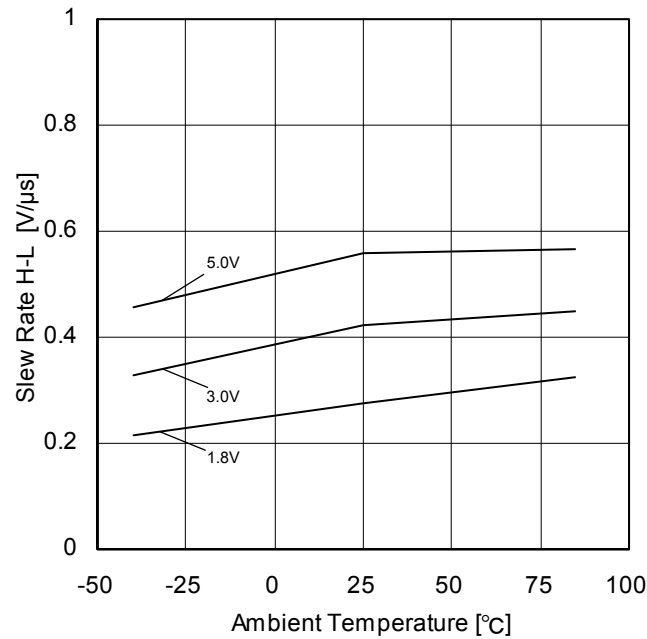


Figure 22.
Slew Rate H-L vs Ambient Temperature
($R_L=2k\Omega$)

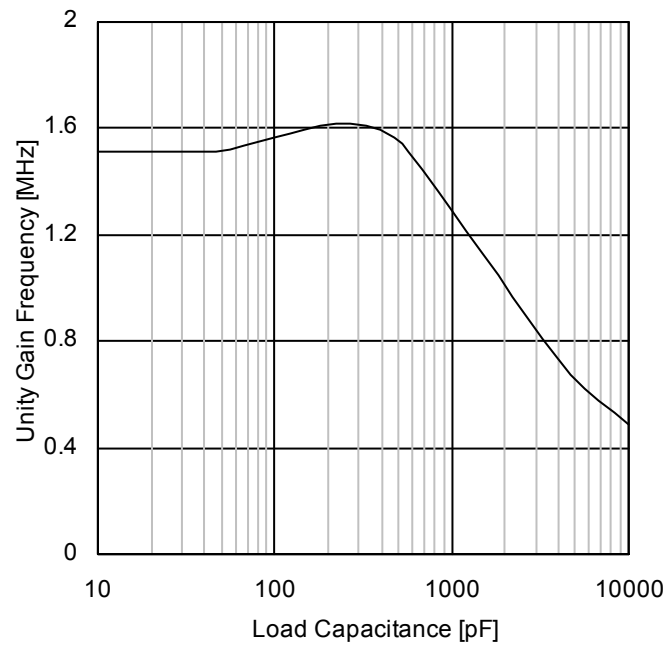


Figure 23.
Unity Gain Frequency vs Load Capacitance
($V_+=5V$, $T_A=25^\circ C$)

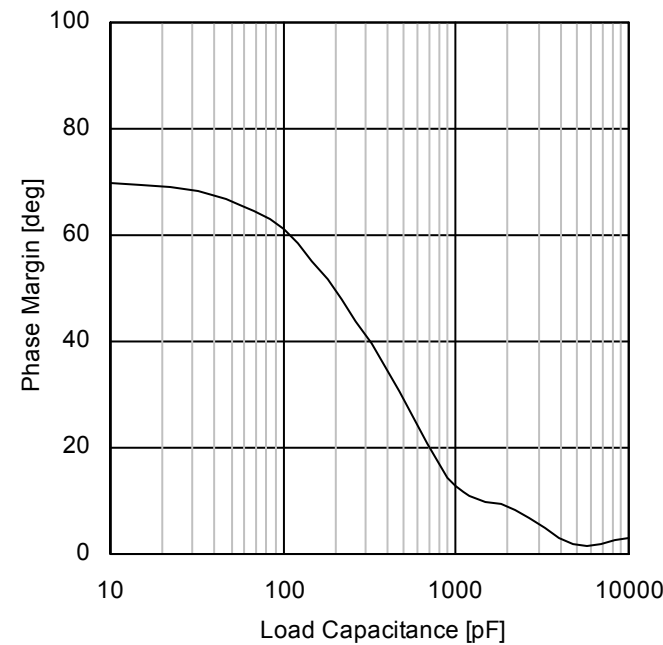


Figure 24.
Phase Margin vs Load Capacitance
($V_+=5V$, $T_A=25^\circ C$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12730G

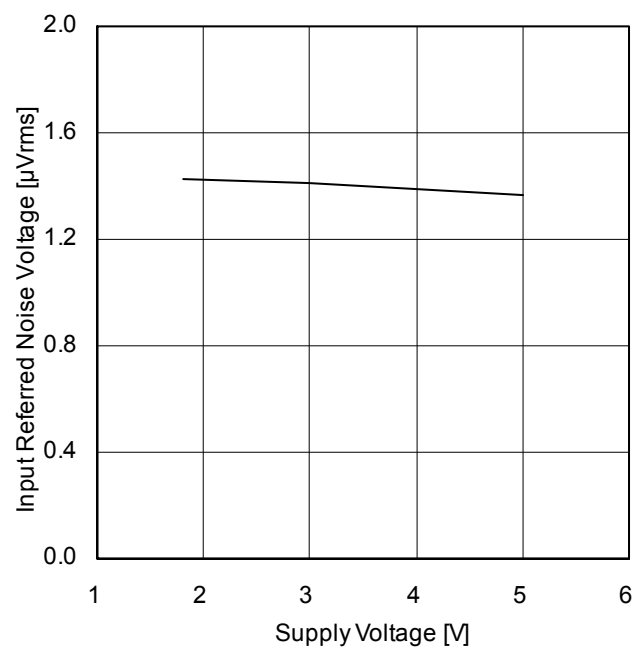


Figure 25.
Input Referred Noise Voltage vs Supply Voltage
($T_A=25^{\circ}\text{C}$)

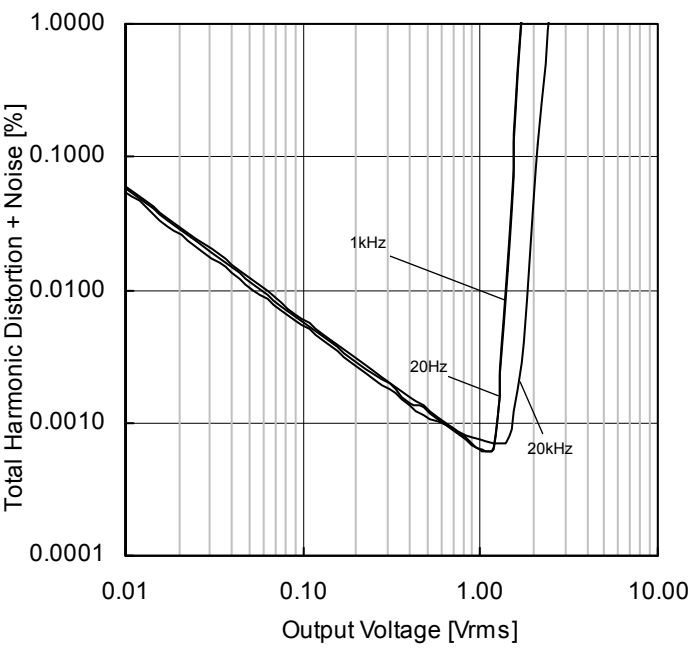


Figure 26.
Total Harmonic Distortion + Noise vs Output Voltage
($V+=5\text{V}$, $R_L=2\text{k}\Omega$, $T_A=25^{\circ}\text{C}$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued

OBD12732xxx

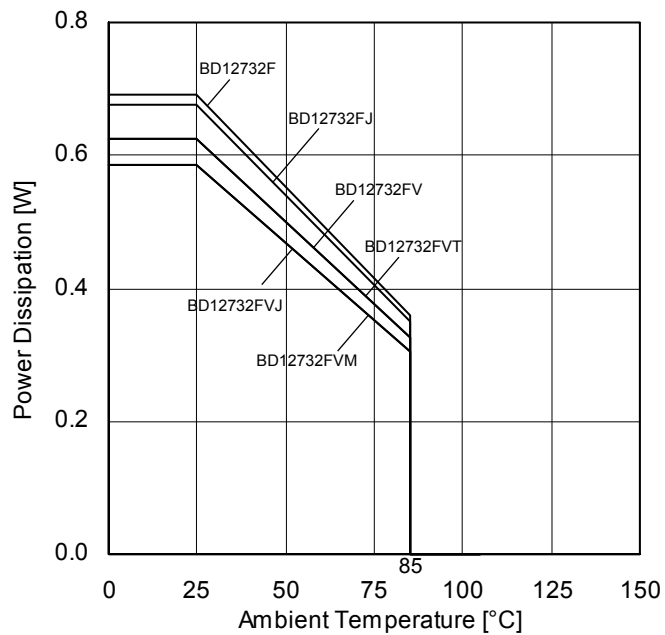


Figure 27.
Power Dissipation vs Ambient Temperature
(Derating Curve)

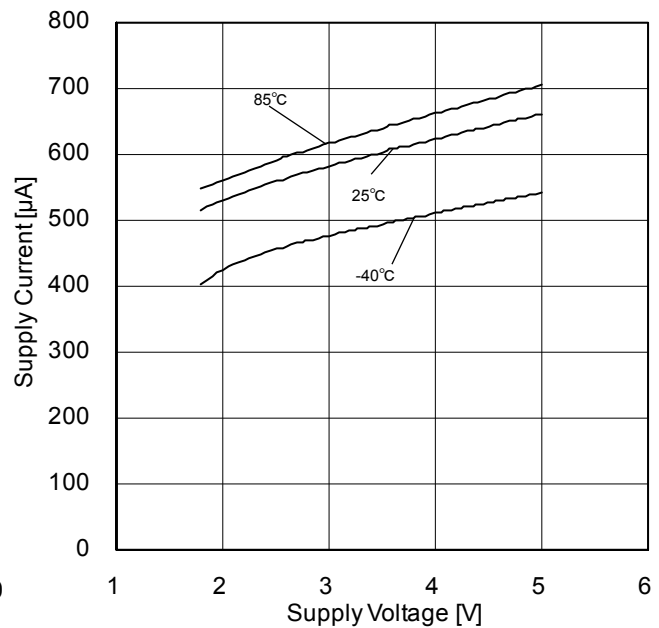


Figure 28.
Supply Current vs Supply Voltage

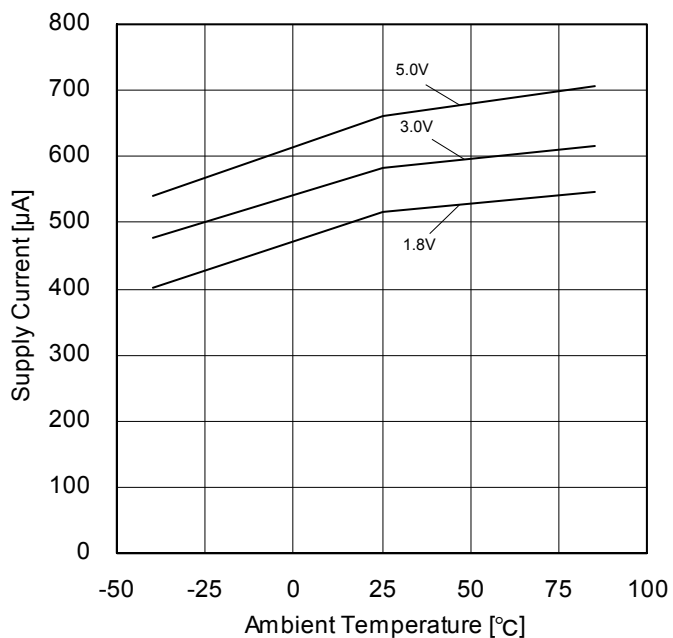


Figure 29.
Supply Current vs Ambient Temperature

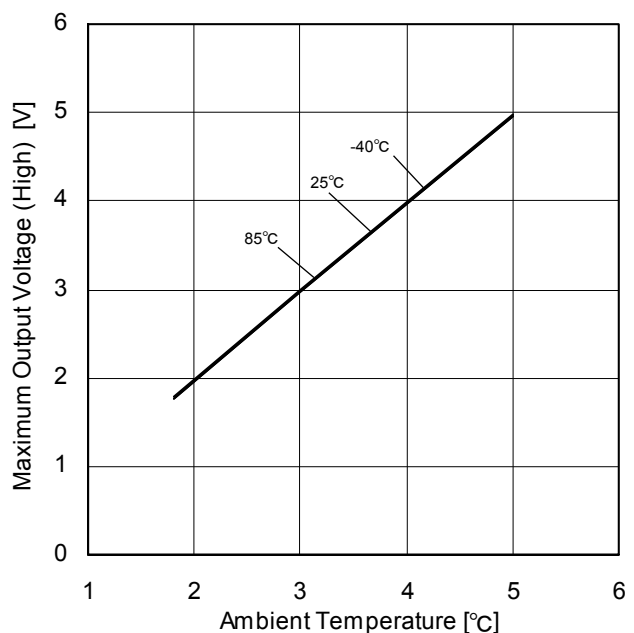


Figure 30.
Maximum Output Voltage (High) vs Supply Voltage
($R_L=20k\Omega$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued

OBD12732xxx

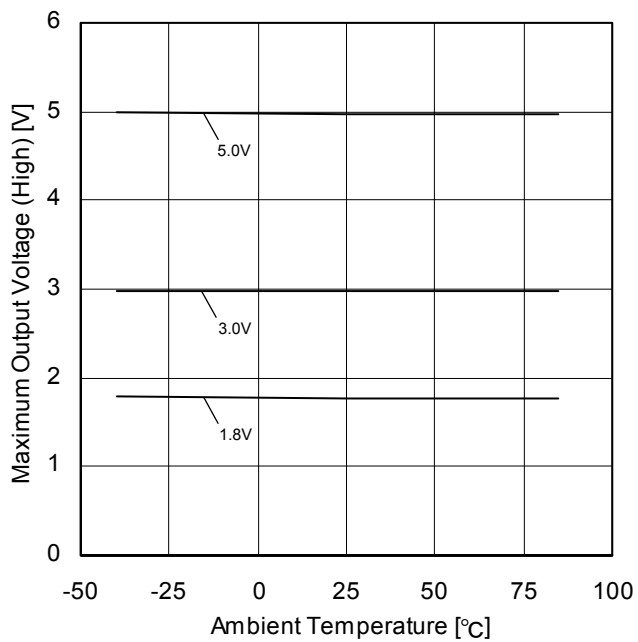


Figure 31.
Maximum Output Voltage (High) vs Ambient Temperature
($R_L=20k\Omega$)

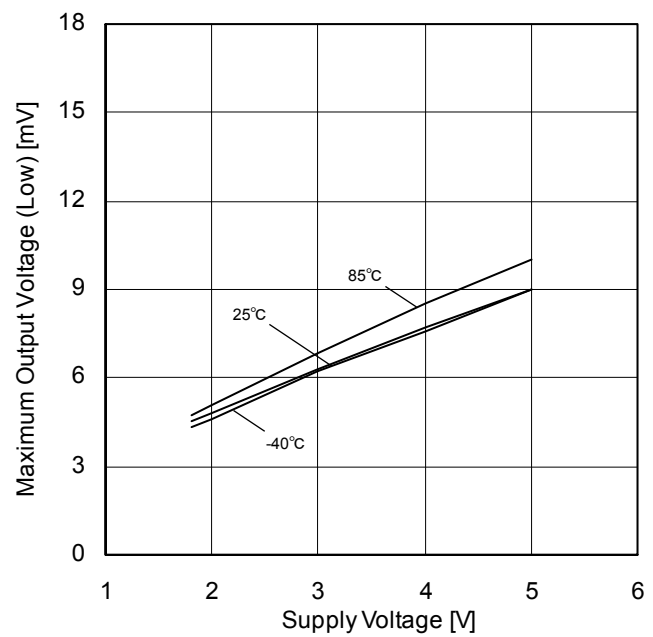


Figure 32.
Maximum Output Voltage (Low) vs Supply Voltage
($R_L=20k\Omega$)

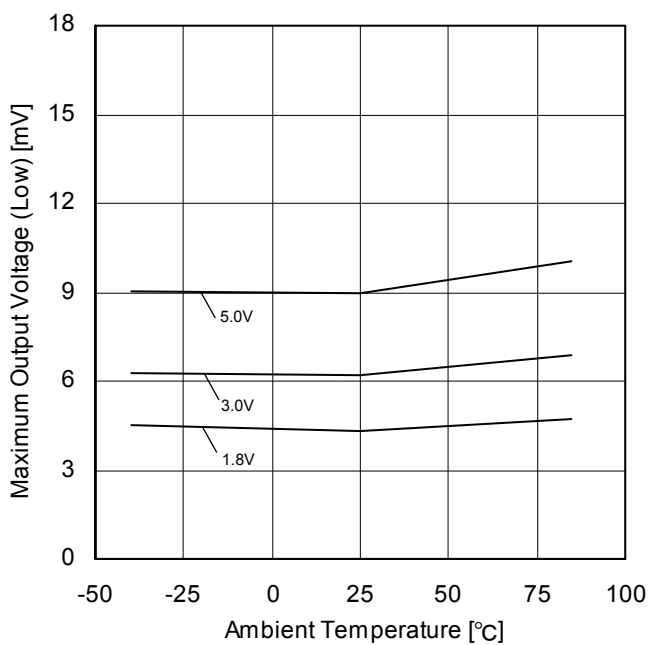


Figure 33.
Maximum Output Voltage (Low) vs Ambient Temperature
($R_L=20k\Omega$)

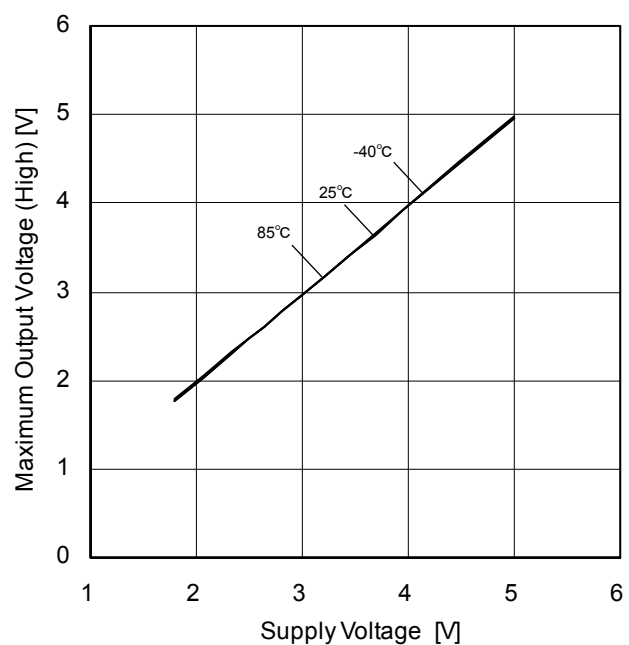


Figure 34.
Maximum Output Voltage (High) vs Supply Voltage
($R_L=2k\Omega$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12732xxx

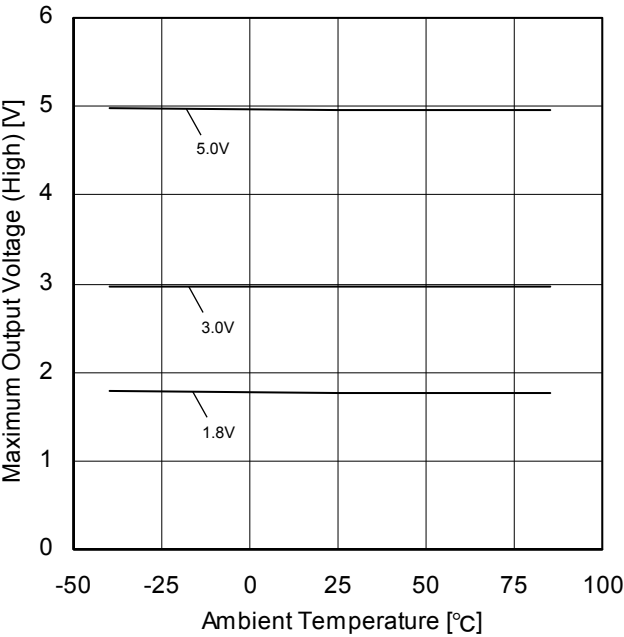


Figure 35.
Maximum Output Voltage (High) vs Ambient Temperature
($R_L=2k\Omega$)

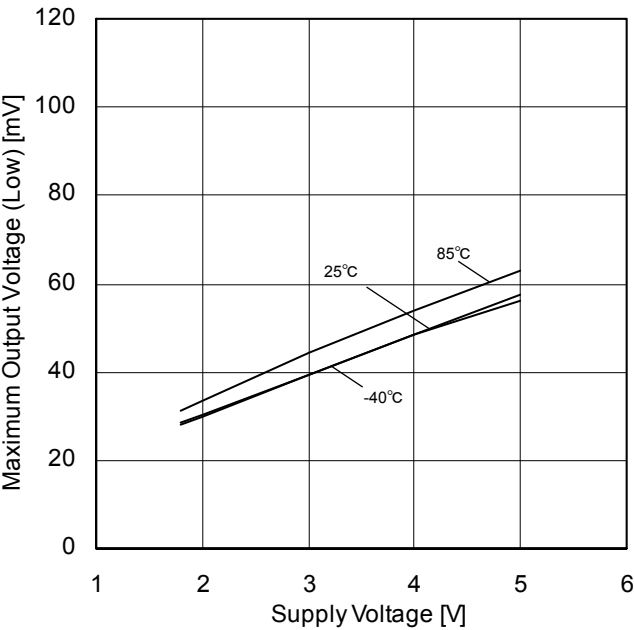


Figure 36.
Maximum Output Voltage (Low) vs Supply Voltage
($R_L=2k\Omega$)

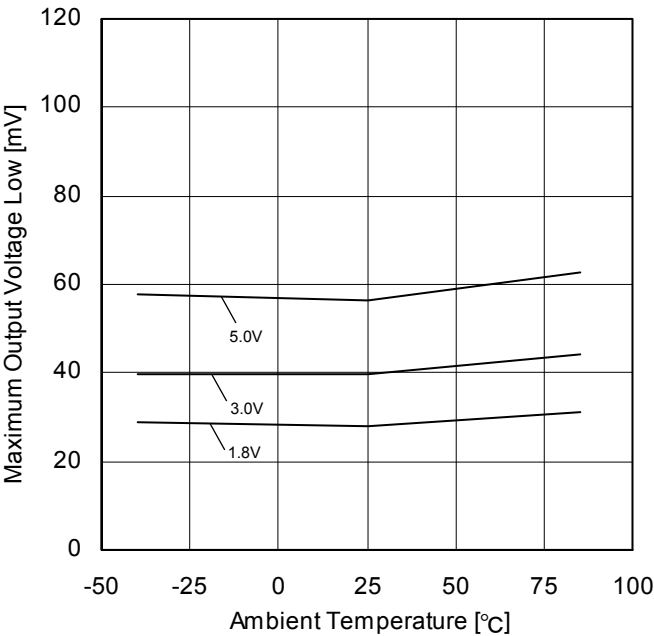


Figure 37.
Maximum Output Voltage (Low) vs Ambient Temperature
($R_L=2k\Omega$)

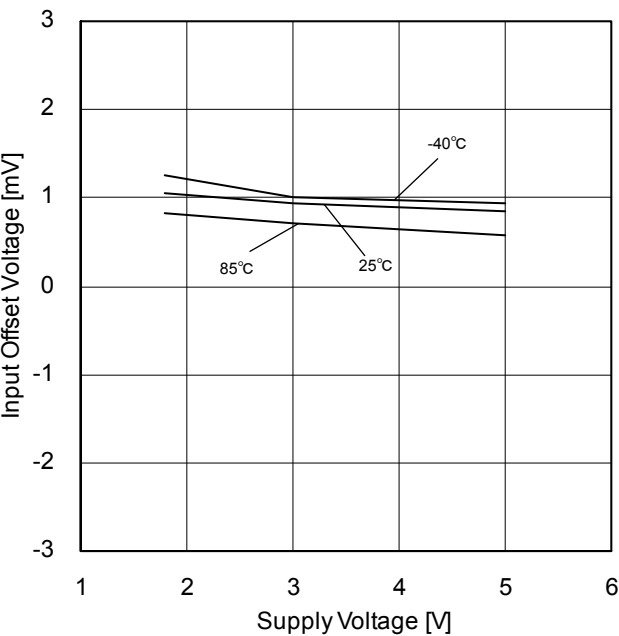


Figure 38.
Input Offset Voltage vs Supply Voltage

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12732xxx

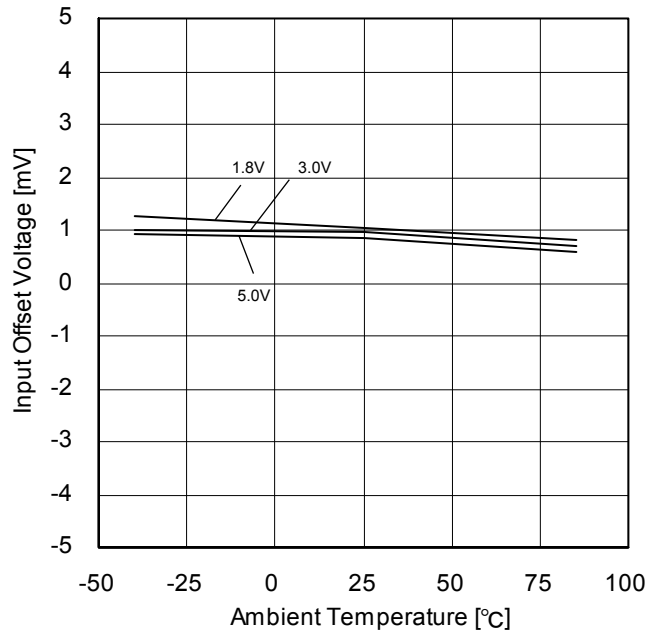


Figure 39.
Input Offset Voltage vs Ambient Temperature

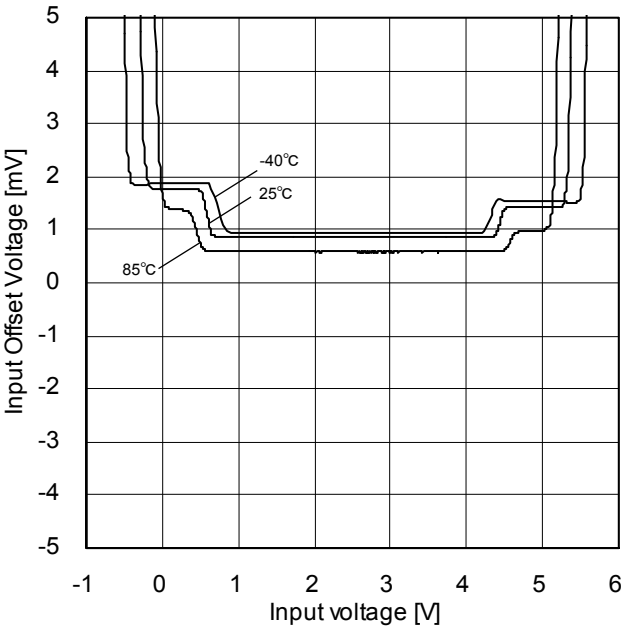


Figure 40.
Input Common Mode Voltage Range
(V+=5V)

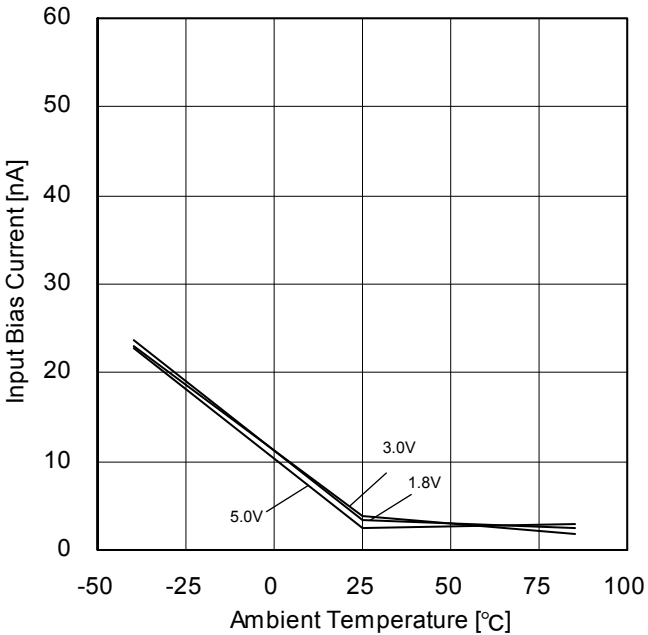


Figure 41.
Input Bias Current vs Ambient Temperature

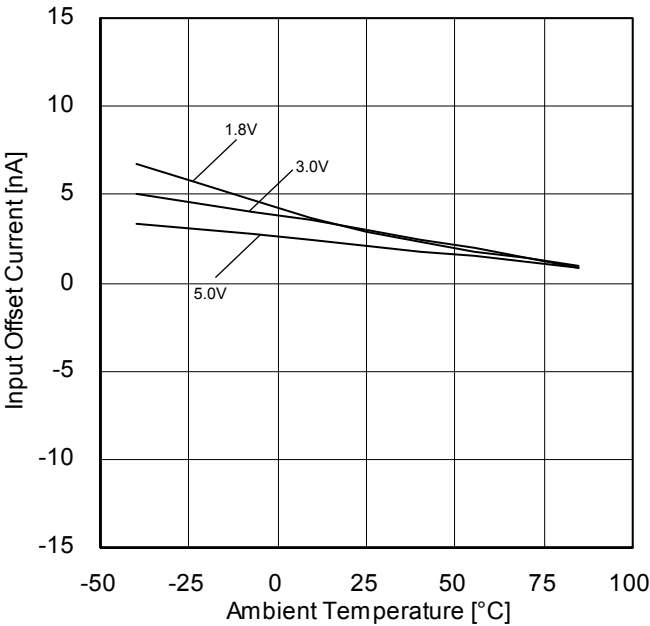


Figure 42.
Input Offset Current vs Ambient Temperature

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued

OBD12732xxx

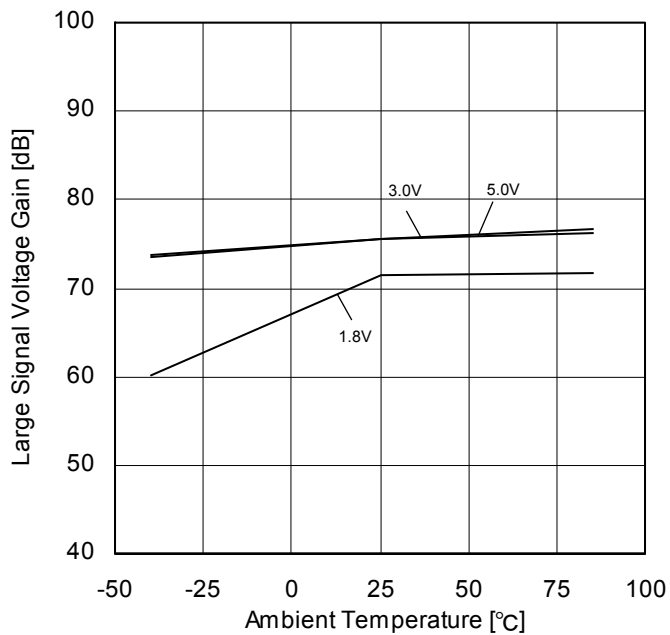


Figure 43.
Large Signal Voltage Gain vs Ambient Temperature
($R_L=2k\Omega$)

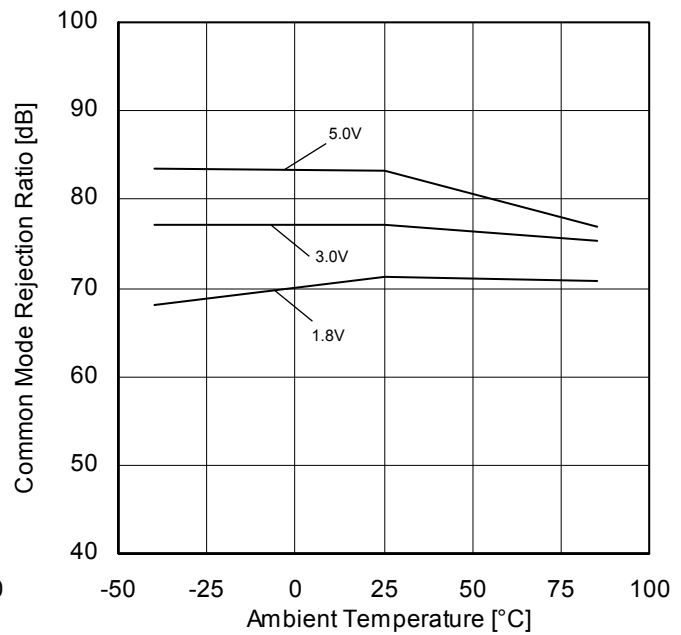


Figure 44.
Common Mode Rejection Ratio vs Ambient Temperature

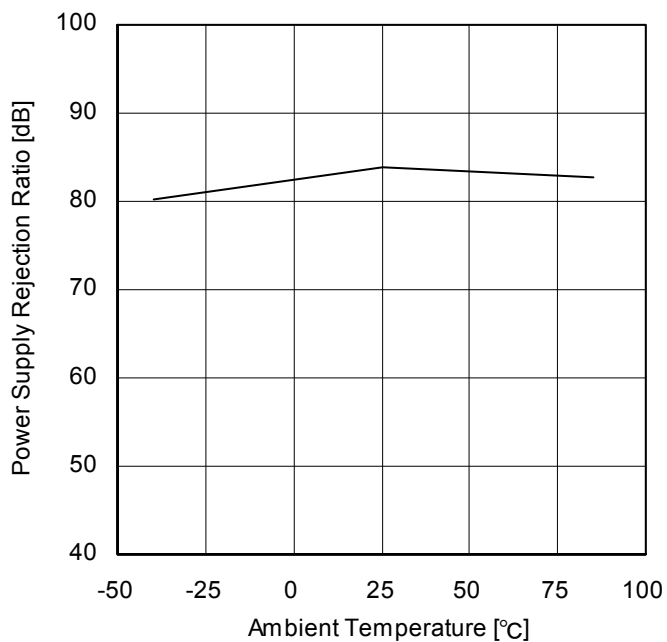


Figure 45.
Power Supply Rejection Ratio vs Ambient Temperature
($V+=1.8V$ to $5.0V$)

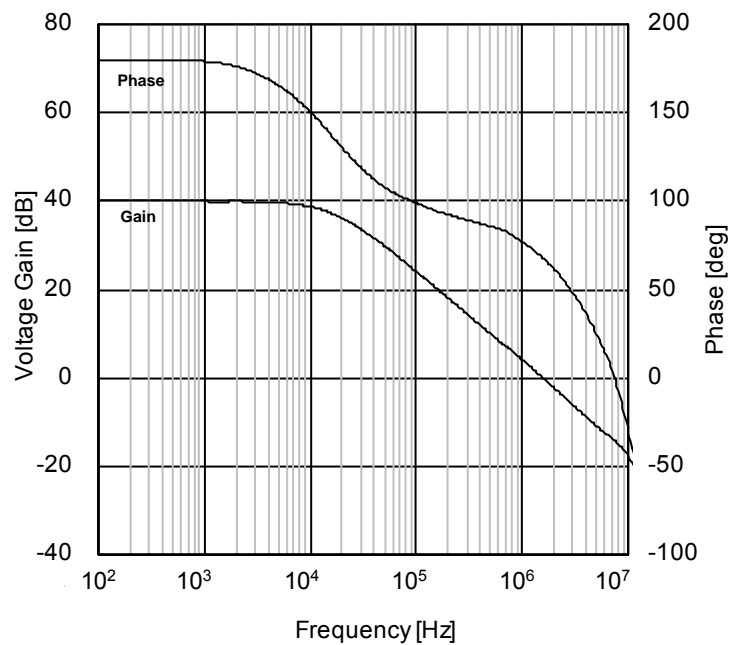


Figure 46.
Voltage Gain · Phase vs Frequency
($V+=5V$, $R_L=2k\Omega$, $T_A=25^\circ\text{C}$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12732xxx

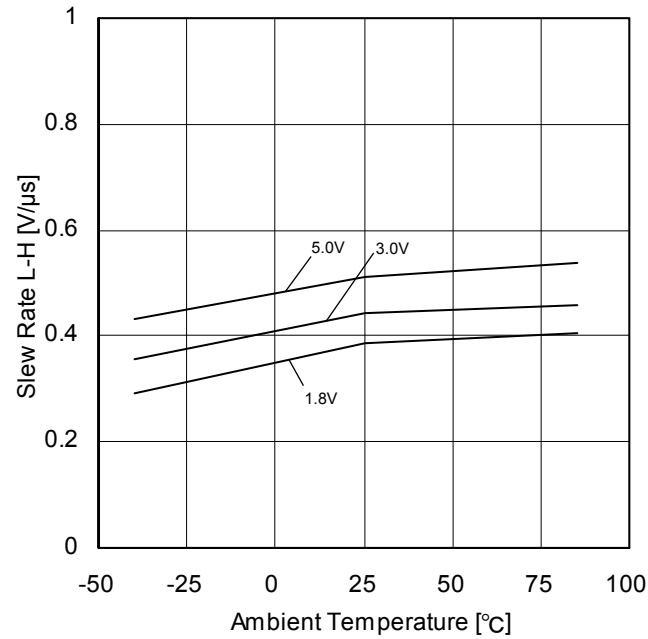


Figure 47.
Slew Rate L-H vs Ambient Temperature
($R_L=2k\Omega$)

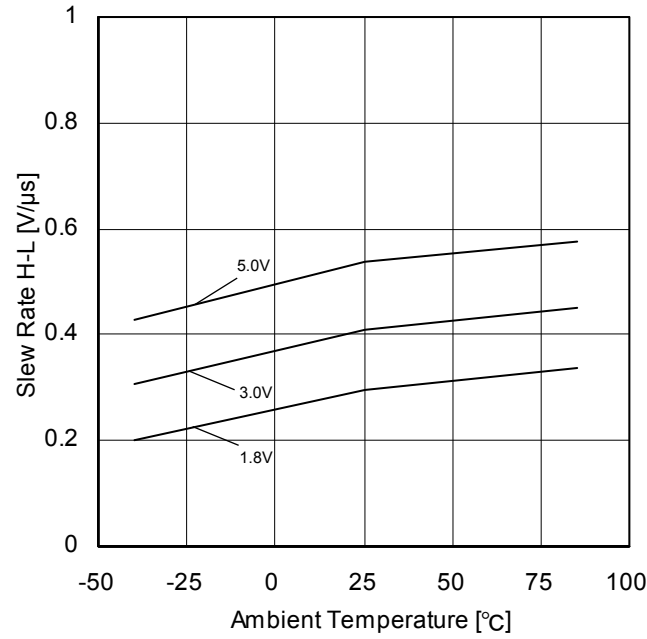


Figure 48.
Slew Rate H-L vs Ambient Temperature
($R_L=2k\Omega$)

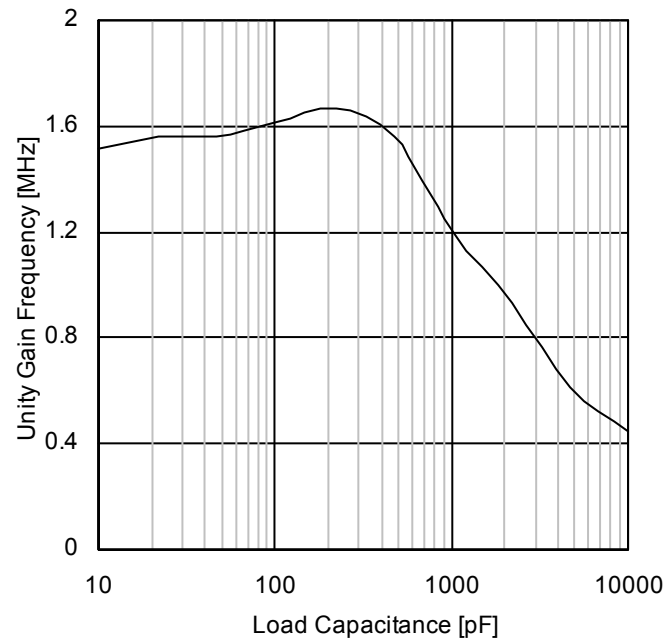


Figure 49.
Unity Gain Frequency vs Load Capacitance
($V_+=5V$, $T_A=25^\circ C$)

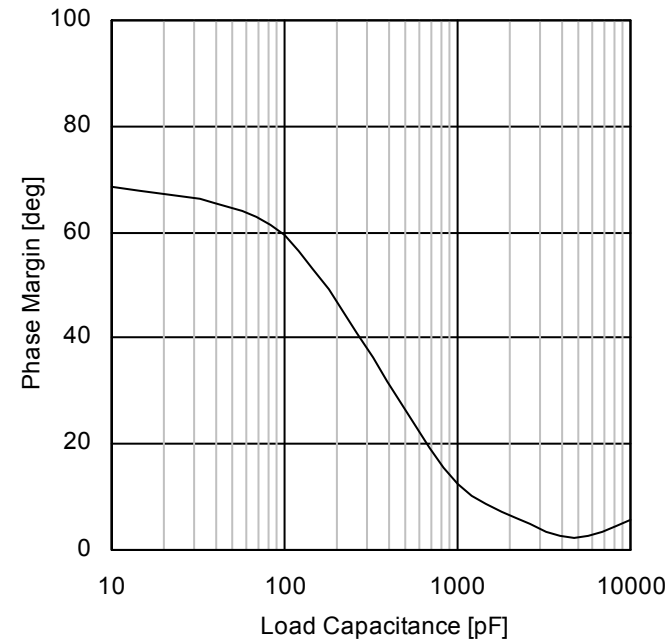


Figure 50.
Phase Margin vs Load Capacitance
($V_+=5V$, $T_A=25^\circ C$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12732xxx

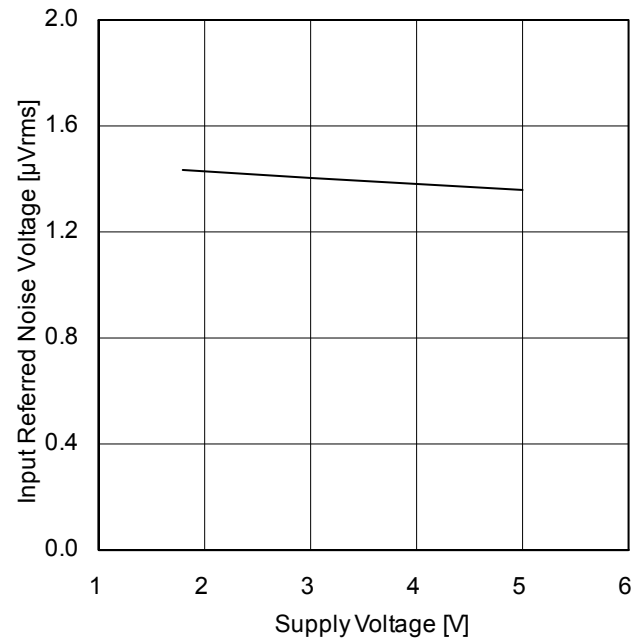


Figure 51.
Input Referred Noise Voltage vs Supply Voltage
(T_A=25°C)

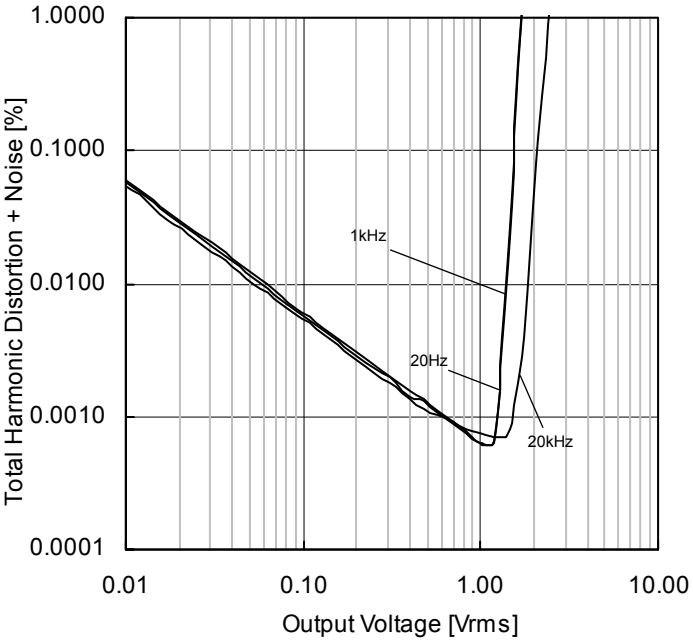


Figure 52.
Total Harmonic Distortion + Noise vs Output Voltage
(V₊=5V, R_L=2kΩ, T_A=25°C)

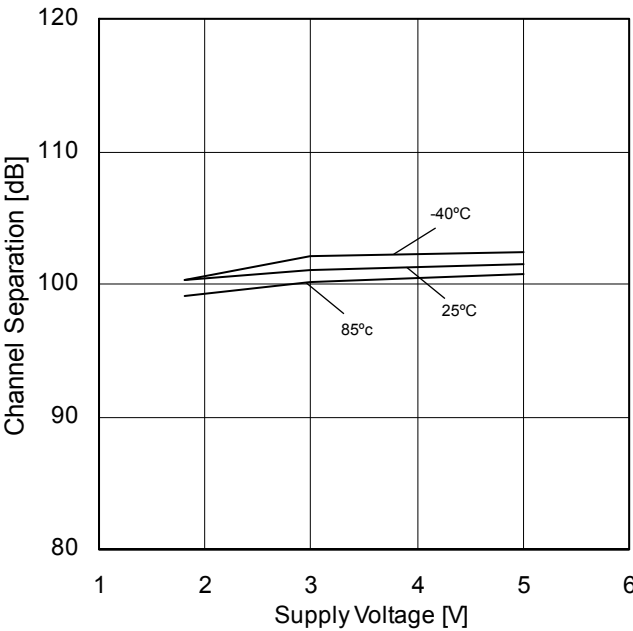


Figure 53.
Channel Separation vs Supply Voltage

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued

OBD12734xxx

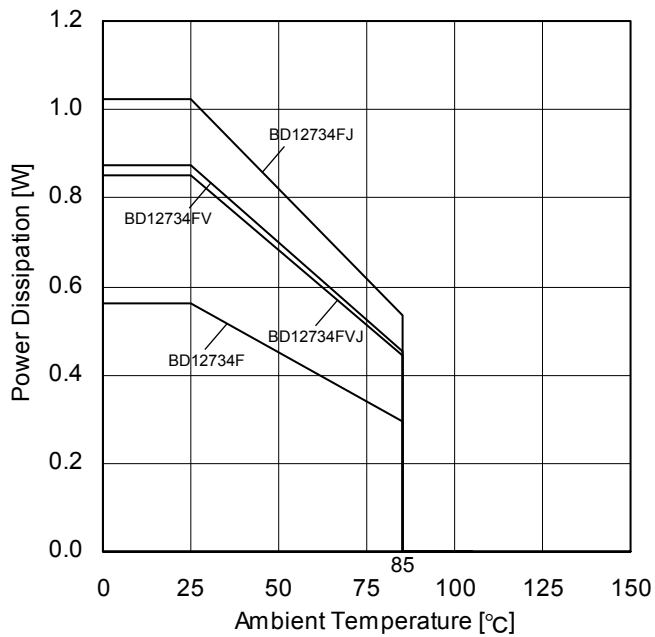


Figure 54.
Power Dissipation vs Ambient Temperature
(Derating Curve)

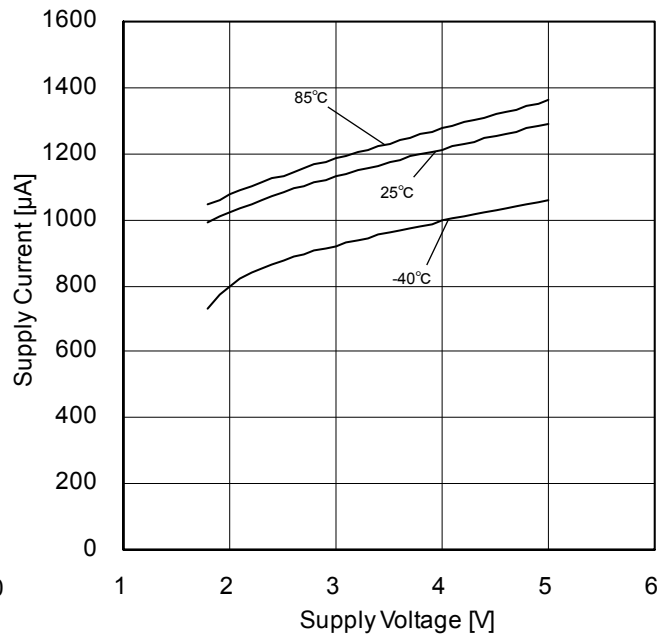


Figure 55.
Supply Current vs Supply Voltage

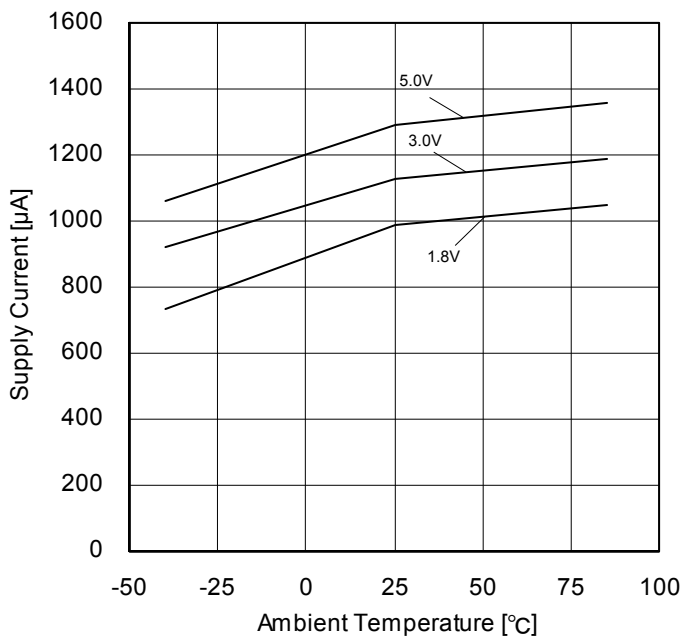


Figure 56.
Supply Current vs Ambient Temperature

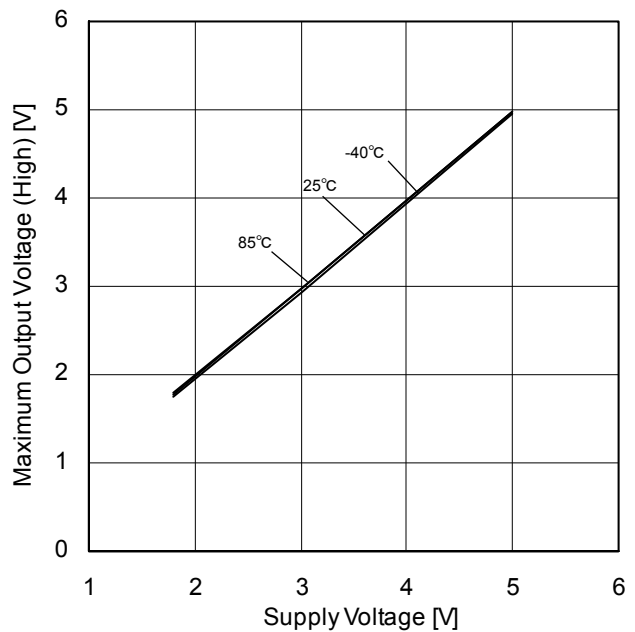


Figure 57.
Maximum Output Voltage (High) vs Supply Voltage
($R_L=20k\Omega$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12734xxx

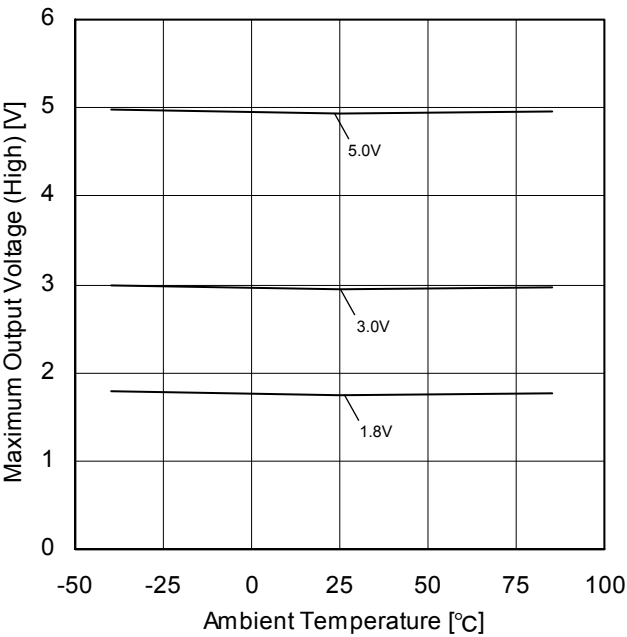


Figure 58.
Maximum Output Voltage (High) vs Ambient Temperature
($R_L=20k\Omega$)

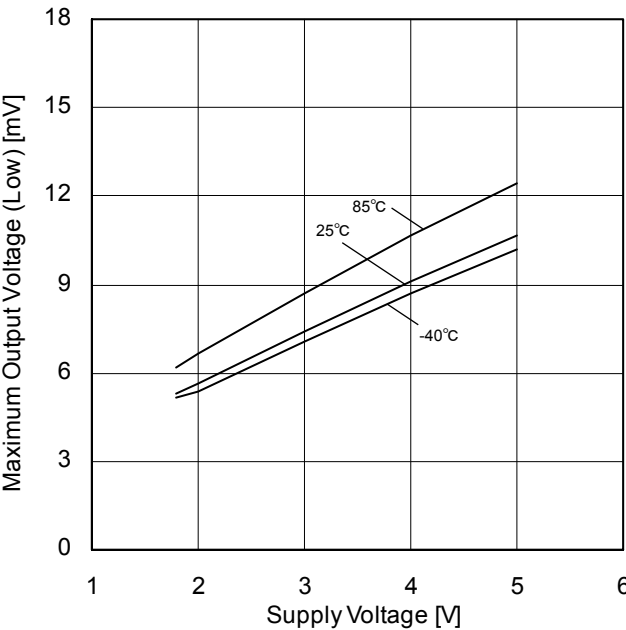


Figure 59.
Maximum Output Voltage (Low) vs Supply Voltage
($R_L=20k\Omega$)

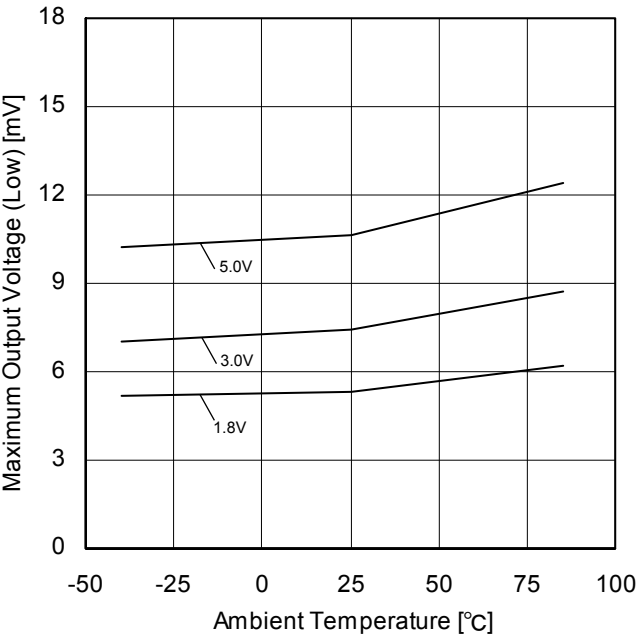


Figure 60.
Maximum Output Voltage (Low) vs Ambient Temperature
($R_L=20k\Omega$)

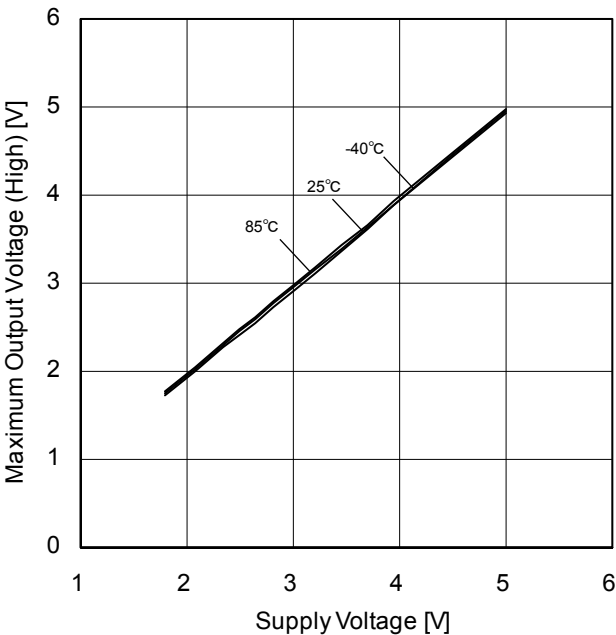


Figure 61.
Maximum Output Voltage (High) vs Supply Voltage
($R_L=2k\Omega$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12734xxx

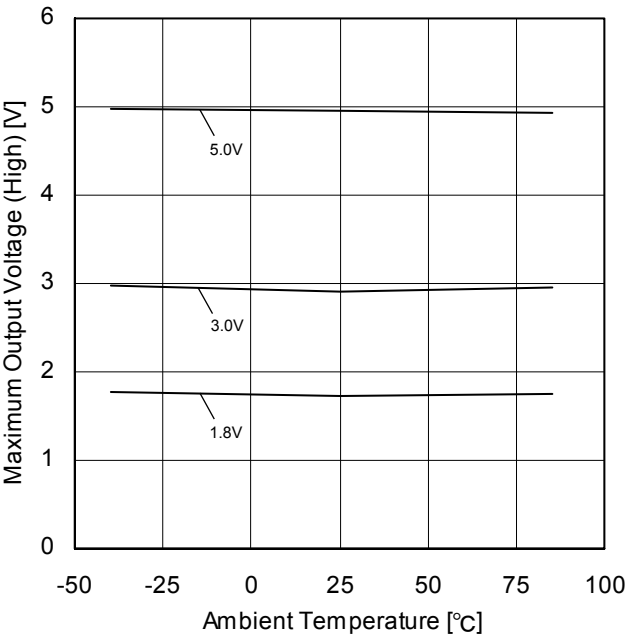


Figure 62.
Maximum Output Voltage (High) vs Ambient Temperature
($R_L=2k\Omega$)

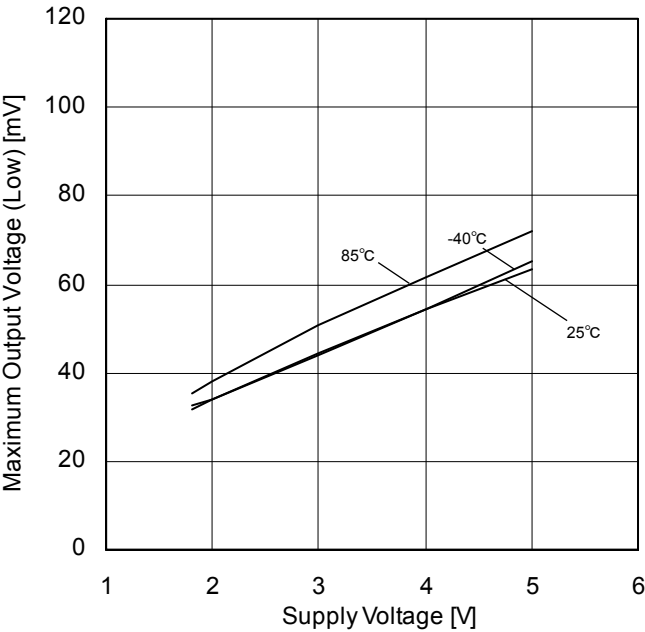


Figure 63.
Maximum Output Voltage (Low) vs Supply Voltage
($R_L=2k\Omega$)

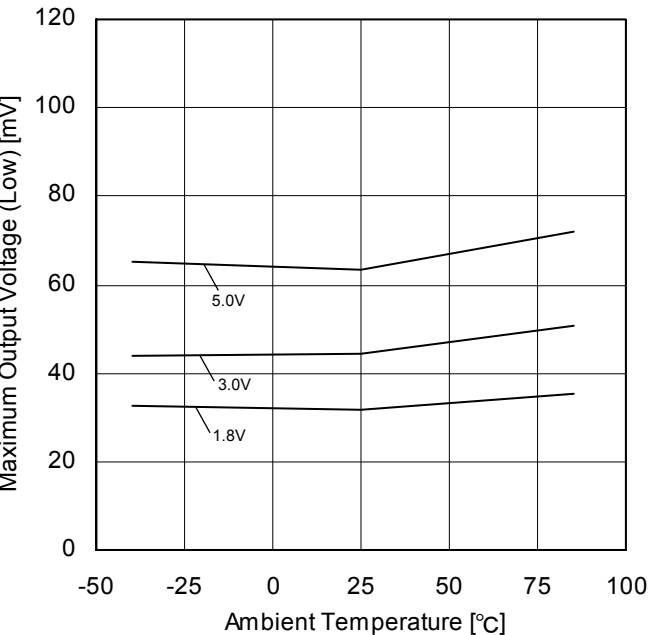


Figure 64.
Maximum Output Voltage (Low) vs Ambient Temperature
($R_L=2k\Omega$)

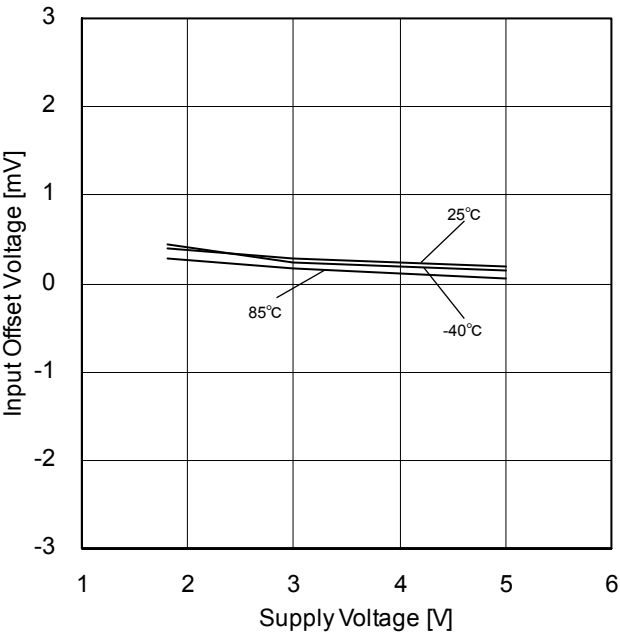


Figure 65.
Input Offset Voltage vs Supply Voltage

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12734xxx

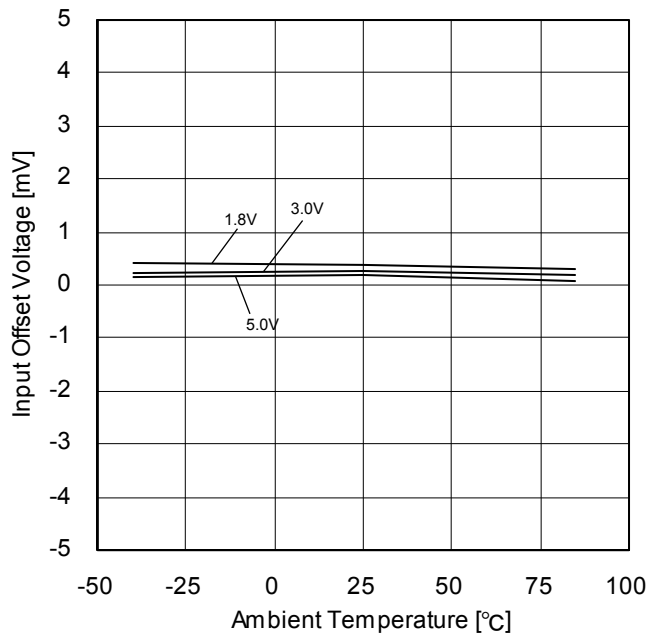


Figure 66.
Input Offset Voltage vs Ambient Temperature

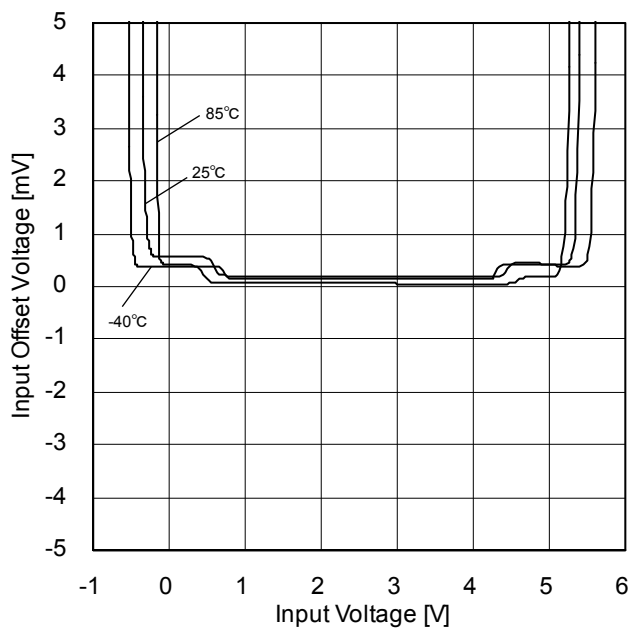


Figure 67.
Input Common Mode Voltage Range
(V+=5V)

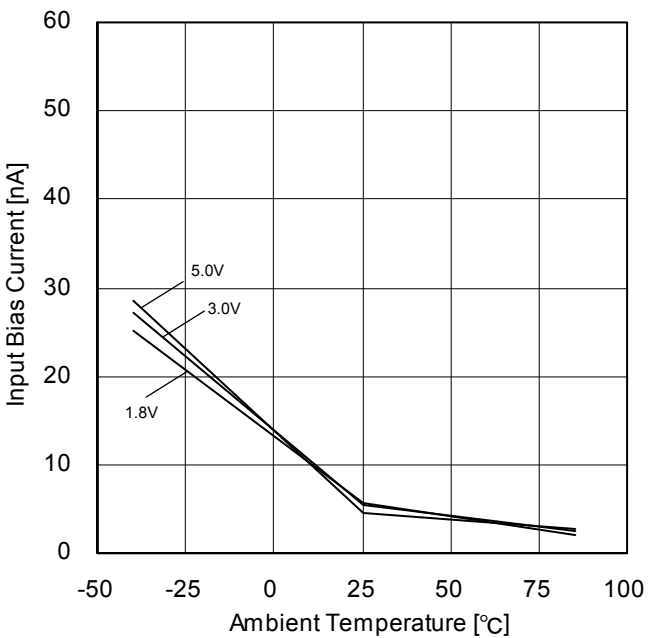


Figure 68.
Input Bias Current vs Ambient Temperature

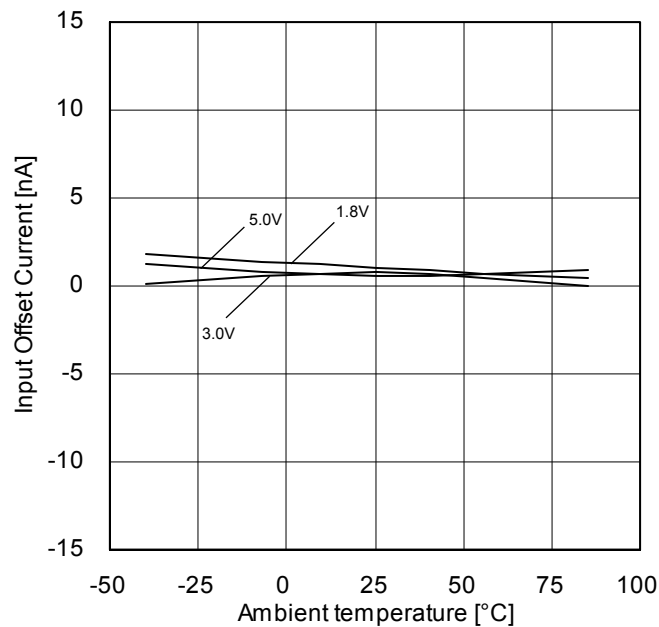


Figure 69.
Input Offset Current vs Ambient Temperature

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued

OBD12734xxx

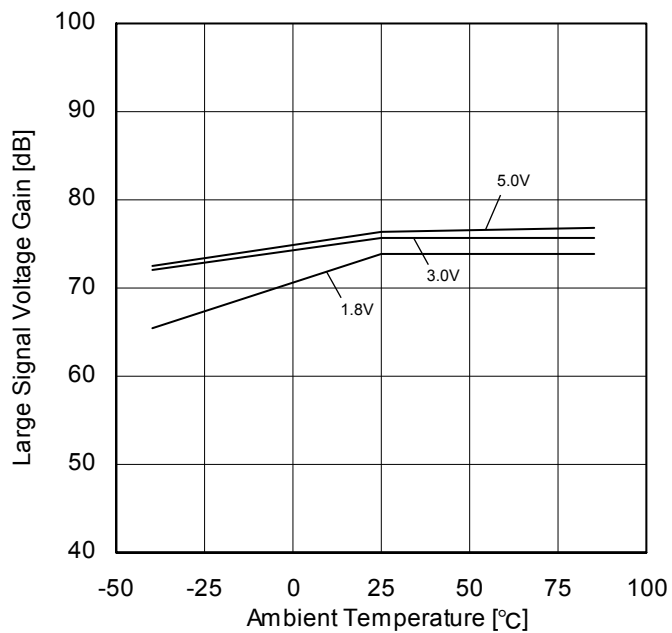


Figure 70.
Large Signal Voltage Gain vs Ambient Temperature
($R_L=2k\Omega$)

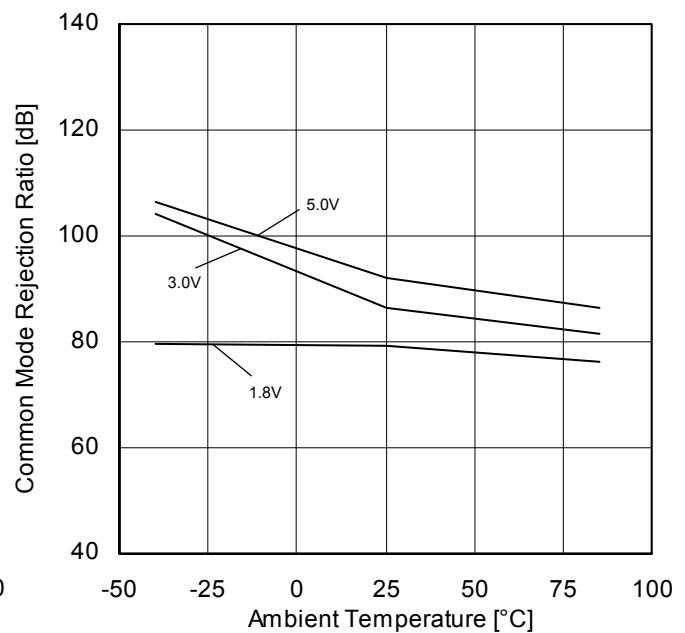


Figure 71.
Common Mode Rejection Ratio vs Ambient Temperature

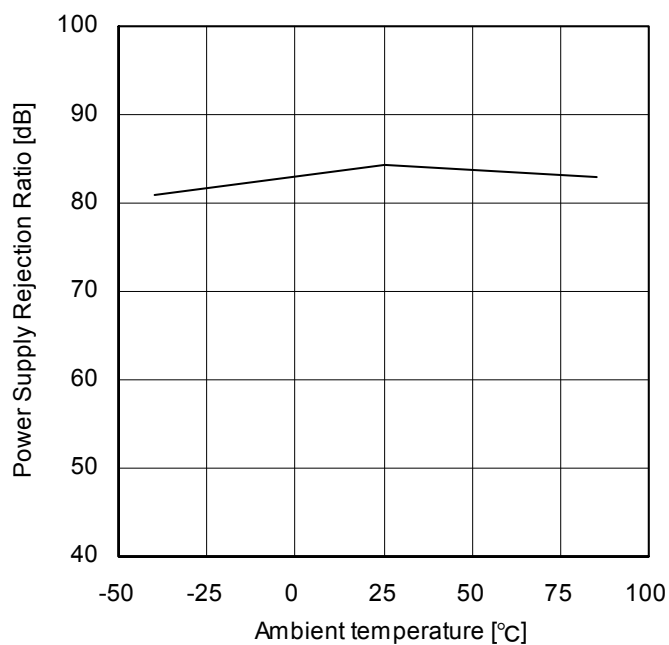


Figure 72.
Power Supply Rejection Ratio vs Ambient Temperature
($V_+=1.8V$ to $5.0V$)

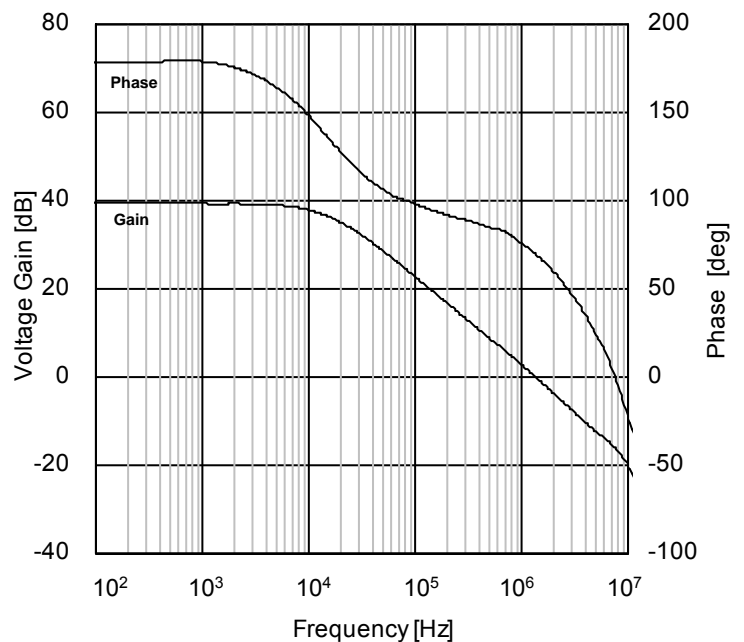


Figure 73.
Voltage Gain · Phase vs Frequency
($V_+=5V$, $R_L=2k\Omega$, $T_A=25^\circ C$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued

OBD12734xxx

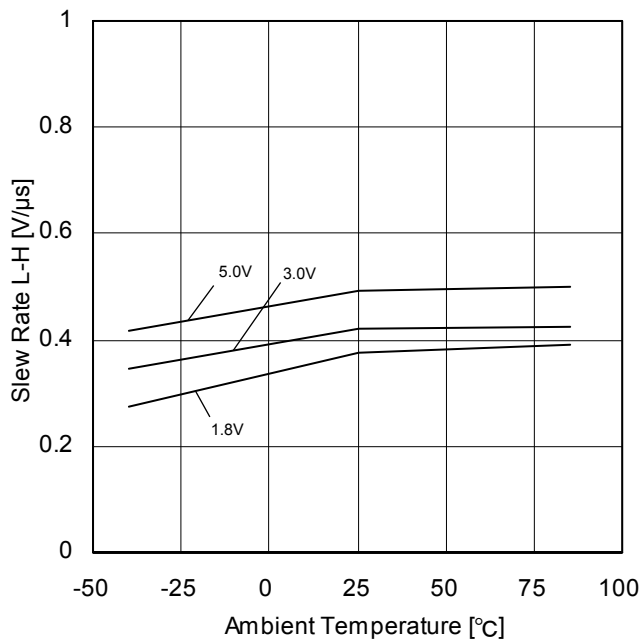


Figure 74.
Slew Rate L-H vs Ambient Temperature
($R_L=2k\Omega$)

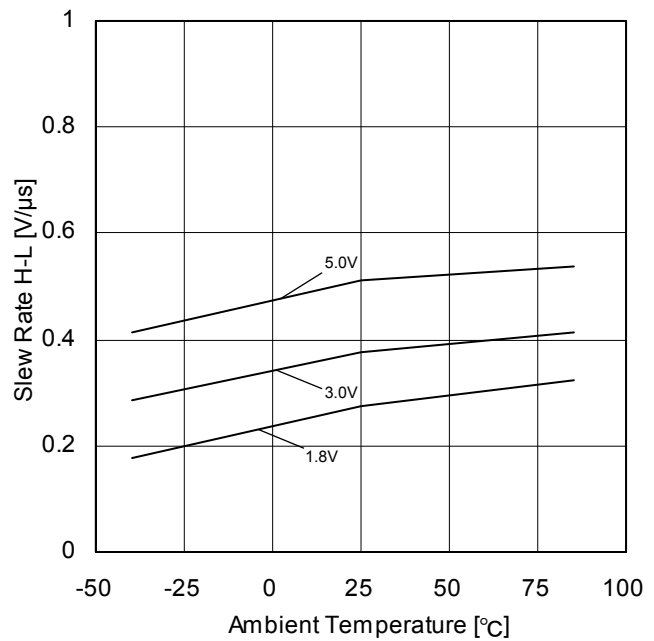


Figure 75.
Slew Rate H-L vs Ambient Temperature
($R_L=2k\Omega$)

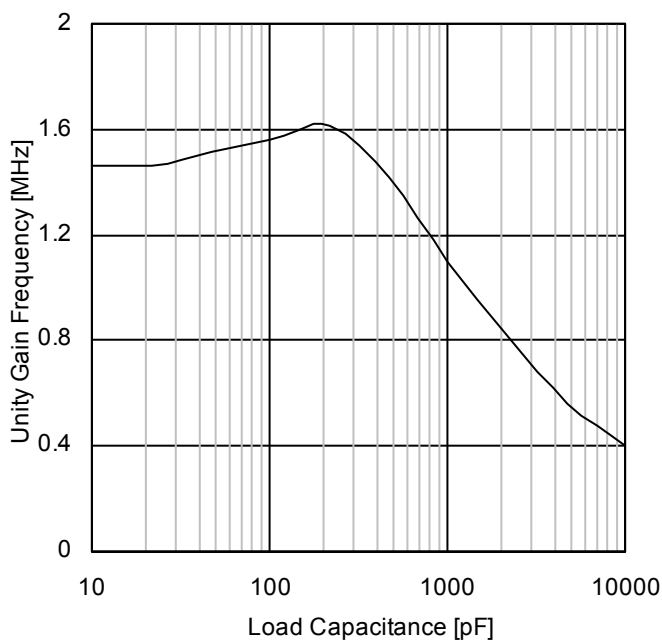


Figure 76.
Unity Gain Frequency vs Load Capacitance
($V_+=5V$, $T_A=25^\circ C$)

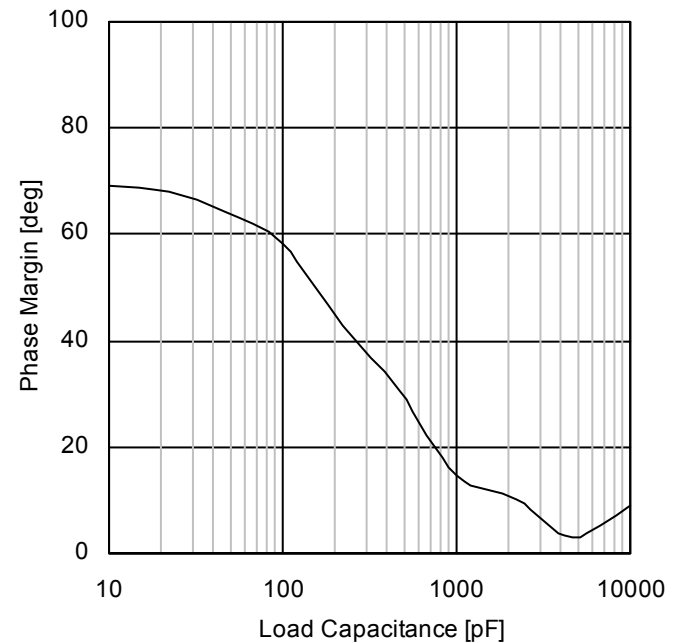


Figure 77.
Phase Margin vs Load Capacitance
($V_+=5V$, $T_A=25^\circ C$)

(*)The data above are measurement values of typical sample, it is not guaranteed.

Typical Performance Curves – Continued
OBD12734xxx

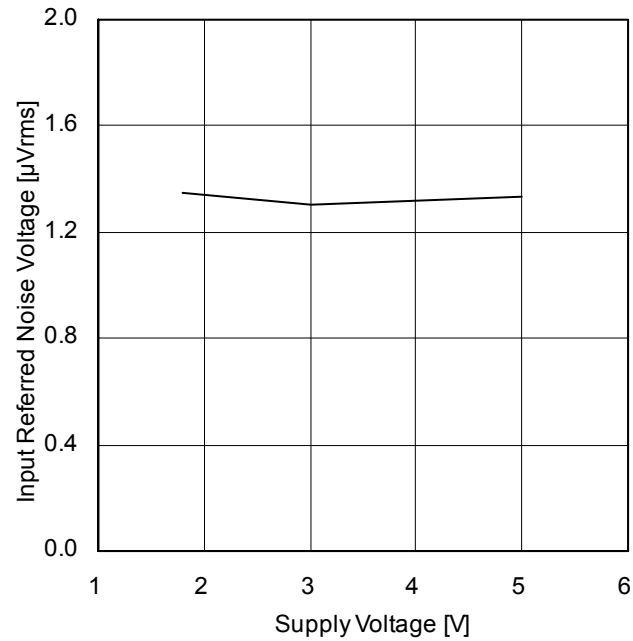


Figure 78.
Input Referred Noise Voltage vs Supply Voltage
(T_A=25°C)

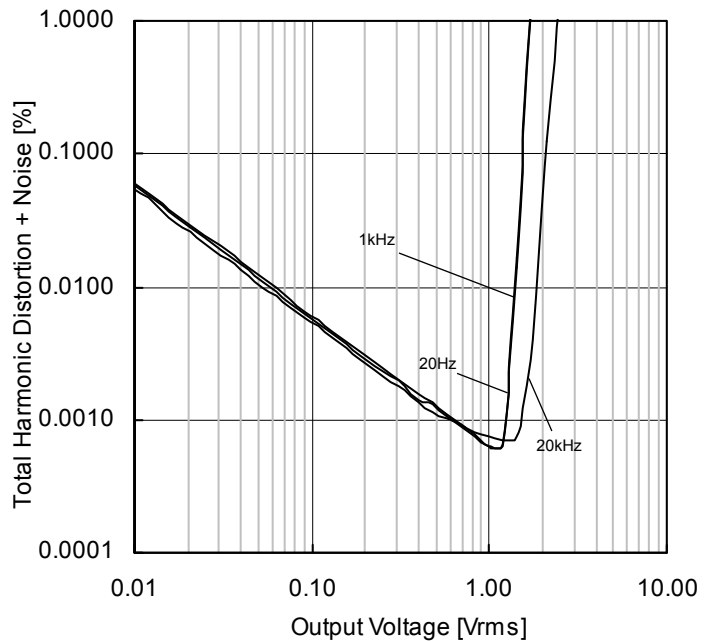


Figure 79.
Total Harmonic Distortion + Noise vs Output Voltage
(V₊=5V, R_L=2kΩ, T_A=25°C)

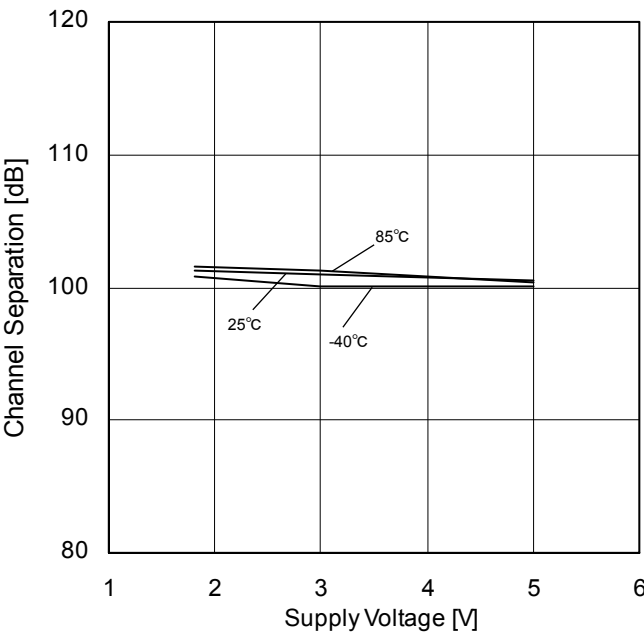


Figure 80.
Channel Separation vs Supply Voltage

(*)The data above are measurement values of typical sample, it is not guaranteed.

Application Information

NULL method condition for Test Circuit 1

V₊, GND, V_{RL}, E_K, V_{ICM} Unit: V

Parameter	V _F	S1	S2	S3	V ₊	GND	V _{RL}	R _L Ω	E _K	V _{ICM}	Calculation
Input Offset Voltage	V _{F1}	ON	ON	OFF	5.0	0	-	open	-2.5	2.5	1
Large Signal Voltage Gain	V _{F2}	ON	ON	ON	5.0	0	2.5	2k	-4.5	2.5	2
	V _{F3}								-0.5		
Common Mode Rejection Ratio (Input Common-mode Voltage Range)	V _{F4}	ON	ON	OFF	5.0	0	-	open	-2.5	0	3
	V _{F5}								-2.5	5.0	
Power Supply Rejection Ratio	V _{F6}	ON	ON	OFF	5.0	0	-	open	-0.9	0.9	4
	V _{F7}				1.8						

— Calculation —

1. Input Offset Voltage (V_{IO})
$$V_{IO} = \frac{|V_{F1}|}{1+R_F/R_S} \quad [V]$$

2. Large Signal Voltage Gain (A_v)
$$A_v = 20\text{Log} \frac{\Delta E_K \times (1+R_F/R_S)}{|V_{F2}-V_{F3}|} \quad [\text{dB}]$$

3. Common-mode Rejection Ratio (CMRR)
$$\text{CMRR} = 20\text{Log} \frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F4} - V_{F5}|} \quad [\text{dB}]$$

4. Power Supply Rejection Ratio (PSRR)
$$\text{PSRR} = 20\text{Log} \frac{\Delta V_+ \times (1+R_F/R_S)}{|V_{F6} - V_{F7}|} \quad [\text{dB}]$$

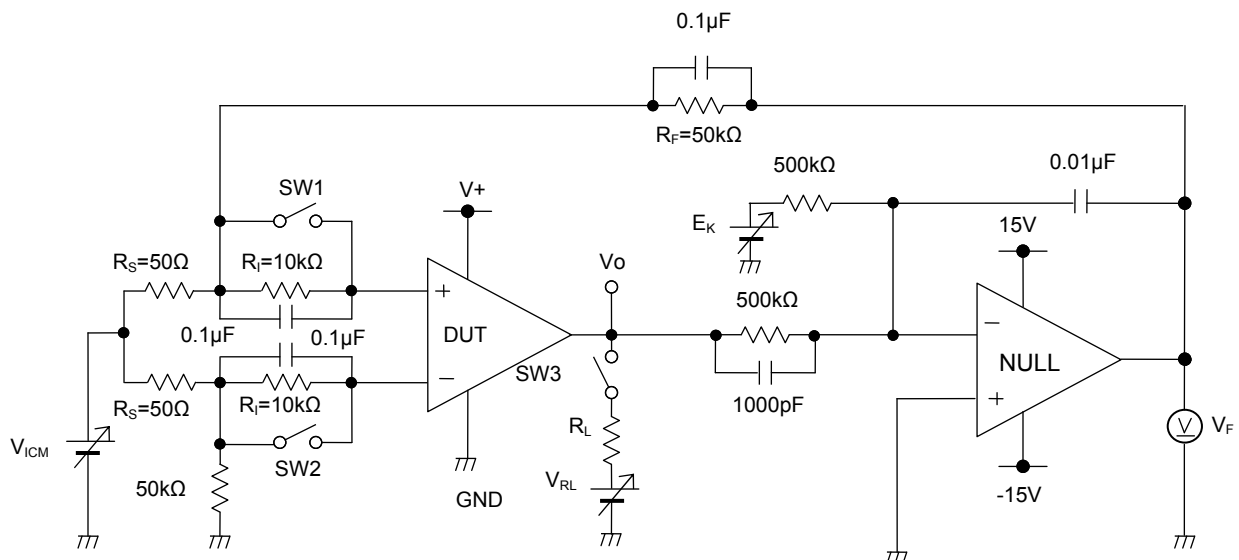


Figure 81. Test Circuit 1

Application Information – continued
Switch Condition for Test Circuit 2

SW No.	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage $R_L=10k\Omega$	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON
Unity Gain Frequency	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON

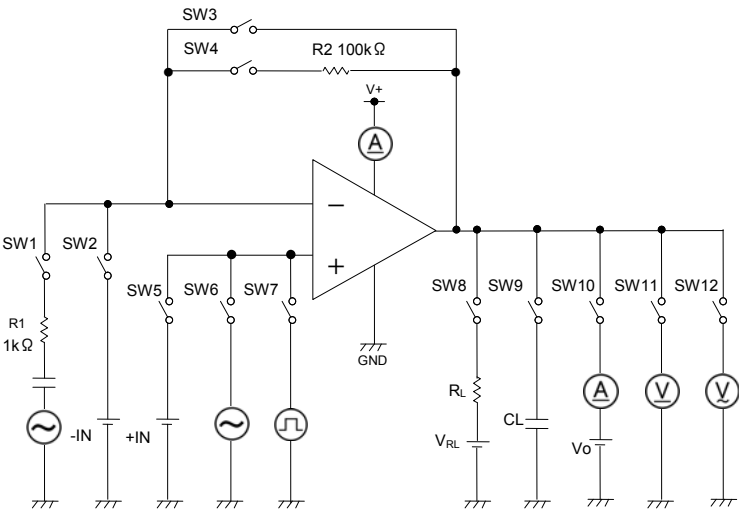


Figure 82. Test Circuit 2

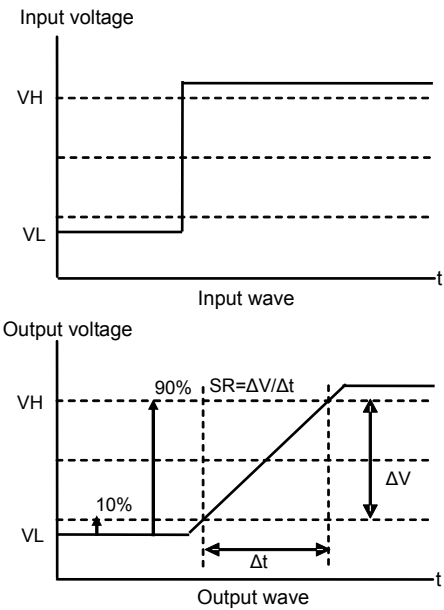


Figure 83. Slew Rate Input Output Wave

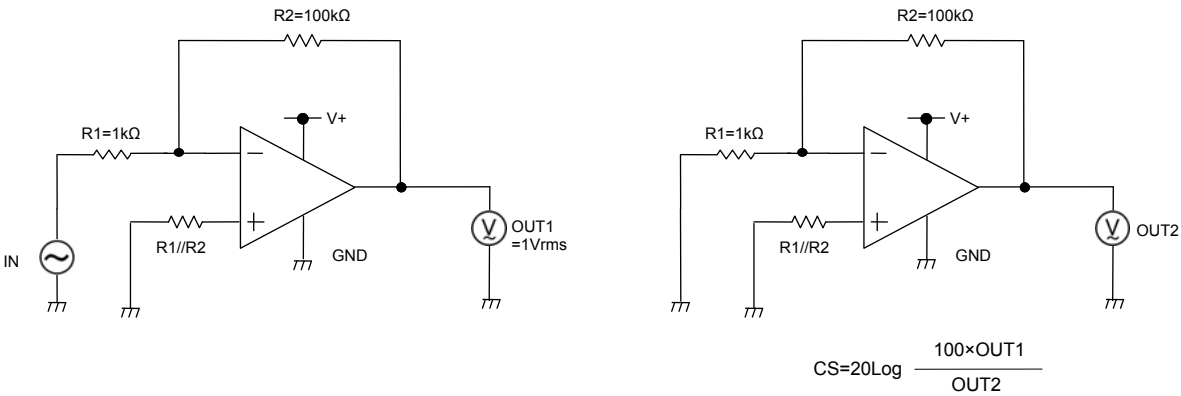


Figure 84. Test Circuit 3 (Channel separation)

Application Example

○Voltage follower

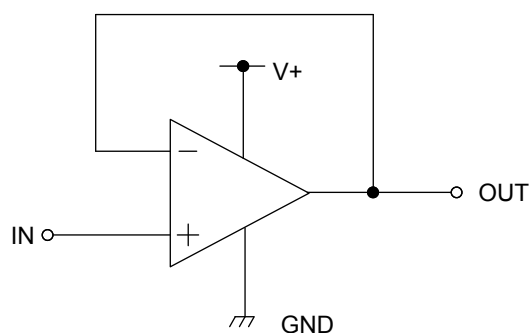


Figure 85. Voltage Follower

Voltage gain is 0dB.

Using this circuit, the output voltage (OUT) is configured to be equal to the input voltage (IN). This circuit also stabilizes the output voltage (OUT) due to high input impedance and low output impedance. Computation for output voltage (OUT) is shown below.

$$OUT=IN$$

○Inverting amplifier

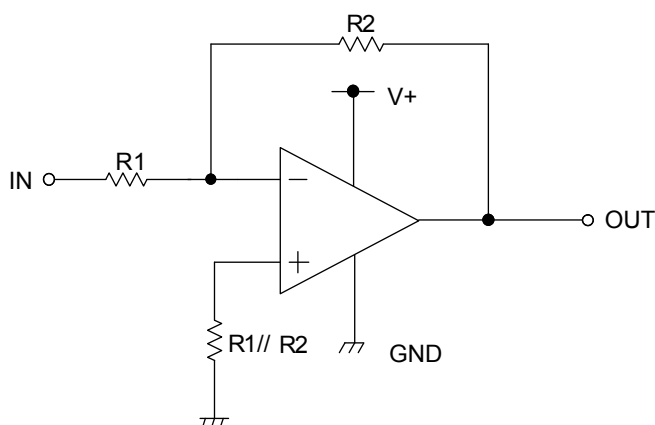


Figure 86. Inverting Amplifier Circuit

For inverting amplifier, input voltage (IN) is amplified by a voltage gain and depends on the ratio of R1 and R2. The out-of-phase output voltage is shown in the next expression

$$OUT=-(R2/R1) \cdot IN$$

This circuit has input impedance equal to R1.

○Non-inverting amplifier

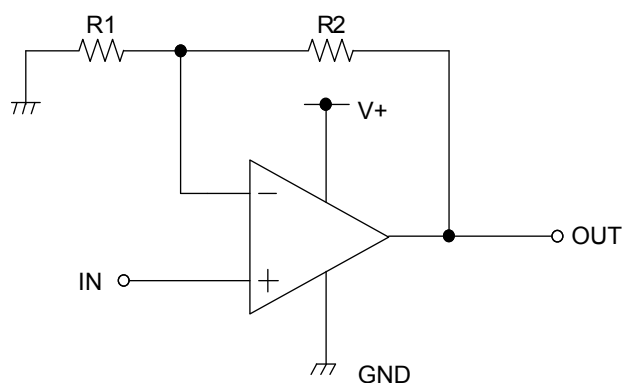


Figure 87. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (IN) is amplified by a voltage gain, which depends on the ratio of R1 and R2. The output voltage (OUT) is -INphase with the input voltage (IN) and is shown in the next expression.

$$OUT=(1 + R2/R1) \cdot IN$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

Power Dissipation

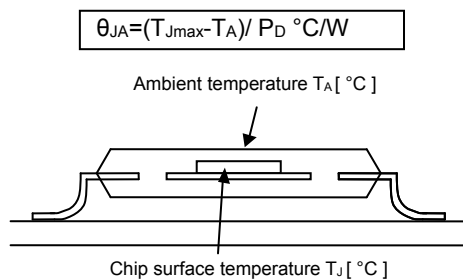
Power dissipation (total loss) indicates the power that the IC can consume at $T_A=25^{\circ}\text{C}$ (normal temperature). As the IC consumes power, it heats up, causing its temperature to be higher than the ambient temperature. The allowable temperature that the IC can accept is limited. This depends on the circuit configuration, manufacturing process, and consumable power.

Power dissipation is determined by the allowable temperature within the IC (maximum junction temperature) and the thermal resistance of the package used (heat dissipation capability). Maximum junction temperature is typically equal to the maximum storage temperature. The heat generated through the consumption of power by the IC radiates from the mold resin or lead frame of the package. Thermal resistance, represented by the symbol $\theta_{JA}^{\circ}\text{C/W}$, indicates this heat dissipation capability. Similarly, the temperature of an IC inside its package can be estimated by thermal resistance.

Figure 88(a) shows the model of the thermal resistance of a package. The equation below shows how to compute for the Thermal resistance (θ_{JA}), given the ambient temperature (T_A), maximum junction temperature (T_{Jmax}), and power dissipation (P_D).

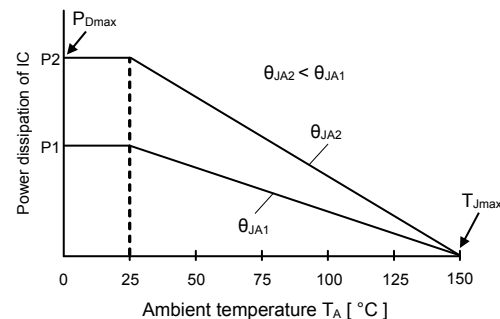
$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad ^{\circ}\text{C/W}$$

The Derating curve in Figure 88(b) indicates the power that the IC can consume with reference to ambient temperature. Power consumption of the IC begins to attenuate at certain temperatures. This gradient is determined by Thermal resistance (θ_{JA}), which depends on the chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc. This may also vary even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 88(c) to (f) shows an example of the derating curve for BD12730G, BD12732xxx and BD12734xxx.

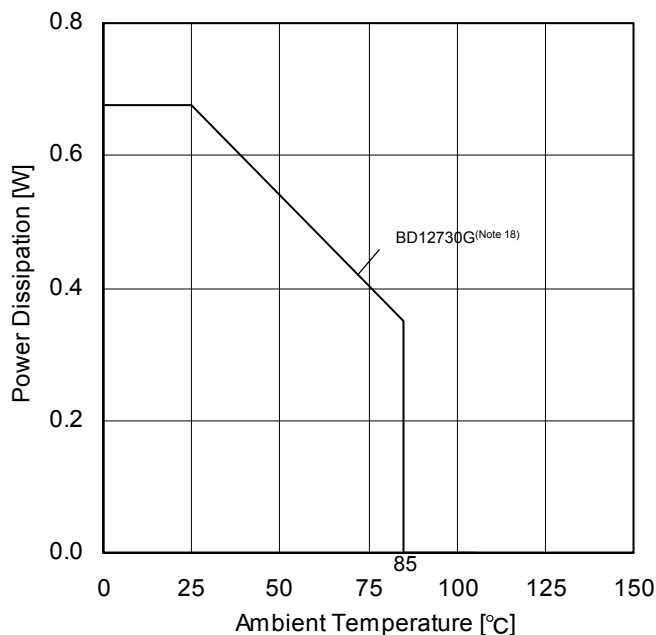


(a) Thermal Resistance

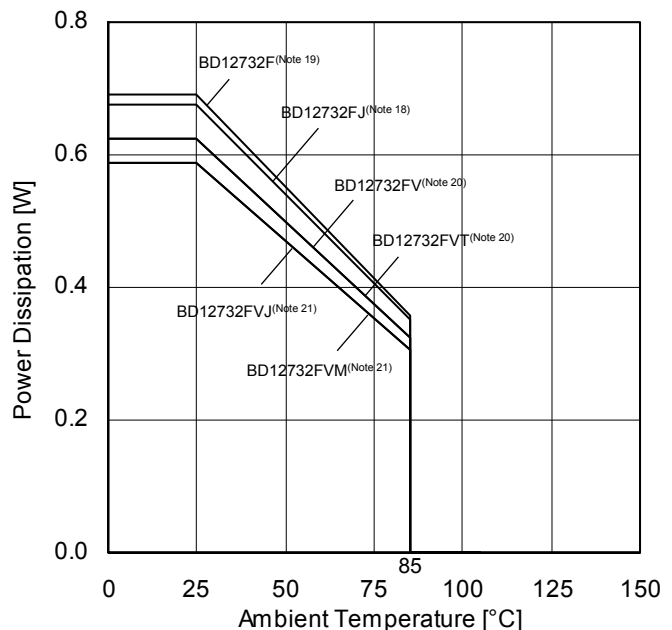
Power dissipation of LSI [W]



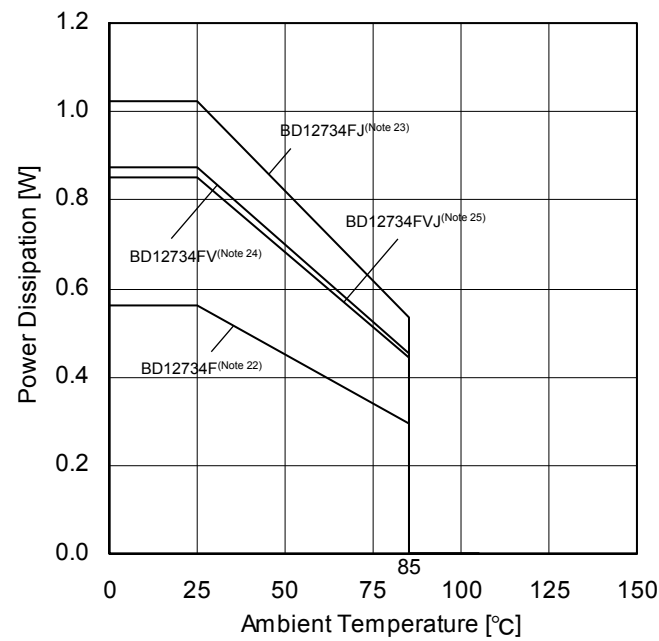
(b) Derating Curve



(c) BD12730G



(d) BD12732xxx



(e) BD12734xxx

(Note 18)	(Note 19)	(Note 20)	(Note 21)	(Note 22)	(Note 23)	(Note 24)	(Note 25)	Unit
5.4	5.5	5.0	4.7	4.5	8.2	7.0	6.8	mW/°C

When using the unit above $T_A=25^{\circ}\text{C}$, subtract the value above per $^{\circ}\text{C}$. Permissible dissipation is the value when FR4 glass epoxy board $70\text{mm} \times 70\text{mm} \times 1.6\text{mm}$ (copper foil area below 3%) is mounted

Figure 88. Thermal Resistance and Derating Curve

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the P_D stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the P_D rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So, unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

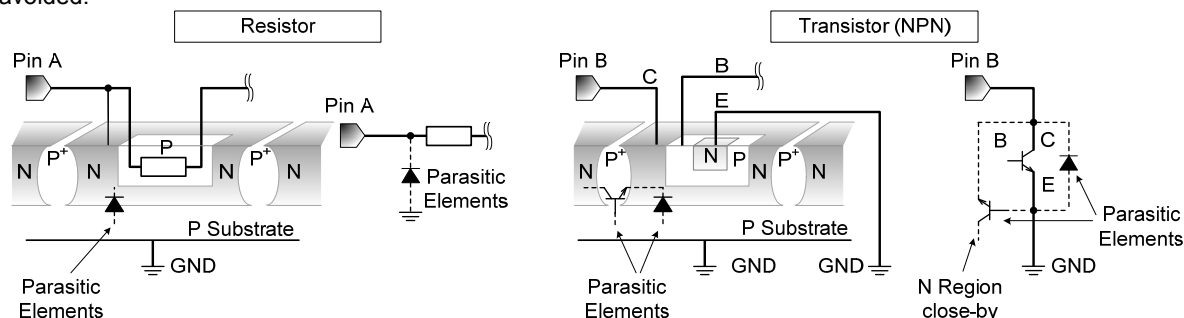


Figure 89. Example of monolithic IC structure

13. Applied voltage to the input terminal

For normal circuit operation of voltage comparator, please input voltage for its input terminal within input common mode voltage $V_{+} + 0.3V$. Then, regardless of power supply voltage, GND-0.3V can be applied to input terminals without deterioration or destruction of its characteristics.

14. Power supply (single / dual)

The operational amplifiers operate when the voltage supplied is between V_{+} and GND. Therefore, the single supply operational amplifiers can be used as dual supply operational amplifiers as well.

15. Power dissipation (P_d)

Using the unit in excess of the rated power dissipation may cause deterioration in electrical characteristics due to a rise in chip temperature, including reduced current capability. Therefore, please take into consideration the power dissipation (P_d) under actual operating conditions and apply a sufficient margin in thermal design. Refer to the thermal derating curves for more information.

16. IC handling

Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuations in the electrical characteristics due to piezo resistance effects.

17. The IC destruction caused by capacitive load

The transistors in circuits may be damaged when V_{+} terminal and GND terminal is shorted with the charged output terminal capacitor. When IC is used as an operational amplifier or as an application circuit, where oscillation is not activated by an output capacitor, the output capacitor must be kept below 0.1 μ F in order to prevent the damage mentioned above.

18. Latch up

Be careful in the application of input voltage that exceeds the V_{+} and GND. For CMOS device, sometimes latch up operation occurs. Also protect the IC from abnormal noise.

19. Decoupling capacitor

Insert a decoupling capacitor between V_{+} and GND for a stable operation of the operational amplifier.

Operational Notes – continued

20. Unused circuits

When there are unused Op-amps, it is recommended that they are connected as in Figure 90, setting the non-inverting input terminal to a potential within the Input Common-mode Voltage Range (V_{ICM}).

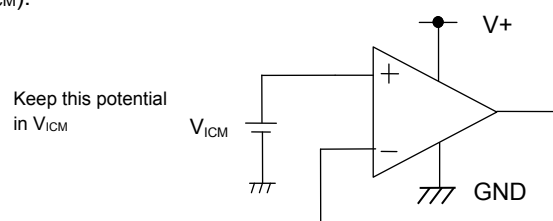
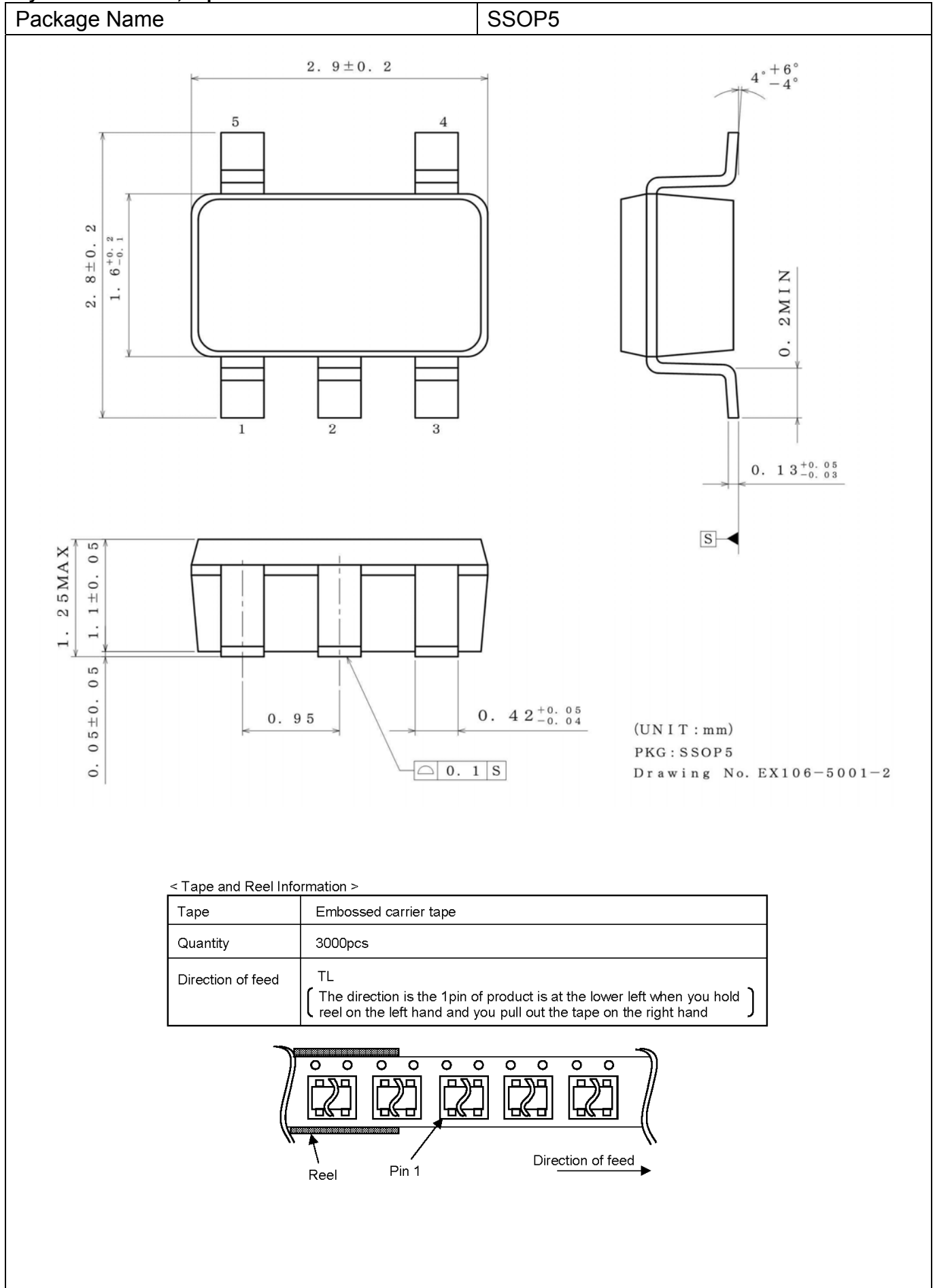
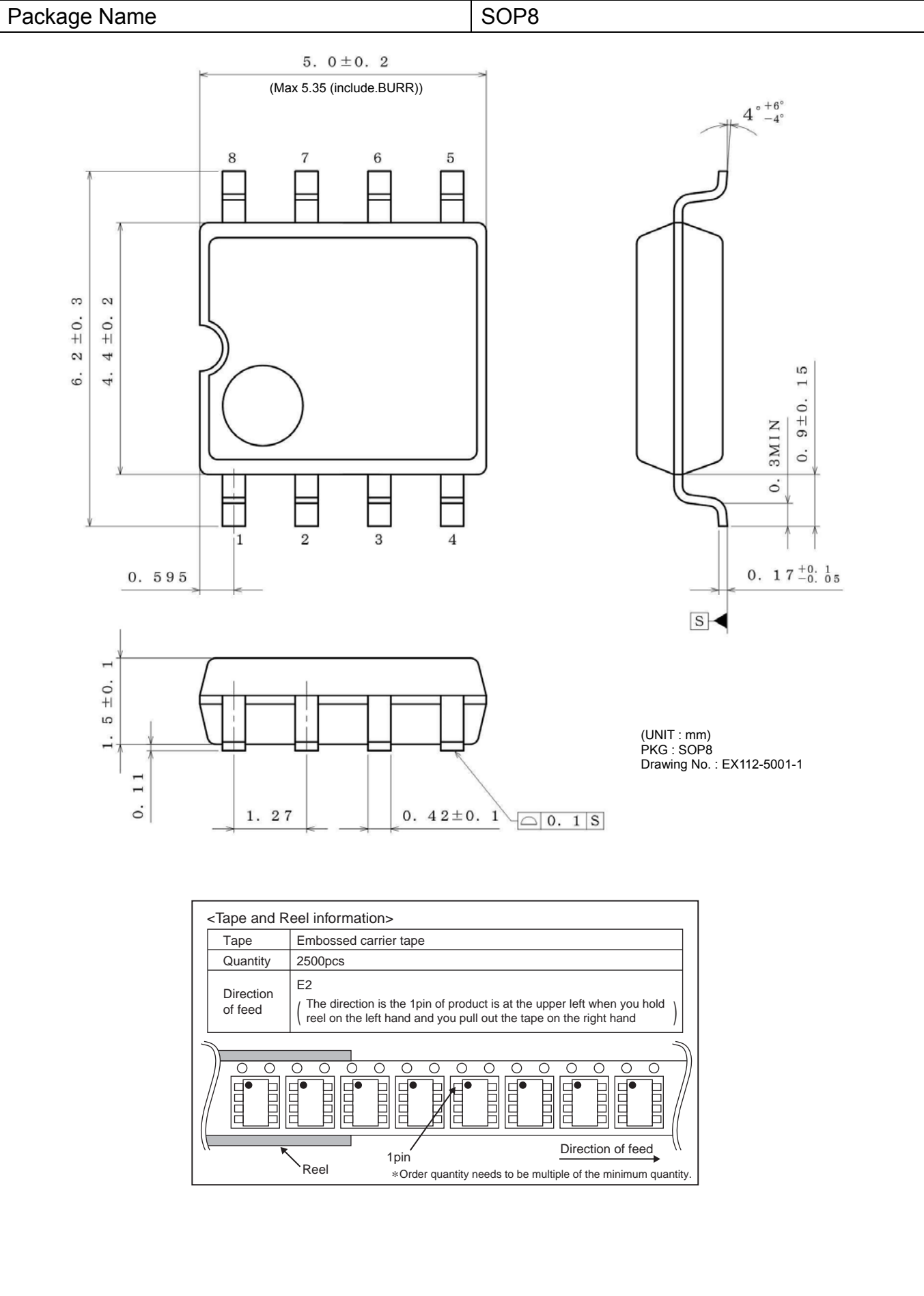


Figure 90. Example of Application Circuit for Unused Op-Amp

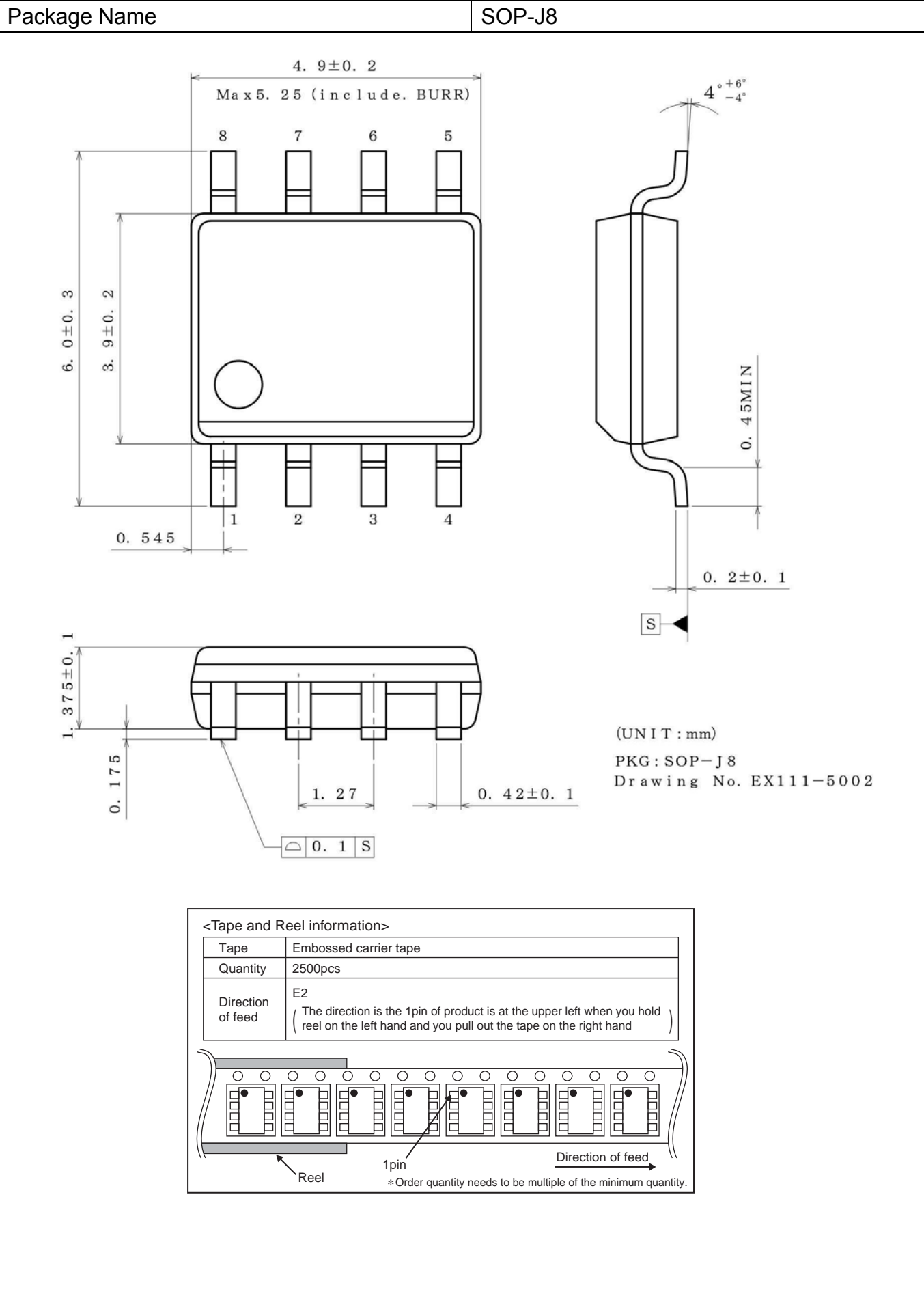
Physical Dimension, Tape and Reel Information



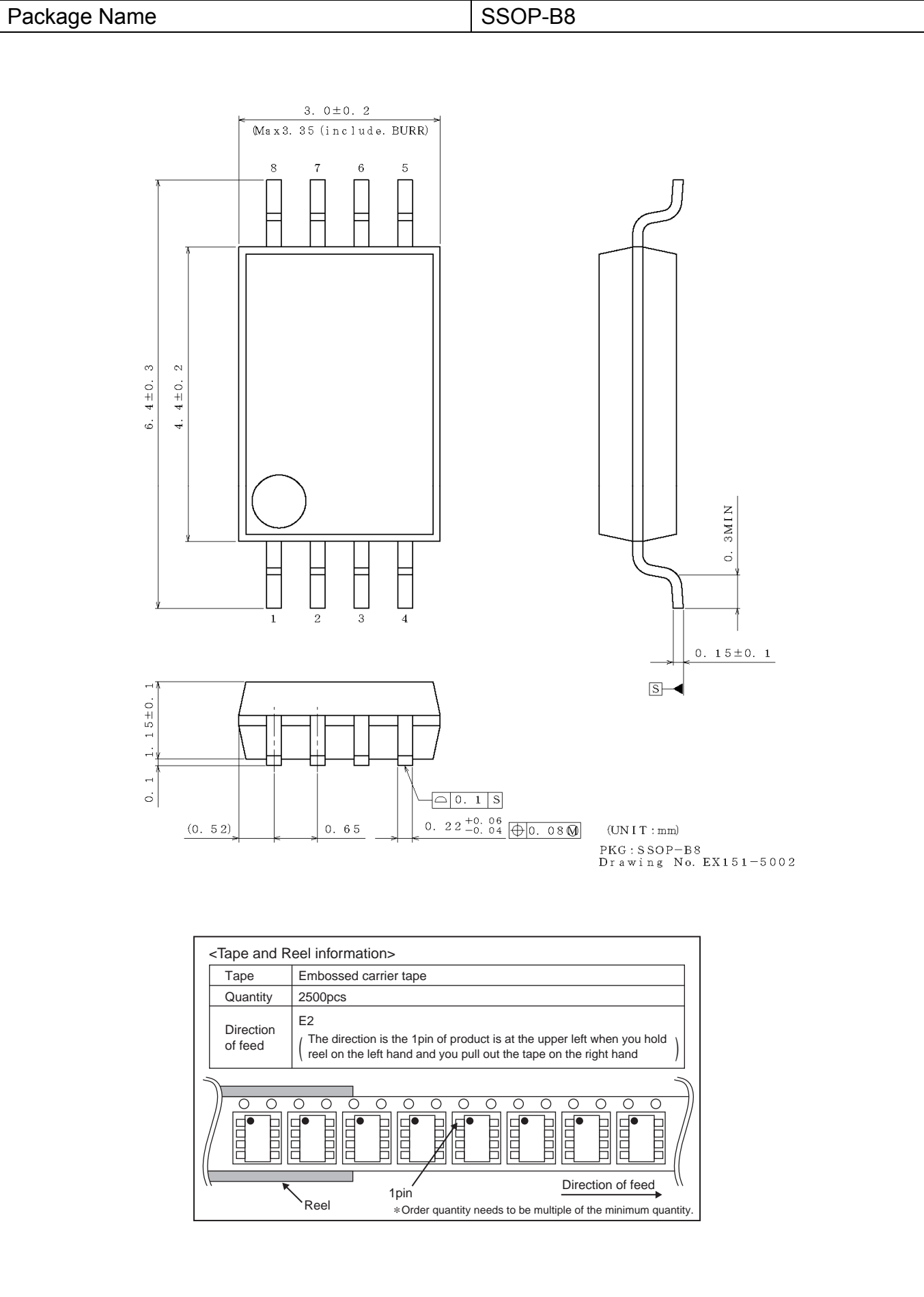
Physical Dimension, Tape and Reel Information - continued



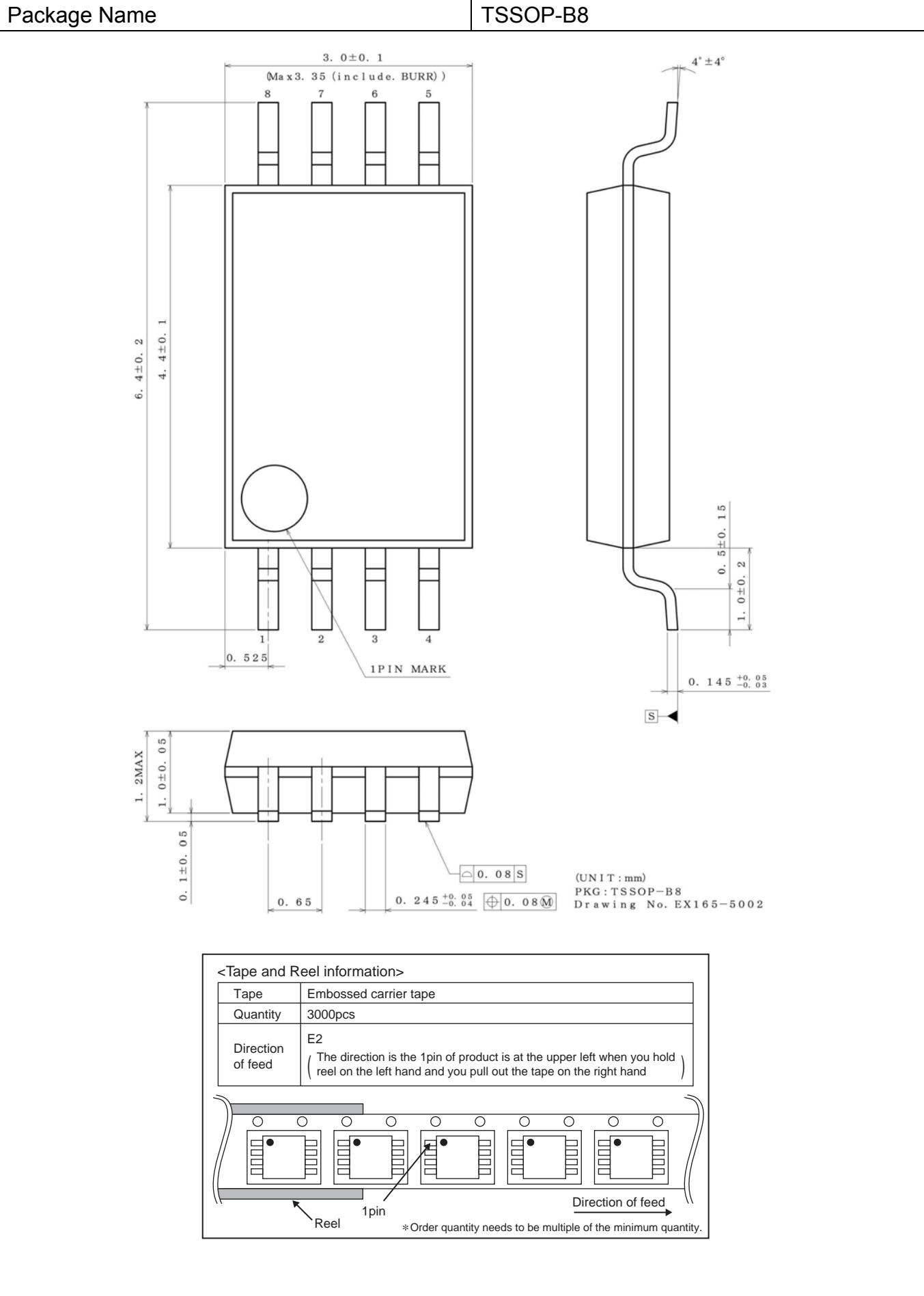
Physical Dimension, Tape and Reel Information - continued



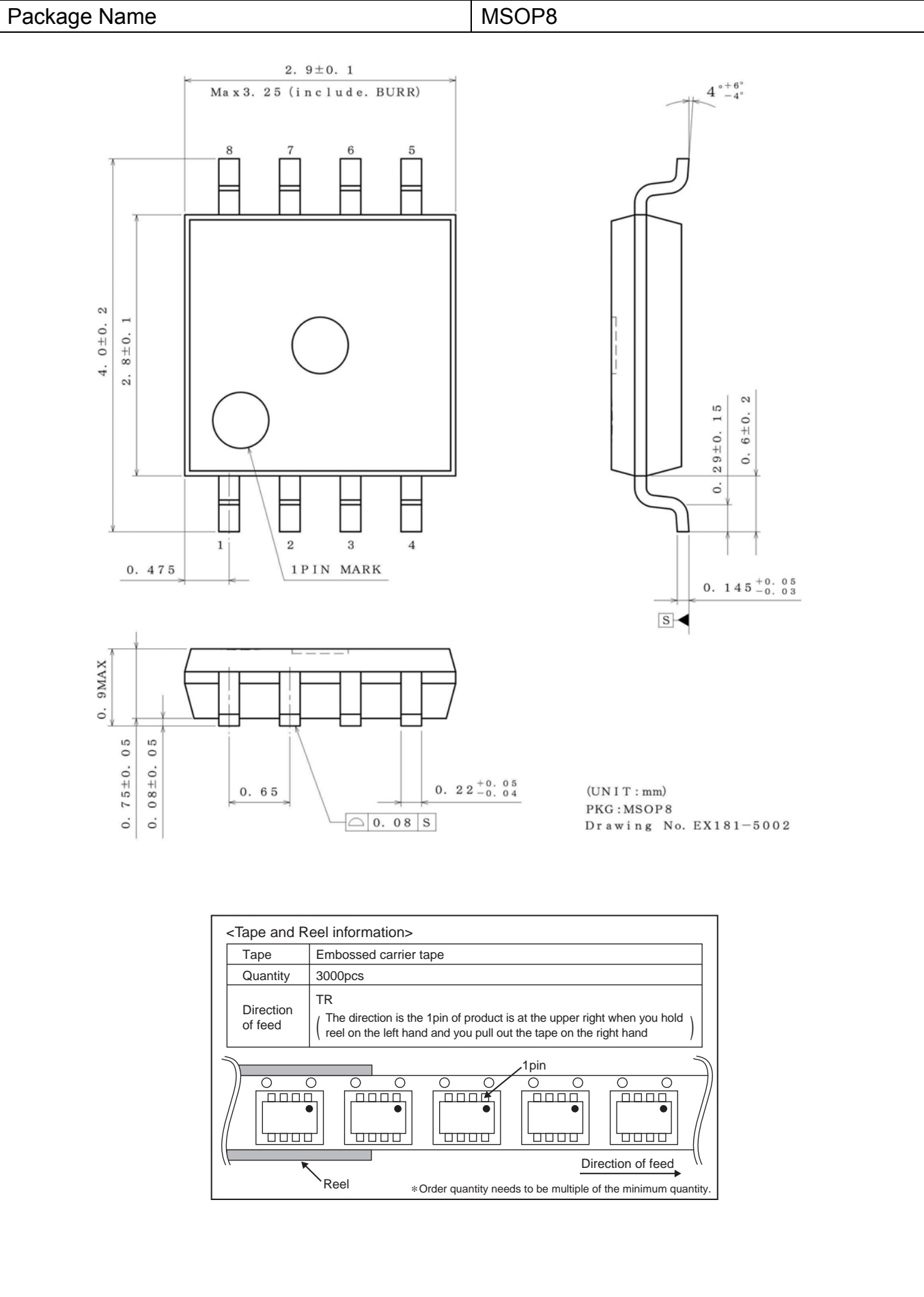
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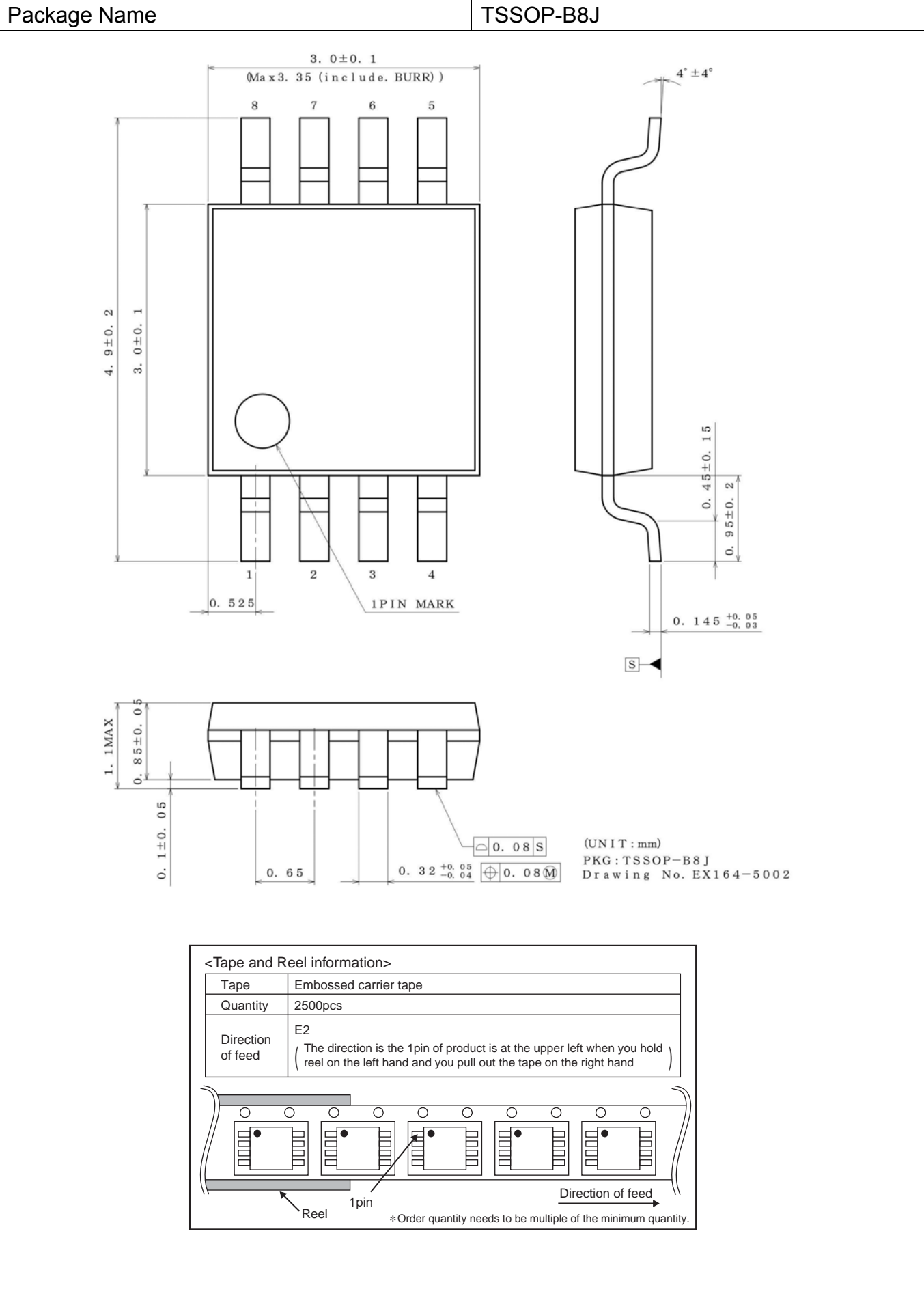
Physical Dimension, Tape and Reel Information - continued



Physical Dimension, Tape and Reel Information - continued

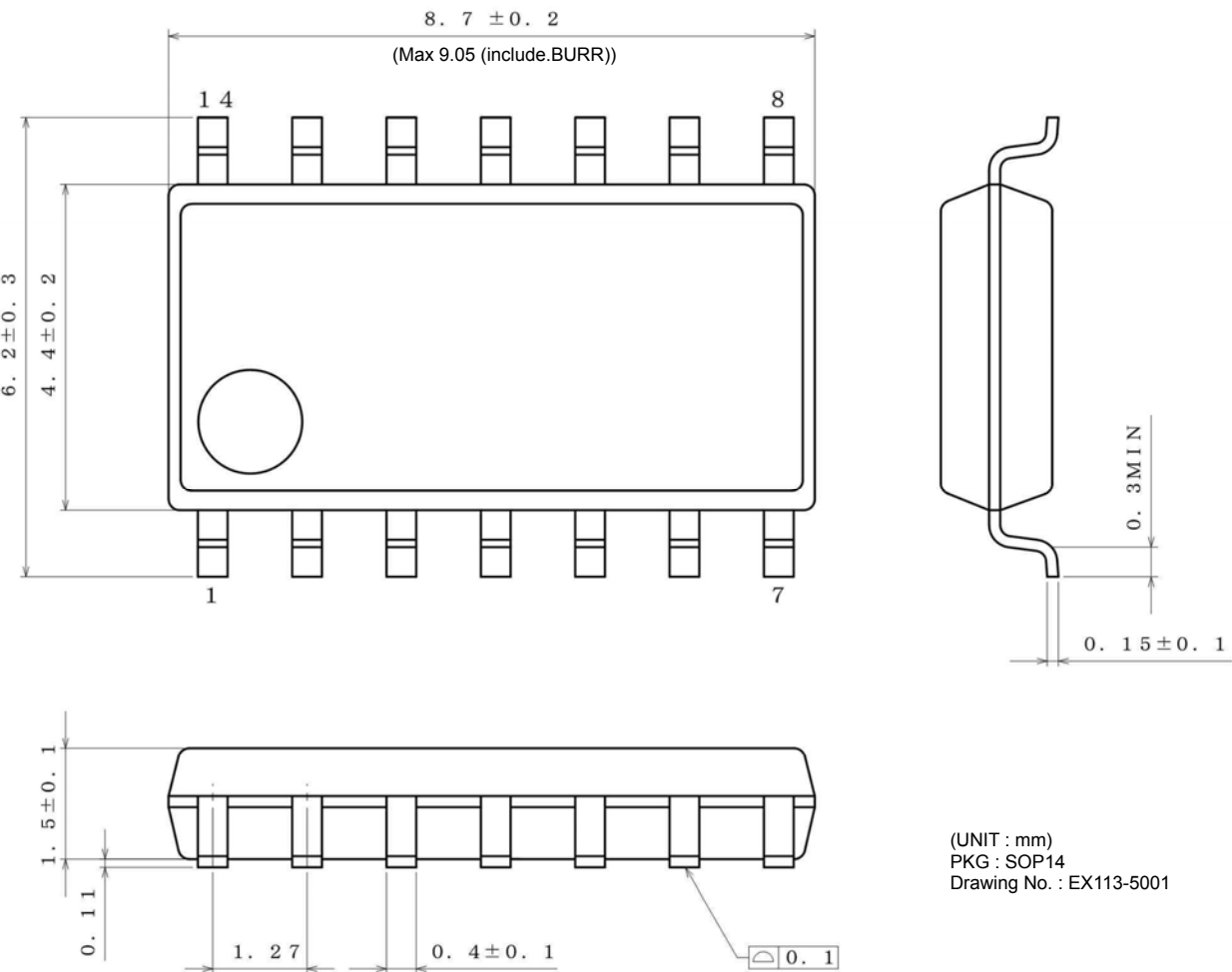


Physical Dimension, Tape and Reel Information - continued



Physical Dimension, Tape and Reel Information - continued

Package Name	SOP14
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<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Reel

1pin

Direction of feed

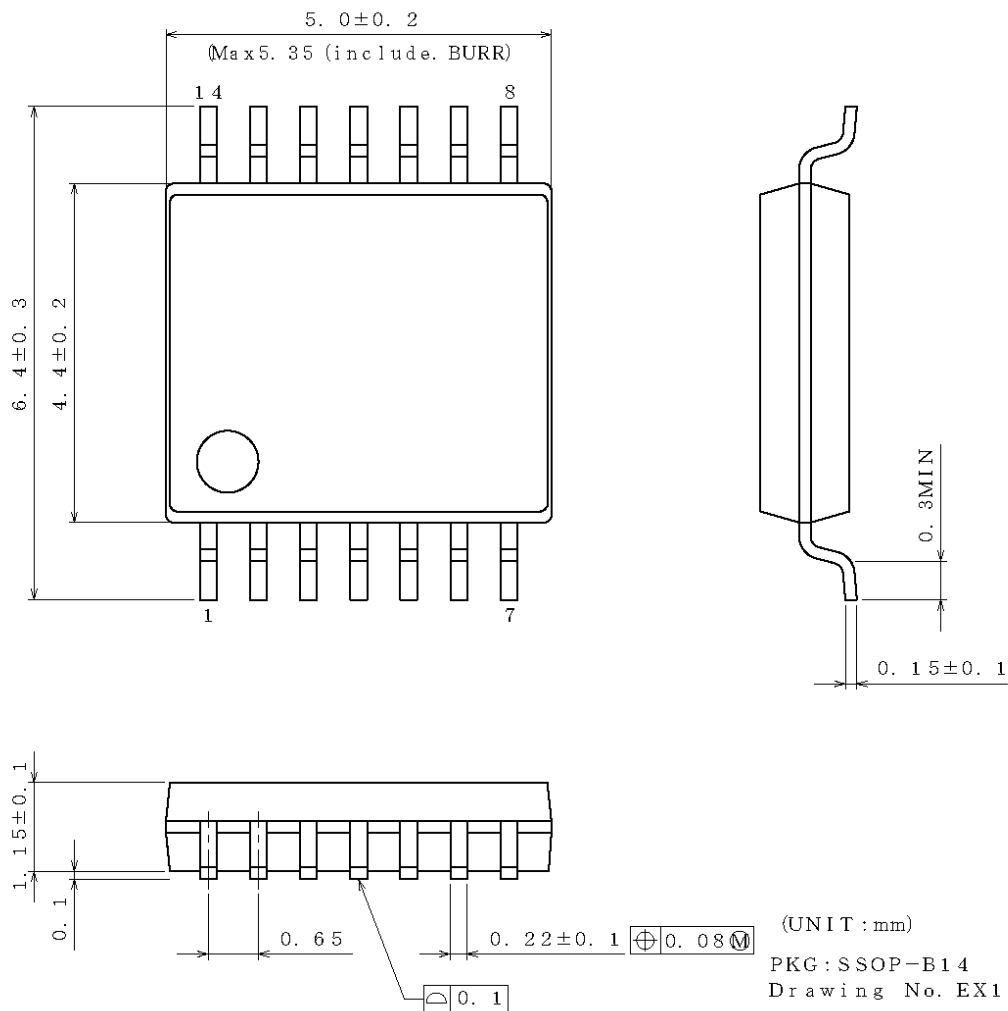
*Order quantity needs to be multiple of the minimum quantity.

Physical Dimension, Tape and Reel Information - continued

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Physical Dimension, Tape and Reel Information - continued

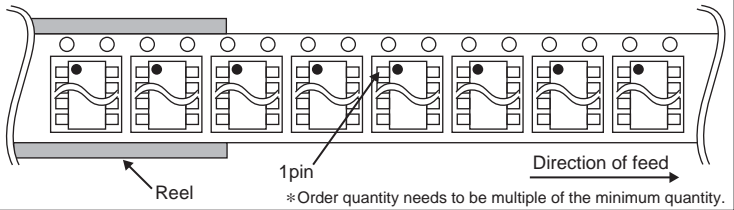
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PKG : SSOP-B14
Drawing No. EX152-5002

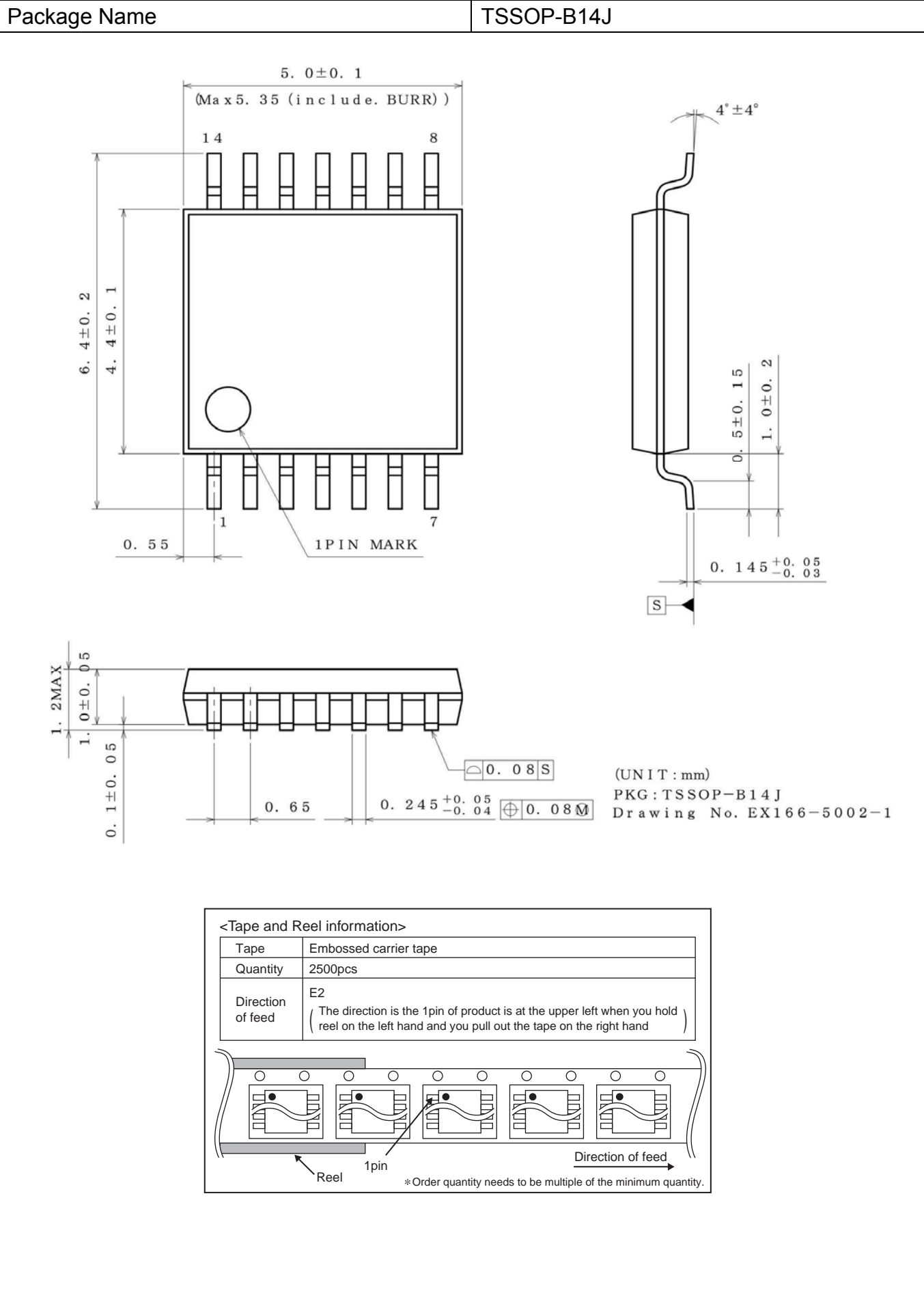
<Tape and Reel information>

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Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

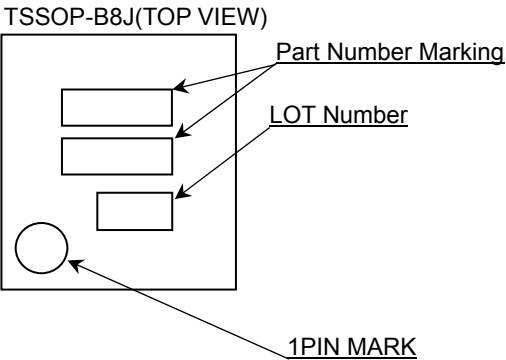
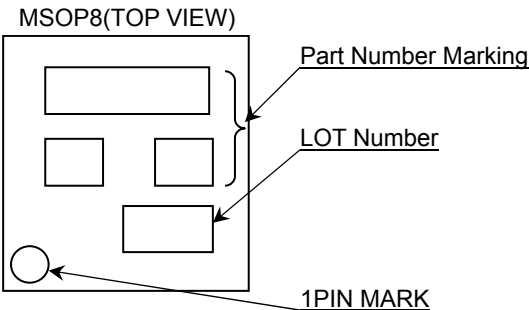
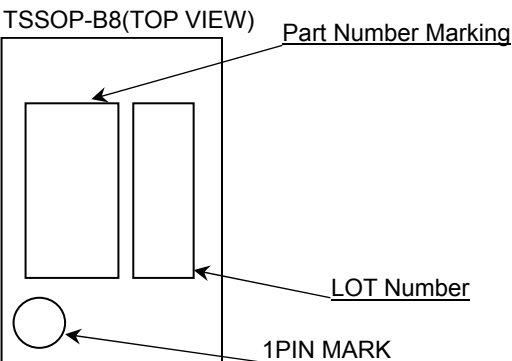
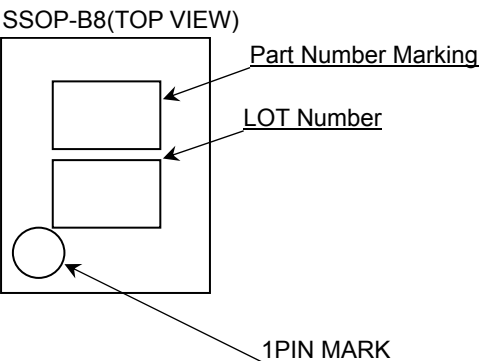
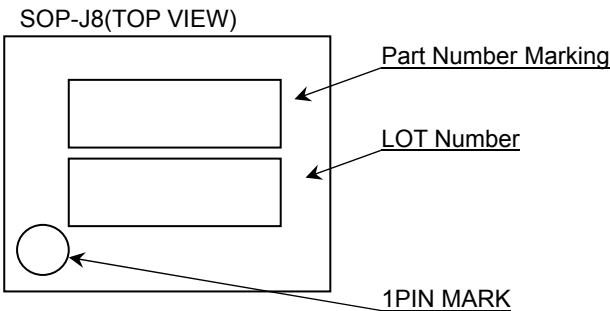
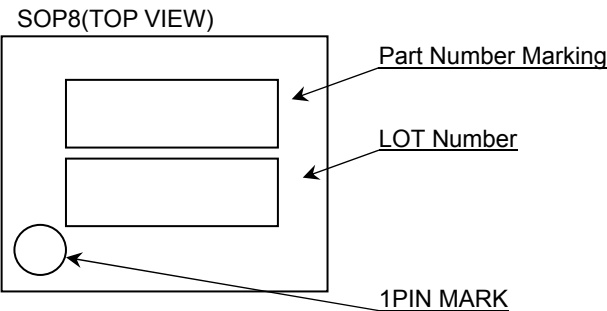
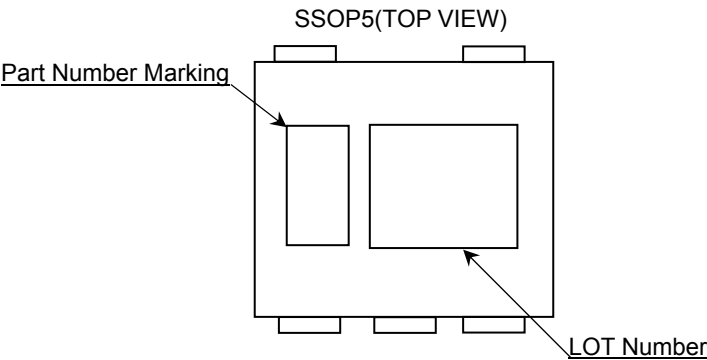


*Order quantity needs to be multiple of the minimum quantity.

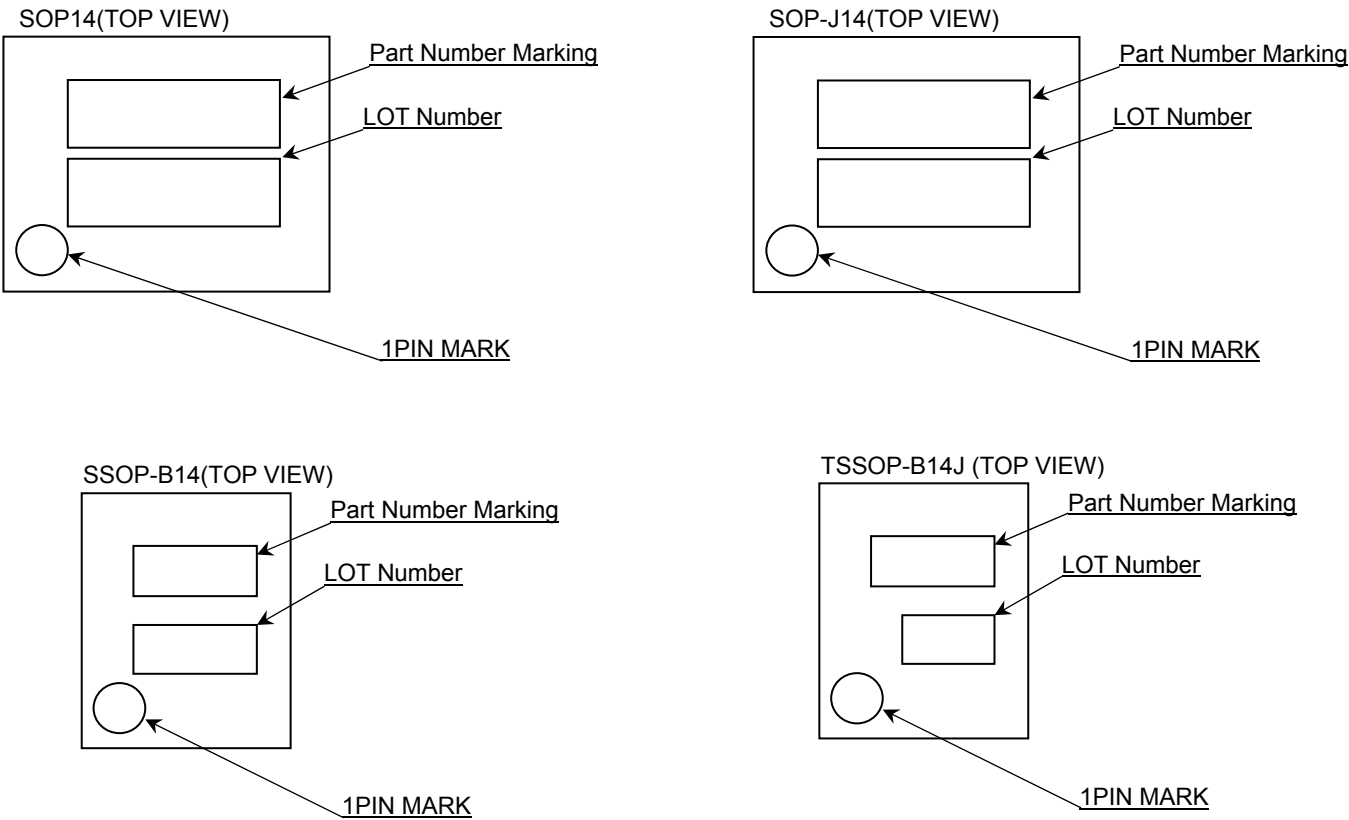
Physical Dimension, Tape and Reel Information - continued



Marking Diagram



Marking Diagram - continued



Product Name		Package Type	Marking
BD12730	G	SSOP5	K7
BD12732	F	SOP8	D2732
	FJ	SOP-J8	D2732
	FV	SSOP-B8	2732
	FVT	TSSOP-B8	D2732
	FVM	MSOP8	D2732
	FVJ	TSSOP-B8J	D2732
BD12734	F	SOP14	BD12734F
	FJ	SOP-J14	D2734
	FV	SSOP-B14	D2734
	FVM	TSSOP-B14J	D2734

Revision History

Date	Revision	Changes
30.Nov.2013	001	New Release
11.Feb.2013	002	Added BD12732F and BD12734F
1.Apr.2014	003	BD12732FJ/FV/FVT/FVM/FVJ and BD12734FJ/FV/FVJ package variation added
4.July.2016	004	Change Operating Voltage Range Before:1.8V to 5V After:1.8V to 5.5V, Correction of erroneous description(P.28)
14.July.2016	005	Key Specifications : Temperature Range → Operating Temperature Range(P.1) Line-up : T _{opr} → Operating Temperature(P.3) Delete Land Pattern Data(P.50) Correction of erroneous description (P.49 Diag-r-m → Diagram)

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
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 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
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- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
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- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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 - [d] the Products are exposed to high Electrostatic
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