18Mb SYNCBURST™ SRAM

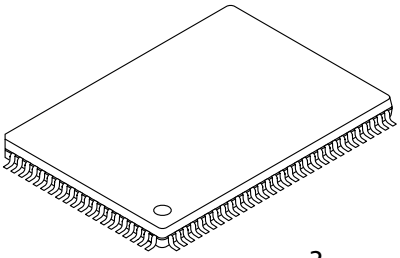
MT58L1MY18P, MT58V1MV18P,
MT58L512Y32P, MT58V512V32P,
MT58L512Y36P, MT58V512V36P

3.3V VDD, 3.3V or 2.5V I/O; 2.5V VDD, 2.5V I/O

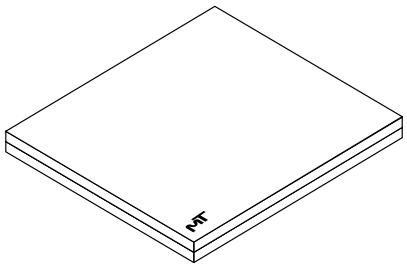
FEATURES

- Fast clock and OE# access times
- Single +3.3V ±0.165V or 2.5V =/-0.125V power supply (VDD)
- Separate +3.3V or +2.5V isolated output buffer
- Supply (VDDQ)
- SNOOZE MODE for reduced-power standby
- Single-cycle deselect (Pentium® BSRAM-compatible)
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- Low capacitive bus loading
- x18, x32, and x36 versions available

100-Pin TQFP[1]



165-Ball FBGA[2]



1. JEDEC-Standard MS-025 BHA (LQFP).
2. JEDEC Standard MS-216 (Var. CAB-1)

OPTIONS

OPTIONS	TQFP MARKING
• Timing (Access/Cycle/MHz)	
3.3V VDD, 3.3V or 2.5V I/O, and 2.5V VDD, 2.5V I/O	
3.1ns/5ns/200 MHz	-5
3.5ns/6ns/166 MHz	-6
4.2ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10
• Configurations	
3.3V VDD, 3.3V or 2.5V I/O	
1 Meg x 18	MT58L1MY18P
512K x 32	MT58L512Y32P
512K x 36	MT58L512Y36P
2.5V VDD, 2.5V I/O	
1 Meg x 18	MT58V1MV18P
512K x 32	MT58V512V32P
512K x 36	MT58V512V36P

OPTIONS

OPTIONS	TQFP MARKING
• Packages	
100-pin TQFP (3-chip enable)	T
165-ball FBGA	F*
• Operating Temperature Range	
Commercial (+10°C ≤ T_J ≤ 110°C)	None

*A Part Marking Guide for the FBGA devices can be found on Micron's Web site—http://www.micron.com/numberguide.

Part Number Example:

MT58L512Y36P-10

GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

Micron's 18Mb SyncBurst SRAMs integrate a 1 Meg x 18, 512K x 32, or 512K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#), and global write (GW#).

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa pins/balls and DQPa; BWb# controls DQb pins/balls and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa pins/balls and DQPa; BWb# controls DQb pins/balls and DQPb; BWc# controls DQc pins/balls and DQPc; BWd# controls DQd pins/balls and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

This device incorporates a single-cycle deselect feature during READ cycles. If the device is immediately deselected after a READ cycle, the output bus goes to a High-Z state ^{t}KQHZ nanoseconds after the rising edge of clock.

The device is ideally suited for Pentium and PowerPC pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64-, and 72-bit-wide applications.

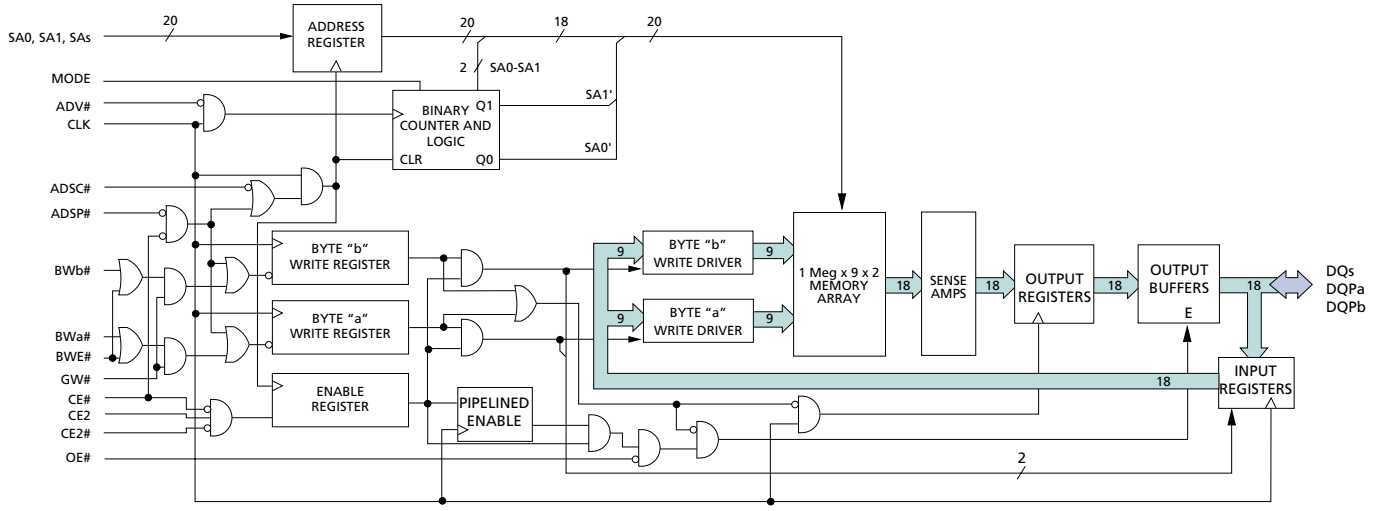
Please refer to Micron's Web site (www.micron.com/sramds) for the latest data sheet.

DUAL VOLTAGE I/O

The 3.3V V_{DD} device is tested for 3.3V and 2.5V I/O function. The 2.5V V_{DD} device is tested for only 2.5V I/O function.

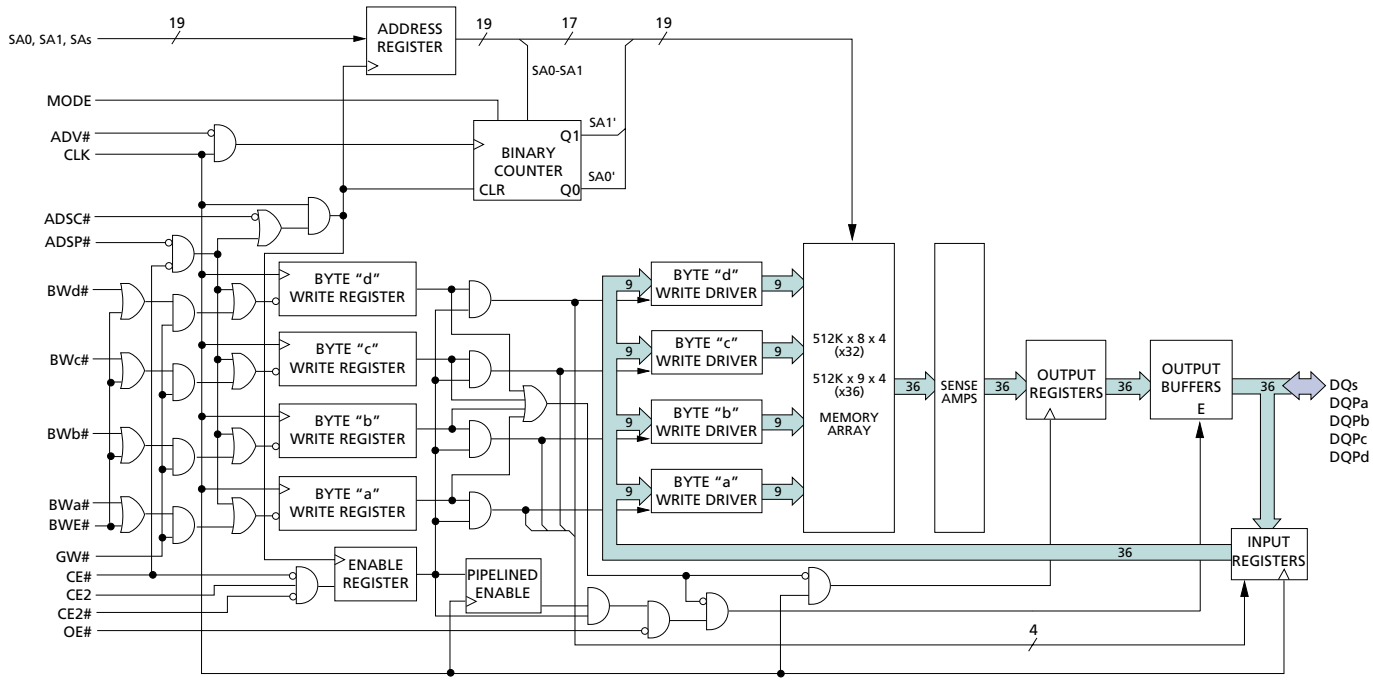
FUNCTIONAL BLOCK DIAGRAM

1 MEG x 18



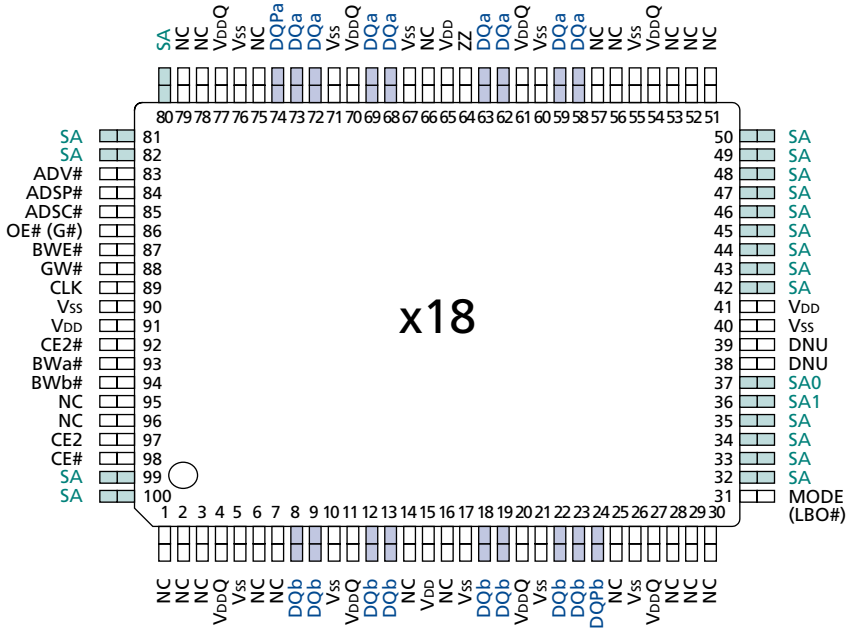
FUNCTIONAL BLOCK DIAGRAM

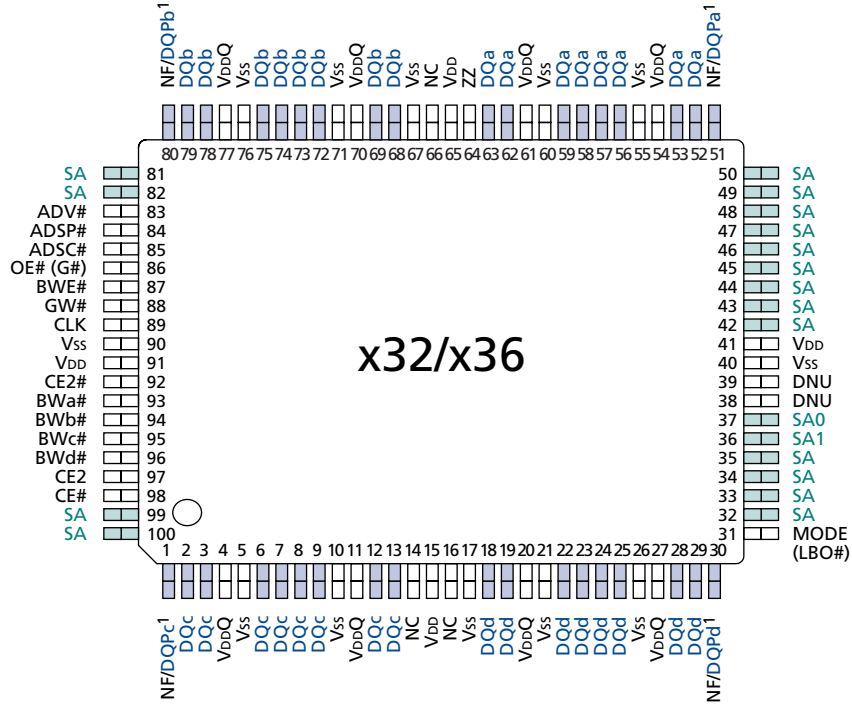
512K x 32/36



Note: Functional block diagrams illustrate simplified device operation. See truth tables, pin descriptions, and timing diagrams for detailed information.

PIN LAYOUT (TOP VIEW)
100-PIN TQFP (3-Chip Enable)





Notes: **1.** No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.
2. Pins 39 and 38 are reserved for address expansion; 36Mb and 72Mb, respectively.

TQFP PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. For the x32 and x36 versions, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. Parity is only available on the x18 and x36 versions.
BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
GW#	Input	Global Write: This active LOW input allows a full 18-, 32- or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.
ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2, and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. This pin has an internal pull-down and can be floating.
DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte "a" is DQa pins; Byte "b" is DQb pins. For the x32 and x36 versions, Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.

TQFP PIN DESCRIPTIONS (Continued)

SYMBOL	TYPE	DESCRIPTION
NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF/ I/O	No Function/Parity Data I/Os: On the x32 version, these pins are No Function (NF). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd. No Function pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals.
V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
V_{DDQ}	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
V_{SS}	Supply	Ground: GND.
DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.

BALL LAYOUT (TOP VIEW)
165-BALL FBGA

x18

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWb#	NC	CE2#	BWE#	ADSC#	ADV#	SA	SA
B	NC	SA	CE2	NC	BWa#	CLK	GW#	OE# (G#)	ADSP#	SA	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	VDD	VSS	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	VSS	NC	SA	VSS	VSS	VDDQ	NC	NC
P	NC	NC	SA	SA	TD1	SA1	TD0	SA	SA	SA	SA
R	MODE (LBO#)	NC	SA	SA	TMS	SA0	TCK	SA	SA	SA	SA

TOP VIEW

x32/x36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWc#	BWb#	CE2#	BWE#	ADSC#	ADV#	SA	NC
B	NC	SA	CE2	BWd#	BWa#	CLK	GW#	OE# (G#)	ADSP#	SA	NC
C	NF/DQPc[1]	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	NF/DQPb[1]
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	VDD	VSS	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
P	NF/DQPd[1]	NC	VDDQ	VSS	NC	SA	VSS	VSS	VDDQ	NC	NF/DQPa[1]
R	NC	NC	SA	SA	TD1	SA1	TD0	SA	SA	SA	SA
	MODE (LBO#)	NC	SA	SA	TMS	SA0	TCK	SA	SA	SA	SA

TOP VIEW

Notes: **1.** No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.
2. Pins 2R and 2P are reserved for address expansion; 36Mb and 72Mb, respectively.

FBGA BALL DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOWfor a WRITE cycle and HIGH for a READ cycle. For the x18 version,BWa# controls DQa and DQPa balls; BWb# controls DQb and DQPb balls. For the x32 and x36 versions, BWa# controls DQa and DQPa balls; BWb# controls DQb and DQPb balls; BWc# controls DQcs and DQPc balls; BWd# controls DQd and DQPd balls. Parity is only available on the x18 and x36 versions.
BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
GW#	Input	Global Write: This active LOW input allows a full 18-, 32-, or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
OE#(G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
ADV#	Input	Synchcronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling busrt access after the external address is loaded. A HIGH on ADV# effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is iniated.
ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2, and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new extrnal address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this ball selects "linear burst." NC or HIGH on this ball selects "interleaved burst." Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
TMS TDI TCK	Input	IEEE 1149.1 test inputs: JEDEC-standard 2.5V I/O levels. These balls may be left not connected if the JTAG function is not used in the circuit.
DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte "a" is DQa balls; Byte "b" is DQb balls. For the x32 and x36 versions, Byte "a" is DQa balls; Byte "b" is DQb balls; Byte "c" is DQc balls; Byte "d" is DQd balls. Input data must meet setup and hold times around the rising edge of CLK.

FBGA BALL DESCRIPTIONS (Continued)

SYMBOL	TYPE	DESCRIPTION
NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF/ I/O	No Function/Parity Data I/Os: On the x32 version, these pins are No Function (NF). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd.
V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
$V_{DD}Q$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
V_{SS}	Supply	Ground: GND.
TDO	Output	IEEE 1149.1 test outputs: JEDEC-standard 2.5V I/O level.
NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x18)

FUNCTION	GW#	BWE#	BWa#	BWb#
READ	H	H	X	X
READ	H	L	H	H
WRITE Byte “a”	H	L	L	H
WRITE Byte “b”	H	L	H	L
WRITE All Bytes	H	L	L	L
WRITE All Bytes	L	X	X	X

Note: Using BWE# and BWa# through BWd#, any one or more bytes may be written.

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x32/x36)

FUNCTION	GW#	BWE#	BWa#	BWb#	BWc#	BWd#
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte “a”	H	L	L	H	H	H
WRITE All Bytes	H	L	L	L	L	L
WRITE All Bytes	L	X	X	X	X	X

Note: Using BWE# and BWa# through BWd#, any one or more bytes may be written.

TRUTH TABLE

(Notes: 1-8)

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	DQ
DESELECT Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
DESELECT Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Notes:
1. X means "Don't Care." # means active LOW. H means logic HIGH. L means logic LOW.
2. For WRITE#, L means any one or more byte write enable signals (BWa#, BWb#, BWc# or BWd#) and BWE# are LOW or GW# is LOW. WRITE# = H for all BWx#, BWE#, GW# HIGH.
3. BWa# enables WRITEs to DQa's and DQPa. BWb# enables WRITEs to DQb's and DQPb. BWc# enables WRITEs to DQc's and DQPc. BWd# enables WRITEs to DQd's and DQPd. DQPa and DQPb are only available on the x18 and x36 versions. DQPc and DQPd are only available on the x36 version.
4. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, OE# must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP# LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE# LOW or GW# LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

3.3V VDD, ABSOLUTE MAXIMUM RATINGS*

Voltage on VDD Supply Relative to VSS..... -0.5V to +4.6V
Voltage on VDDQ Supply
Relative to VSS ..... -0.5V to +4.6V
VIN (DQx) ..... -0.5V to VDDQ + 0.5V
VIN (inputs) ..... -0.5V to VDD + 0.5V
Storage Temperature (TQFP).....-55ºC to +150ºC
Storage Temperature (FBGA).....-55ºC to +125ºC
Junction Temperature**..... +150ºC
Short Circuit Output Current 100mA

2.5V VDD, ABSOLUTE MAXIMUM RATINGS*

Voltage on VDD Supply Relative to VSS..... -0.3V to +3.6V
Voltage on VDDQ Supply
Relative to VSS..... -0.3V to +3.6V
VIN (DQx) ..... -0.3V to VDDQ + 0.3V
VIN (inputs) ..... -0.3V to VDD + 0.3V
Storage Temperature (TQFP)..... -55ºC to +150ºC
Storage Temperature (FBGA)..... -55ºC to +125ºC
Junction Temperature**..... +150ºC
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

3.3V VDD, 3.3V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+10°C ≤ T_J ≤ 110°C; VDD = + 3.3V ±0.165V; VDDQ = + 3.3V ±0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.0	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDD	ILO	-1.0	1.0	µA	
Output High Voltage	IOH = -4.0mA	VOH	2.4	–	V	1, 4
Output Low Voltage	IOL = 8.0mA	VOL	–	0.4	V	1, 4
Supply Voltage		VDD	3.135	3.465	V	1
Isolated Output Buffer Supply		VDDQ	3.135	3.465	V	1, 5

Notes:
1. All voltages referenced to VSS (GND).
2. For 3.3V VDD:
   Overshoot: VIH ≤ +4.6V for t ≤ ^{t}KC/2 for I ≤ 20mA
   Undershoot: VIL ≥ -0.7V for t ≤ ^{t}KC/2 for I ≤ 20mA
   Power-up: VIH ≤ +3.6V and VDD ≤ 3.135V for t ≤ 200ms
   For 2.5V VDD:
   Overshoot: VIH ≤ +3.6V for t ≤ ^{t}KC/2 for I ≤ 20mA
   Undershoot: VIL ≥ -0.7V for t ≤ ^{t}KC/2 for I ≤ 20mA
   Power-up: VIH ≤ +2.65V and VDD ≤ 2.375V for t ≤ 200ms
3. MODE pin has an internal pull-up, and input leakage = ±10µA.
4. The load used for VOH, VOL testing is shown in Figure 2 for 3.3V I/O. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
5. VDDQ should never exceed VDD. VDD and VDDQ can be connected together.

3.3V VDD, 2.5V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+10°C ≤ T_J ≤110°C; VDD = + 3.3V ±0.165V; VDDQ = +2.5V ±0.125V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	VIHQ	1.7	VDDQ + 0.3	V	1, 2
	Inputs	VIH	1.7	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (DQx)	ILO	-1.0	1.0	µA	
Output High Voltage	IOH = -2.0mA	VOH	1.7	–	V	1, 4
	IOH = -1.0mA	VOH	2.0	–	V	1, 4
Output Low Voltage	IOL = 2.0mA	VOL	–	0.7	V	1, 4
Supply Voltage		VDD	3.135	3.465	V	1
Isolated Output Buffer Supply		VDDQ	2.375	2.625	V	1

2.5V VDD, 2.5V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+10°C ≤ T_J ≤110°C; VDD = + 2.5V ±0.125V; VDDQ = + 2.5V ±0.125V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	VIHQ	1.7	VDDQ + 0.3	V	1, 2
	Inputs	VIH	1.7	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (DQx)	ILO	-1.0	1.0	µA	
	IOH = -1.0mA	VOH	2.0	–	V	1, 4
Output Low Voltage	IOL = 2.0mA	VOL	–	0.7	V	1, 4
	IOL = 1.0mA	VOL	–	0.4	V	1, 4
Supply Voltage		VDD	2.375	2.625	V	1
Isolated Output Buffer Supply		VDDQ	2.375	2.625	V	1

Notes:
1. All voltages referenced to VSS (GND).
2. For 3.3V VDD:
   Overshoot: VIH ≤ +4.6V for t ≤ $^tKC/2$ for I ≤ 20mA
   Undershoot: VIL ≥ -0.7V for t ≤ $^tKC/2$ for I ≤ 20mA
   Power-up: VIH ≤ +3.6V and VDD ≤ 3.135V for t ≤ 200ms
   For 2.5V VDD:
   Overshoot: VIH ≤ +3.6V for t ≤ $^tKC/2$ for I ≤ 20mA
   Undershoot: VIL ≥ -0.7V for t ≤ $^tKC/2$ for I ≤ 20mA
   Power-up: VIH ≤ +2.65V and VDD ≤ 2.375V for t ≤ 200ms
3. MODE pin has an internal pull-up, and input leakage = ±10µA.
4. The load used for VOH, VOL testing is shown in Figure 2 for 3.3V I/O. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
5. VDDQ should never exceed VDD. VDD and VDDQ can be connected together.

TQFP CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	TA = 25°C; f = 1 MHz; V_{DD} = 3.3V	Ci	4.2	5	pF	1
Input/Output Capacitance (DQ)		Co	3.5	4	pF	1
Address Capacitance		Ca	4	5	pF	1
Clock Capacitance		CCK	4.2	5	pF	1

FBGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A= 25°C; f = 1 MHz	C_I	4	5	pF	1
Output Capacitance (Q)		C_O	4	4.5	pF	1
Clock Capacitance		C_{CK}	5	5.5	pF	1

TQFP THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	46	°C/W	1
Thermal Resistance (Junction to Top of Case)		θ_{JC}	2.8	°C/W	1

FBGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	40	°C/W	1
Junction to Case (Top)		θ_{JC}	9	°C/W	1
Junction to Balls		θ_{JB}	17	°C/W	1

Notes: **1.** This parameter is sampled.

3.3V VDD IDD OPERATINGCONDITIONS AND MAXIMUM LIMITS (1 MEG x 18)

(Note 1, unless otherwise noted) (+10°C ≤ T_J ≤110°C)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYM**	**TYP**	**-5**	**-6**	**-7.5**	**-10**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; All inputs ≥ VIL or ≤ VIH; Cycle time ≤ tKC (MIN); VDD = MAX; Outputs open	IDD	TBD	300	275	225	200	mA	1, 2, 3
Power Supply Current: Idle	Device selected; VDD = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≤ VIH; All inputs ≥ VSS + 0.2 or ≤ VDDQ - 0.2; Cycle time ≥ tKC (MIN)	IDD1	TBD	210	190	170	145	mA	2, 3, 4
CMOS Standby	Device deselected; VDD = MAX; All inputs ≥ VSS + 0.2 or ≤ VDDQ - 0.2; All inputs static; CLK frequency = 0	ISB2	TBD	30	30	30	30	mA	3, 4
Clock Running	Device deselected; VDD = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≤ VIH; All inputs ≥ VSS + 0.2 or ≤ VDDQ - 0.2; Cycle time ≤ tKC (MIN)	ISB4	TBD	210	190	170	145	mA	3, 4
Snooze Mode	ZZ ≥ VIH	ISB2Z	TBD	30	30	30	30	mA	4

2.5V VDD, IDD OPERATING CONDITIONS AND MAXIMUM LIMITS (1 MEG x 18)

(Note 1, unless otherwise noted) (+10°C ≤ T_J ≤110°C)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYM**	**TYP**	**-5**	**-6**	**-7.5**	**-10**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKC (MIN); VDD = MAX; Outputs open	IDD	TBD	290	250	210	180	mA	1, 2, 3
Power Supply Current: Idle	Device selected; VDD = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDDQ - 0.2; Cycle time ≥ tKC (MIN)	IDD1	TBD	195	170	150	130	mA	2, 3, 5
CMOS Standby	Device deselected; VDD = MAX; All inputs ≤ VSS + 0.2 or ≥ VDDQ - 0.2; All inputs static; CLK frequency = 0	ISB2	TBD	30	30	30	30	mA	3, 5
Clock Running	Device deselected; VDD = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDDQ - 0.2; Cycle time ≥ tKC (MIN)	ISB4	TBD	195	170	150	130	mA	3, 5
Snooze Mode	ZZ ≥ VIH	ISB2Z	TBD	30	30	30	30	mA	5

Notes:
1. VDDQ = +2.5V. Voltage tolerances: +3.3V ±0.165 or +2.5V ±0.125V for all values of VDD and VDDQ.
2. IDD is specified with no output current and increases with faster cycle times. IDDQ increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
4. Typical values are measured at 3.3V, 25°C, and 10ns cycle time.
5. Typical values are measured at 2.5V, 25°C, and 10ns cycle time.

3.3V VDD, IDD OPERATING CONDITIONS AND MAXIMUM LIMITS (512K x 32/36)

(Note 1, unless otherwise noted) (+10°C ≤ T_J ≤110°C)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYM**	**TYP**	**-5**	**-6**	**-7.5**	**-10**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKC (MIN); VDD = MAX; Outputs open	IDD	TBD	380	340	280	230	mA	1,2,3
Power Supply Current: Idle	Device selected; VDD = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDDQ - 0.2; Cycle time ≥ tKC (MIN)	IDD1	TBD	210	180	160	145	mA	2, 3, 4
CMOS Standby	Device deselected; VDD = MAX; All inputs ≤ VSS + 0.2 or ≥ VDDQ - 0.2; All inputs static; CLK frequency = 0	ISB2	TBD	30	30	30	30	mA	3, 4
Clock Running	Device deselected; VDD = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDDQ - 0.2; Cycle time ≥ tKC (MIN)	ISB4	TBD	210	180	160	145	mA	3, 4
Snooze Mode	ZZ ≥ VIH	ISB2Z	TBD	30	30	30	30	mA	4

2.5 VDD IDD OPERATINGCONDITIONS AND MAXIMUM LIMITS (512K x 32/36)

(Note 1, unless otherwise noted) (+10°C ≤ T_J ≤110°C)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYM**	**TYP**	**-5**	**-6**	**-7.5**	**-10**	**UNITS**	**NOTES**
Power Supply Current: Operating	Device selected; All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKC (MIN); VDD = MAX; Outputs open	IDD	TBD	360	310	260	210	mA	1,2,3
Power Supply Current: Idle	Device selected; VDD = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDDQ - 0.2; Cycle time ≥ tKC (MIN)	IDD1	TBD	190	165	140	120	mA	2, 3, 5
CMOS Standby	Device deselected; VDD = MAX; All inputs ≤ VSS + 0.2 or ≥ VDDQ - 0.2; All inputs static; CLK frequency = 0	ISB2	TBD	30	30	30	30	mA	3, 5
Clock Running	Device deselected; VDD = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ VIH; All inputs ≤ VSS + 0.2 or ≥ VDDQ - 0.2; Cycle time ≥ tKC (MIN)	ISB4	TBD	190	165	140	120	mA	3, 5
Snooze Mode	ZZ ≥ VIH	ISB2Z	TBD	30	30	30	30	mA	5

Notes:
1. VDDQ = +2.5V. Voltage tolerances: +3.3V ±0.165 or +2.5V ±0.125V for all values of VDD and VDDQ.
2. IDD is specified with no output current and increases with faster cycle times. IDDQ increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
4. Typical values are measured at 3.3V, 25°C, and 10ns cycle time.
5. Typical values are measured at 2.5V, 25°C, and 10ns cycle time.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

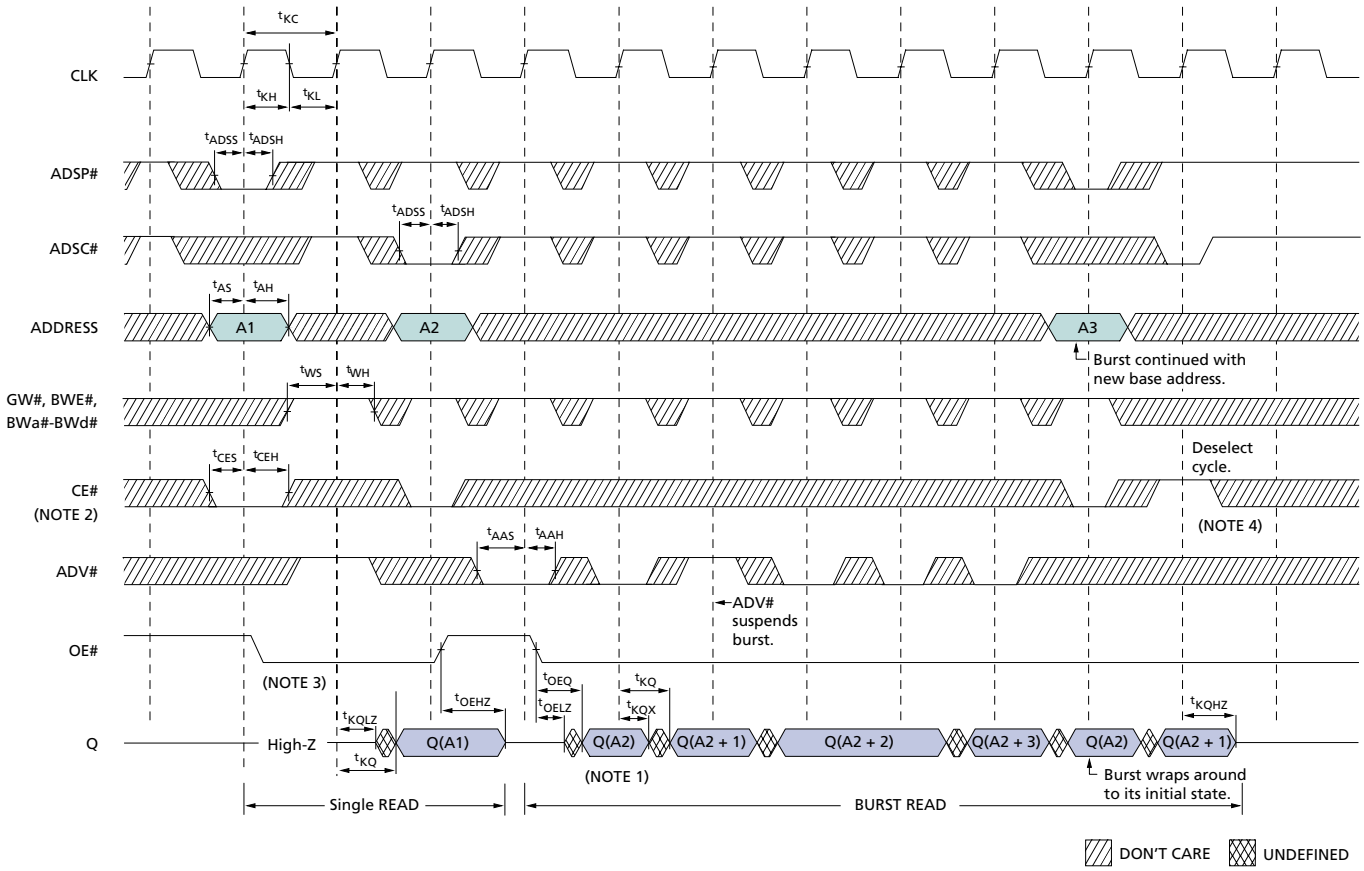
(Note 1) (+10°C ≤ T_J ≤110°C; V_{DD} = +3.3V +0.3V/-0.165V unless otherwise noted)

		-5		-6		-7.5		-10			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	^tKC	5.0		6.0		7.5		10.0		ns	
Clock frequency	^tKF		200		166		133		100	MHz	
Clock HIGH time	^tKH	2.0		2.3		2.5		3.0		ns	2
Clock LOW time	^tKL	2.0		2.3		2.5		3.0		ns	2
Output Times											
Clock to output valid	^tKQ		3.1		3.5		4.0		5.0	ns	
Clock to output invalid	^tKQX	1.0		1.5		1.5		1.5		ns	2
Clock to output in Low-Z	^tKQLZ	0		0		0		0		ns	3, 4, 5, 6
Clock to output in High-Z	^tKQHZ		3.1		3.5		4.2		5.0	ns	3, 4, 5, 6
OE# to output valid	^tOEQ		3.1		3.5		4.0		5.0	ns	7
OE# to output in Low-Z	^tOELZ	0		0		0		0		ns	3, 4, 5, 6
OE# to output in High-Z	^tOEHZ		3.0		3.0		3.5		4.5	ns	3, 4, 5, 6
Setup Times											
Address	^tAS	1.4		1.5		1.5		2.0		ns	8, 9
Address status (ADSC#, ADSP#)	^tADSS	1.4		1.5		1.5		2.0		ns	8, 9
Address advance (ADV#)	^tAAS	1.4		1.5		1.5		2.0		ns	8, 9
Write signals (BWa#-BWd#, BWE#, GW#)	^tWS	1.4		1.5		1.5		2.0		ns	8, 9
Data-in	^tDS	1.4		1.5		1.5		2.0		ns	8, 9
Chip enables (CE#, CE2#, CE2)	^tCES	1.4		1.5		1.5		2.0		ns	8, 9
Hold Times											
Address	^tAH	0.4		0.5		0.5		0.5		ns	8, 9
Address status (ADSC#, ADSP#)	^tADSH	0.4		0.5		0.5		0.5		ns	8, 9
Address advance (ADV#)	^tAAH	0.4		0.5		0.5		0.5		ns	8, 9
Write signals (BWa#-BWd#, BWE#, GW#)	^tWH	0.4		0.5		0.5		0.5		ns	8, 9
Data-in	^tDH	0.4		0.5		0.5		0.5		ns	8, 9
Chip enables (CE#, CE2#, CE2)	^tCEH	0.4		0.5		0.5		0.5		ns	8, 9

Notes:
1. Test conditions as specified with the output loading shown in Figure 1 for +3.3V I/O (V_{DDQ} = +3.3V ±0.165V) and Figure 3 for 2.5V I/O (V_{DDQ} = +2.5V ±0.125V) unless otherwise noted. (All Figures shown following timing diagrams.)
2. If V_{DD} = +3.3V, then V_{DDQ} = +3.3V or +2.5V. If V_{DD} = +2.5V, then V_{DDQ} = +2.5V. Voltage tolerances: +3.3V ±0.165 or +2.5V ±0.125V for all values of V_{DD} and V_{DDQ}.
3. Measured as HIGH above V_{IH} and LOW below V_{IL}.
4. This parameter is measured with the output loading shown in Figure 2. (All Figures shown following timing diagrams.)
5. This parameter is sampled.
6. Transition is measured ±500mV from steady state voltage.
7. Refer to Technical Note TN-58-09, "Synchronous SRAM Bus Contention Design Considerations," for a more thorough discussion on these parameters.
8. OE# is a "Don't Care" when a byte write enable is sampled LOW.

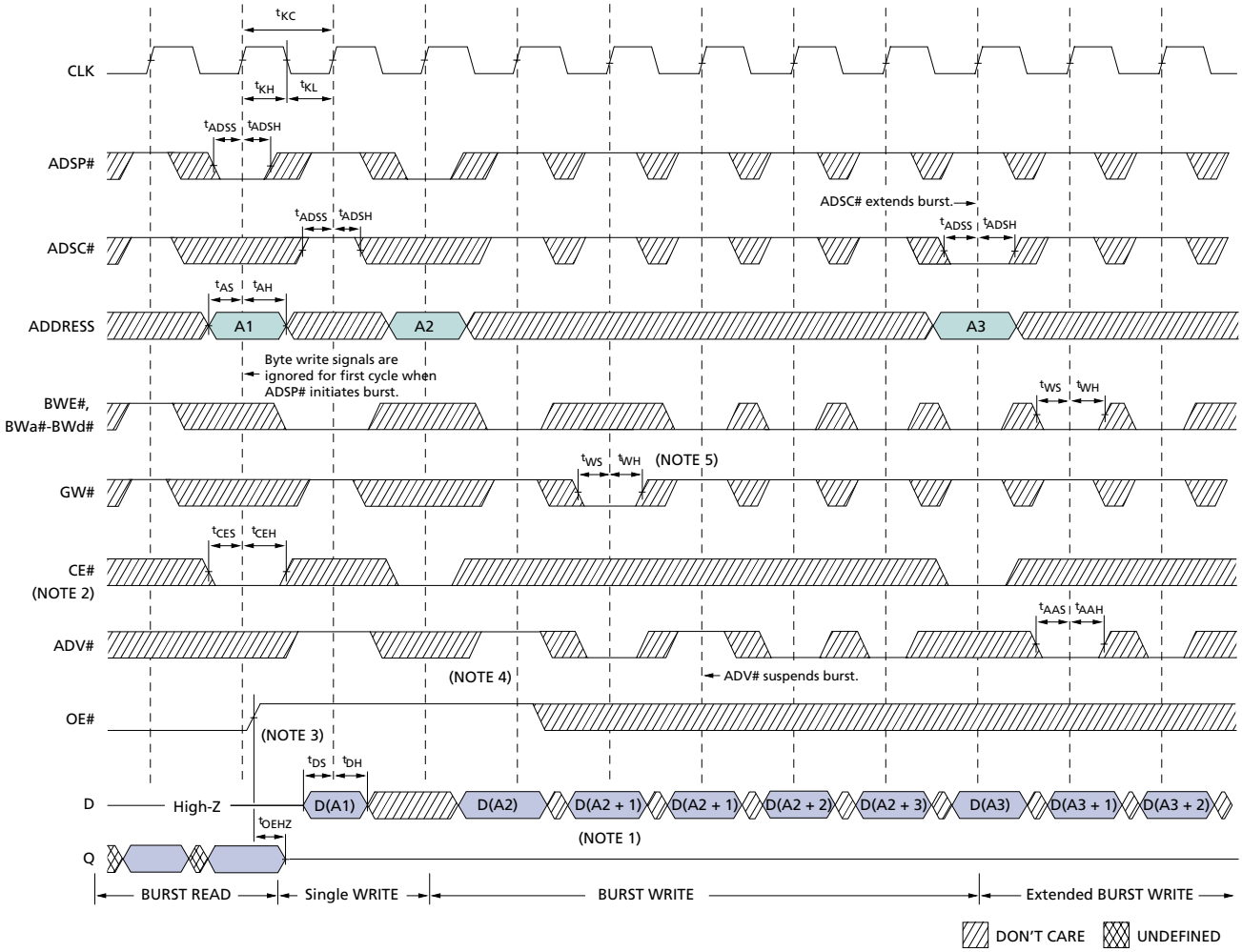
9. A write cycle is defined by at least one byte write enable LOW and ADSP# HIGH for the required setup and hold times. A read cycle is defined by all byte write enables HIGH and ADSC# or ADV# LOW or ADSP# LOW for the required setup and hold times.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP# or ADSC# is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times withstable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP# or ADSC# is LOW to remain enabled.

READ TIMING[3]



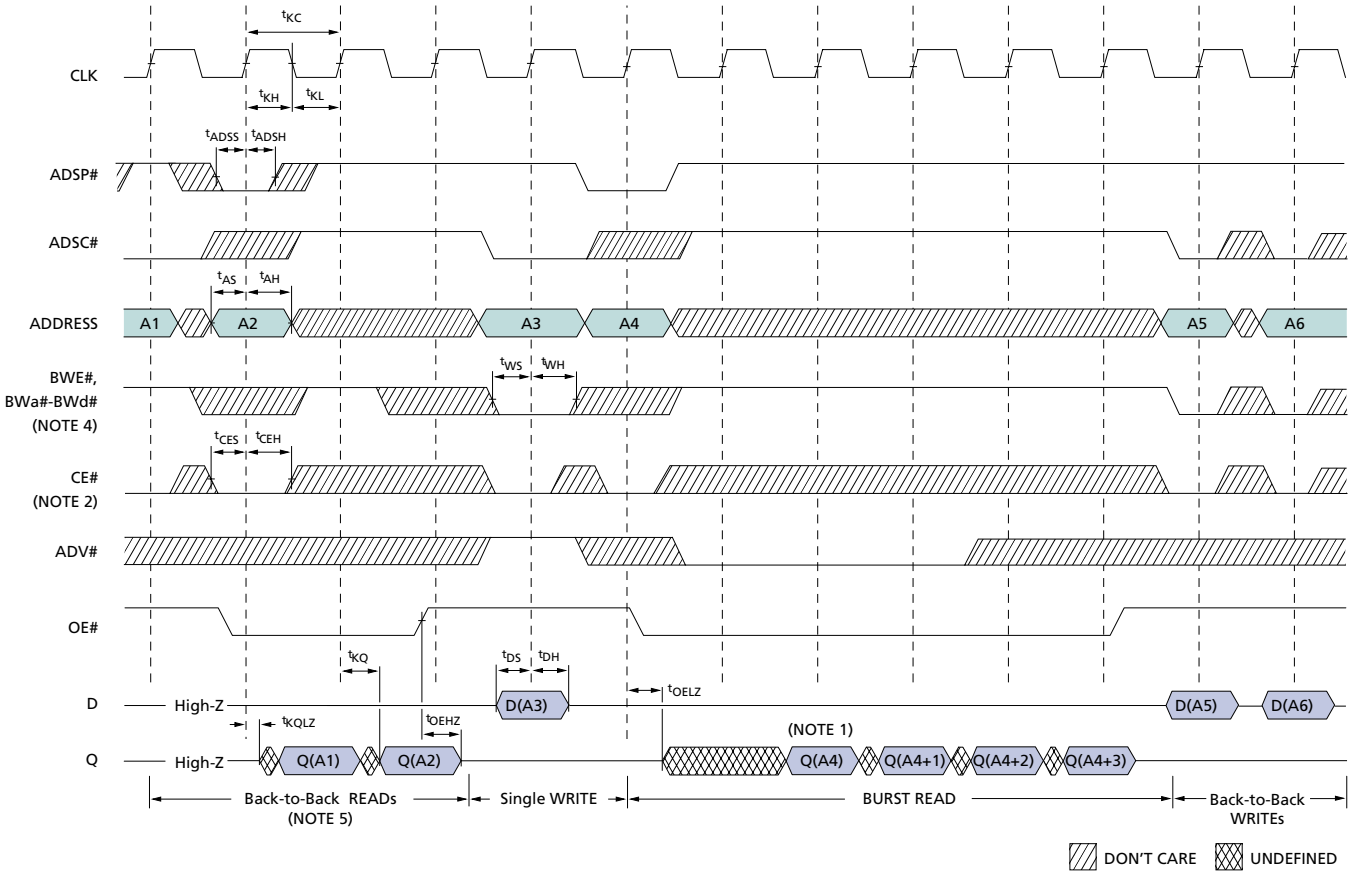
Notes:
1. Q(A2) refers to output from address A2. Q(A2 + 1) refers to output from the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. OE# does not cause Q to be driven until after the following clock rising edge.
4. Outputs are disabled within one clock cycle after deselect.

WRITE TIMING



Notes:
1. D(A2) refers to input for address A2. D(A2 + 1) refers to input for the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. OE# must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. ADV# must be HIGH to permit a WRITE to the loaded address.
5. Full-width WRITE can be initiated by GW# LOW; or GW# HIGH and BWE#, BWa# and BWb# LOW for x18 device; or GW# HIGH and BWE#, BWa#-BWd# LOW for x32 and x36 devices.

READ/WRITE TIMING[3]



Notes:
1. Q(A4) refers to output from address A4. Q(A4 + 1) refers to output from the next internal burst address following A4.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP#, ADSC# or ADV# cycle is performed.
4. GW# is HIGH.
5. Back-to-back READs may be controlled by either ADSP# or ADSC#.

3.3V VDD, 3.3V I/O AC TEST CONDITIONS

Input pulse levels	VIH = (VDD/2.2) + 1.5V
	VIL = (VDD/2.2) - 1.5V
Input rise and fall times	1ns
Input timing reference levels	VDD/2.2
Output reference levels	VDDQ/2.2
Output load	See Figures 1 and 2

3.3V VDD, 2.5V I/O AC TEST CONDITIONS

Input pulse levels	VIH = (VDD/2.64) + 1.25V
	VIL = (VDD/2.64) - 1.25V
Input rise and fall times	1ns
Input timing reference levels	VDD/2.64
Output reference levels	VDDQ/2
Output load	See Figures 3 and 4

2.5V VDD, 2.5V I/O AC TEST CONDITIONS

Input pulse levels	VIH = (VDD/2) + 1.25V
	VIL = (VDD/2) - 1.25V
Input rise and fall times	1ns
Input timing reference levels	VDD/2
Output reference levels	VDD/2
Output load	See Figures 3 and 4

LOAD DERATING CURVES

Micron 1 Meg x 18, 512K x 32, and 512K x 36 SyncBurst SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.

3.3V I/O Output Load Equivalents

Figure 1

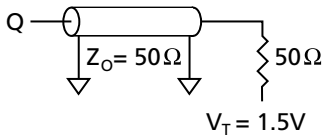
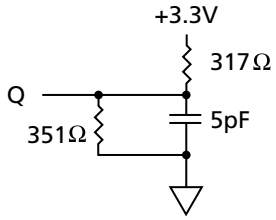


Figure 2



2.5V I/O Output Load Equivalents

Figure 3

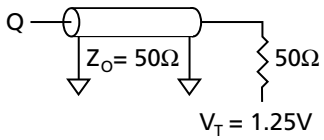
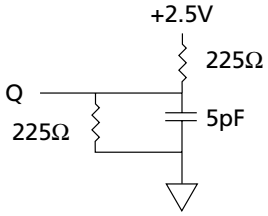


Figure 4



SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to ISB2Z. The duration of SNOOZE MODE is dictated by the length of time ZZ is in a HIGH state.

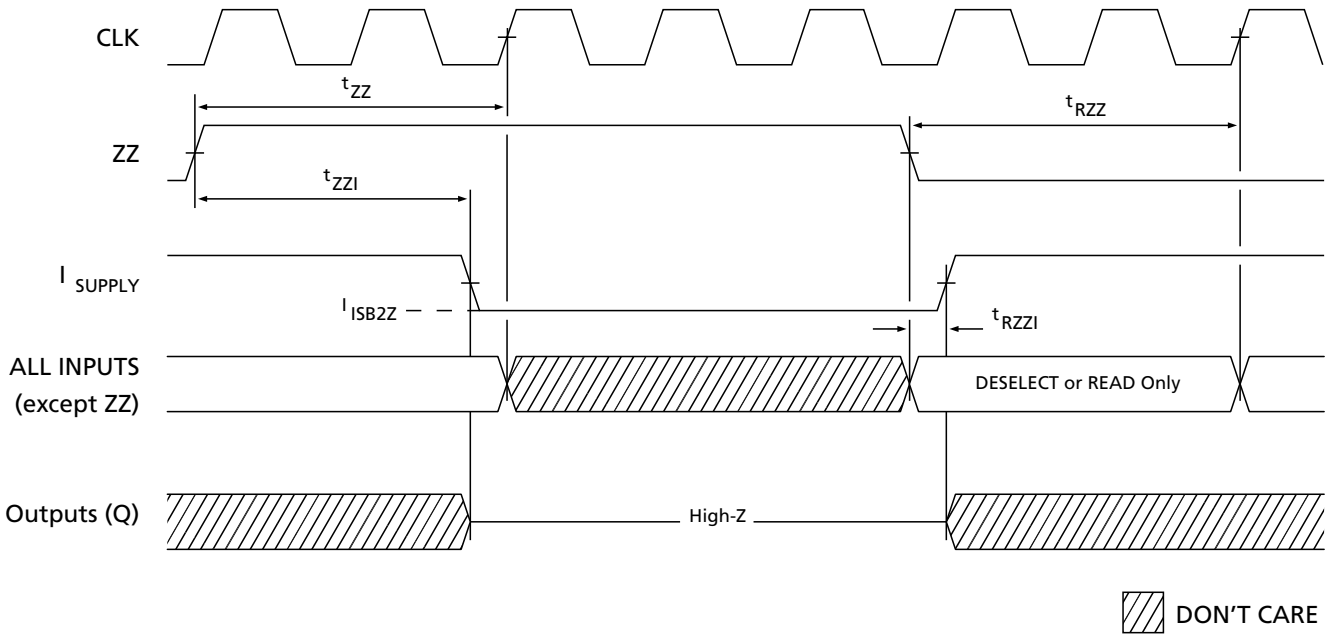
After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When ZZ becomes a logic HIGH, ISB2Z is guaranteed after the setup time ^{t}ZZ is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	ZZ ≥ VIH	I_{SB2Z}		30	mA	
ZZ active to input ignored		^{t}ZZ		2(^{t}KC)	ns	1
ZZ inactive to input sampled		^{t}RZZ	2(^{t}KC)		ns	1
ZZ active to snooze current		^{t}ZZI		2(^{t}KC)	ns	1
ZZ inactive to exit snooze current		^{t}RZZI	0		ns	1

Notes: **1.** This parameter is sampled.

Figure 5
SNOOZE MODE WAVEFORM



IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

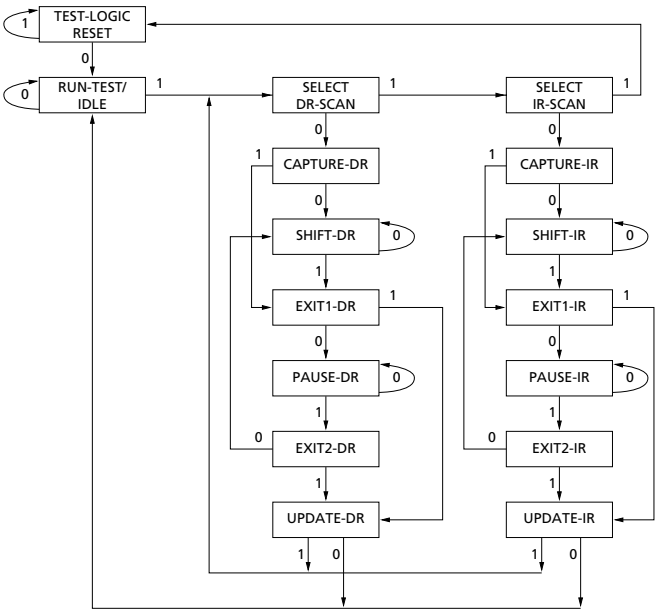
The SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

These pins/balls can be left floating (unconnected), if the JTAG function is not to be implemented. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Figure 6
TAP Controller State Diagram



Note: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TEST ACCESS PORT (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

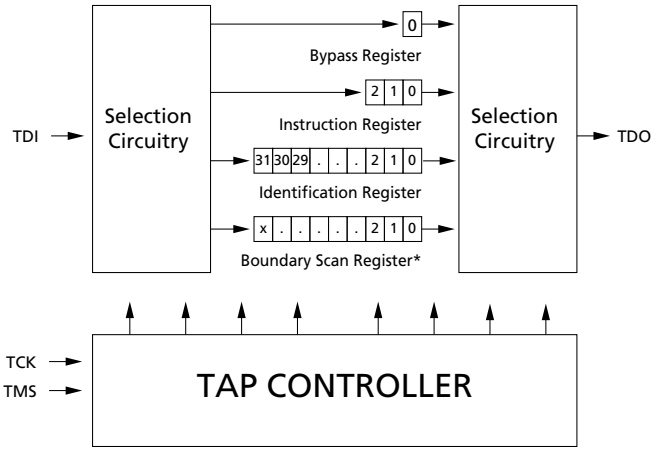
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 6. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 7.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. (See Figure 5.) The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Figure 7.)

Figure 7
TAP Controller Block Diagram



x = 75 for the x18 configuration, x = 75 for the x32 configuration, x = 75 for the x36 configuration.

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin/ball on the rising edge of TCK. Data is output on the TDO pin/ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins/balls as shown in Figure 5. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins/balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (VSS) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional pins/balls on the SRAM. The x36 configuration has a 75-bit-long register, the x32 configuration has a 75-bit-long register, and the x18 configuration has a 75-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins/balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODEcommand is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP INSTRUCTION SET

Overview

Eight different instructions are possible with the threebit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address, data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins/balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is tobe executed whenever the instruction register is loadedwith all 0s. EXTEST is not implemented in this

SRAM TAP controller, and therefore this device is not compliant to1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins/balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins/balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional pins/balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

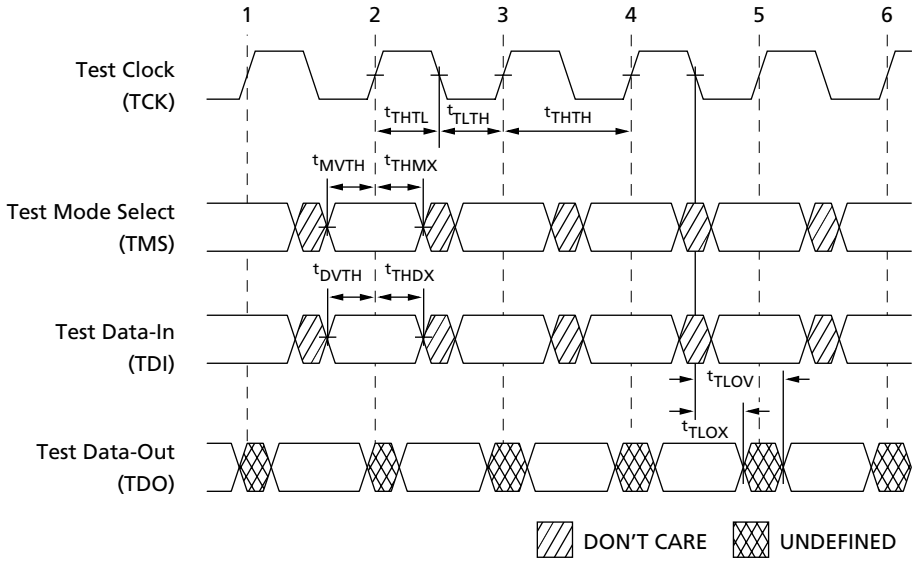
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instruction are not implemented but are reserved for future use. Do not use these instructions.

TAP TIMING



TAP AC ELECTRICAL CHARACTERISTICS

(Notes 1,2) (+10°C ≤ T_J ≤ +110°C; + 2.4V ≤ V_{DD} ≤ + 2.6V)

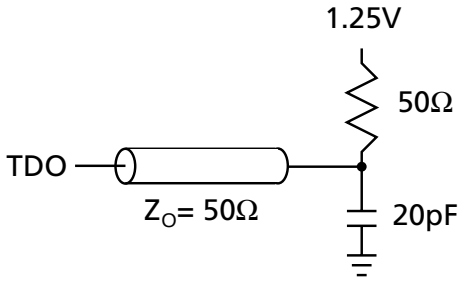
DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	100		ns
Clock frequency	^fTF		10	MHz
Clock HIGH time	^tTHTL	40		ns
Clock LOW time	^tTLTH	40		ns
Output Times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		20	ns
TDI valid to TCK HIGH	^tDVTH	10		ns
TCK HIGH to TDI invalid	^tTHDX	10		ns
Setup Times				
TMS setup	^tMVTH	10		ns
Capture setup	^tCS	10		ns
Hold Times				
TMS hold	^tTHMX	10		ns
Capture hold	^tCH	10		ns

Notes: 1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditons are specified using the load in Figure 7.

TAP AC TEST CONDITIONS

Input pulse levels ..... VSS to 2.5V
Input rise and fall times 1ns
Input timing reference levels..... 1.25V
Output reference levels..... 1.25V
Test load termination supply voltage 1.25V

Figure 7
TAP AC Output Load Equivalent



3.3V VDD, TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+10°C ≤ T_J ≤ +110°C; +3.135V ≤ VDD ≤ +3.465V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.0	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (DQx)	ILO	-5.0	5.0	µA	
Output Low Voltage	IOLC = 100µA	VOL1		0.7	V	1
Output Low Voltage	IOLT = 2mA	VOL2		0.8	V	1
Output High Voltage	IOHC = -100µA	VOH1	2.9		V	1
Output High Voltage	IOHT = -2mA	VOH2	2.0		V	1

2.5V VDD, TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(+10°C ≤ T_J ≤ +110°C; +3.135V ≤ VDD ≤ +3.465V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	1.7	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (DQx)	ILO	-5.0	5.0	µA	
Output Low Voltage	IOLC = 100µA	VOL1		0.2	V	1
Output Low Voltage	IOLT = 2mA	VOL2		0.7	V	1
Output High Voltage	IOHC = -100µA	VOH1	2.1		V	1
Output High Voltage	IOHT = -2mA	VOH2	1.7		V	1

Notes: **1.** All voltages referenced to VSS (GND).
2. Overshoot: VIH (AC) ≤ VDD + 1.5V for t ≤ ^{t}KHKH/2
Undershoot:VIL (AC) ≥ -0.5V for t ≤ ^{t}KHKH/2
Power-up:VIH ≤ +2.6V and VDD ≤ 2.4V and VDDQ ≤ 1.4V for t ≤ 200ms
During normal operation, VDDQ must not exceed VDD. Control input signals (such as LD#, R/W#, etc.) may not have pulse widths less than ^{t}KHKL (MIN) or operate at frequencies exceeding ^{f}KF (MAX).

IDENTIFICATION REGISTER DEFINITIONS

INSTRUCTION FIELD	512K X 18	DESCRIPTION
REVISION NUMBER (31:28)	xxxx	Reserved for version number.
DEVICE DEPTH (27:23)	00111	Defines depth of 512K or 1Mb words.
DEVICE WIDTH (22:18)	00011	Defines width of x18, x32, or x36 bits.
MICRON DEVICE ID (17:12)	xxxxxx	Reserved for future use.
MICRON JEDEC ID CODE (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

SCAN REGISTER SIZES

REGISTER NAME	BIT SIZE		
Instruction	3		
Bypass	1		
ID	32		
Boundary Scan	x18: 75	x32: 75	x36: 75

INSTRUCTION CODES

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

165-Ball FBGA Boundary Scan Order (x18)

FBGA BIT#	SIGNAL NAME	BALL ID
1	MODE (LB0#)	1R
2	SA	6N
3	SA	11P
4	SA	8P
5	SA	8R
6	SA	9R
7	SA	9P
8	SA	10P
9	SA	10R
10	SA	11R
11	ZZ	11H
12	NC	11N
13	NC	11M
14	NC	11L
15	NC	11K
16	NC	11J
17	DQa	10M
18	DQa	10L
19	DQa	10K
20	DQa	10J
21	DQa	11G
22	DQa	11F
23	DQa	11E
24	DQa	11D
25	DQa	11C
26	NC	10F
27	NC	10E
28	NC	10D
29	NC	10G
30	SA	11A
31	SA	10A
32	SA	10B
33	ADV#	9A
34	ADSP#	9B
35	ADSC#	8A
36	OE# (G#)	8B
37	BWE#	7A
38	GW#	7B
39	CLK	6B
40	NC	11B
41	NC	1A
42	CE2#	6A

165-Ball FBGA Boundary Scan Order (x18)

FBGA BIT#	SIGNAL NAME	BALL ID
43	BWa#	5B
44	NC	5A
45	BWb#	4B
46	NC	4B
47	CE2	3B
48	CE#	3A
49	SA	2A
50	SA	2B
51	NC	1B
52	NC	1C
53	NC	1D
54	NC	1E
55	NC	1F
56	NC	1G
57	DQb	2D
58	DQb	2E
59	DQb	2F
60	DQb	2G
61	DQb	1J
62	DQb	1K
63	DQb	1L
64	DQb	1M
65	DQb	1N
66	NC	2K
67	NC	2L
68	NC	2M
69	NC	2J
70	SA	3P
71	SA	3R
72	SA	4R
73	SA	4P
74	SA1	6P
75	SA0	6R

165-Ball FBGA Boundary Scan Order (x32)

FBGA BIT#	SIGNAL NAME	BALL ID
1	MODE (LB0#)	1R
2	SA	6N
3	SA	11P
4	SA	8P
5	SA	8R
6	SA	9R
7	SA	9P
8	SA	10P
9	SA	10R
10	SA	11R
11	ZZ	11H
12	NF	11N
13	DQa	11M
14	DQa	11L
15	DQa	11K
16	DQa	11J
17	DQa	10M
18	DQa	10L
19	DQa	10K
20	DQa	10J
21	DQb	11G
22	DQb	11F
23	DQb	11E
24	DQb	11D
25	DQb	10G
26	DQb	10F
27	DQb	10E
28	DQb	10D
29	NF	11C
30	NF	11A
31	SA	10A
32	SA	10B
33	ADV#	9A
34	ADSP#	9B
35	ADSC#	8A
36	OE# (G#)	8B
37	BWE#	7A
38	GW#	7B
39	CLK	6B
40	NC	11B
41	NC	1A

165-Ball FBGA Boundary Scan Order (x32)

FBGA BIT#	SIGNAL NAME	BALL ID
42	CE2#	6A
43	BWa#	5B
44	BWb#	5A
45	BWC#	4A
46	BWD#	4B
47	CE2	3B
48	CE#	3A
49	SA	2A
50	SA	2B
51	NC	1B
52	NF	1C
53	DQc	1D
54	DQc	1E
55	DQc	1F
56	DQc	1G
57	DQc	2D
58	DQc	2E
59	DQc	2F
60	DQc	2G
61	DQd	1J
62	DQd	1K
63	DQd	1L
64	DQd	1M
65	DQd	2J
66	DQd	2K
67	DQd	2L
68	DQd	2M
69	NF	1N
70	SA	3P
71	SA	3R
72	SA	4R
73	SA	4P
74	SA1	6P
75	SA0	6R

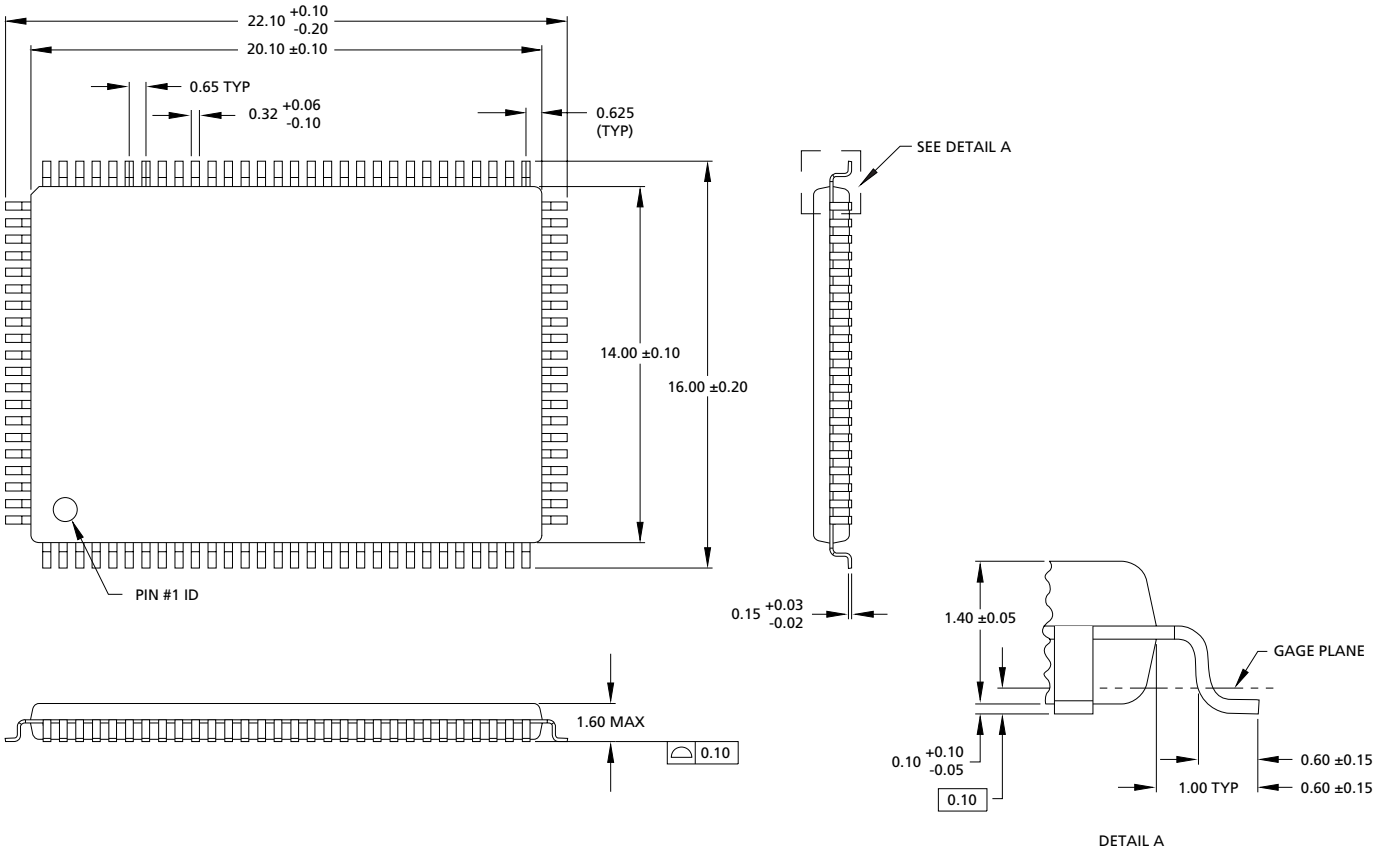
165-Ball FBGA Boundary Scan Order (x36)

FBGA BIT#	SIGNAL NAME	BALL ID
1	MODE (LB0#)	1R
2	SA	6N
3	SA	11P
4	SA	8P
5	SA	8R
6	SA	9R
7	SA	9P
8	SA	10P
9	SA	10R
10	SA	11R
11	ZZ	11H
12	NF/DQPa	11N
13	DQa	11M
14	DQa	11L
15	DQa	11K
16	DQa	11J
17	DQa	10M
18	DQa	10L
19	DQa	10K
20	DQa	10J
21	DQb	11G
22	DQb	11F
23	DQb	11E
24	DQb	11D
25	DQb	10G
26	DQb	10F
27	DQb	10E
28	DQb	10D
29	NF/DQPb	11C
30	NC	11A
31	SA	10A
32	SA	10B
33	ADV#	9A
34	ADSP#	9B
35	ADSC#	8A
36	OE# (G#)	8B
37	BWE#	7A
38	GW#	7B
39	CLK	6B

165-Ball FBGA Boundary Scan Order (x36)

FBGA BIT#	SIGNAL NAME	BALL ID
40	NC	11B
41	NC	1A
42	CE2#	6A
43	BWa#	5B
44	BWb#	5A
45	BWc#	4A
46	BWd#	4B
47	CE2	3B
48	CE#	3A
49	SA	2A
50	SA	2B
51	NC	1B
52	NF/DQPc	1C
53	DQc	1D
54	DQc	1E
55	DQc	1F
56	DQc	1G
57	DQc	2D
58	DQc	2E
59	DQc	2F
60	DQc	2G
61	DQd	1J
62	DQd	1K
63	DQd	1L
64	DQd	1M
65	DQd	2J
66	DQd	2K
67	DQd	2L
68	DQd	2M
69	NF/DQPd	1N
70	SA	3P
71	SA	3R
72	SA	4R
73	SA	4P
74	SA1	6P
75	SA0	6R

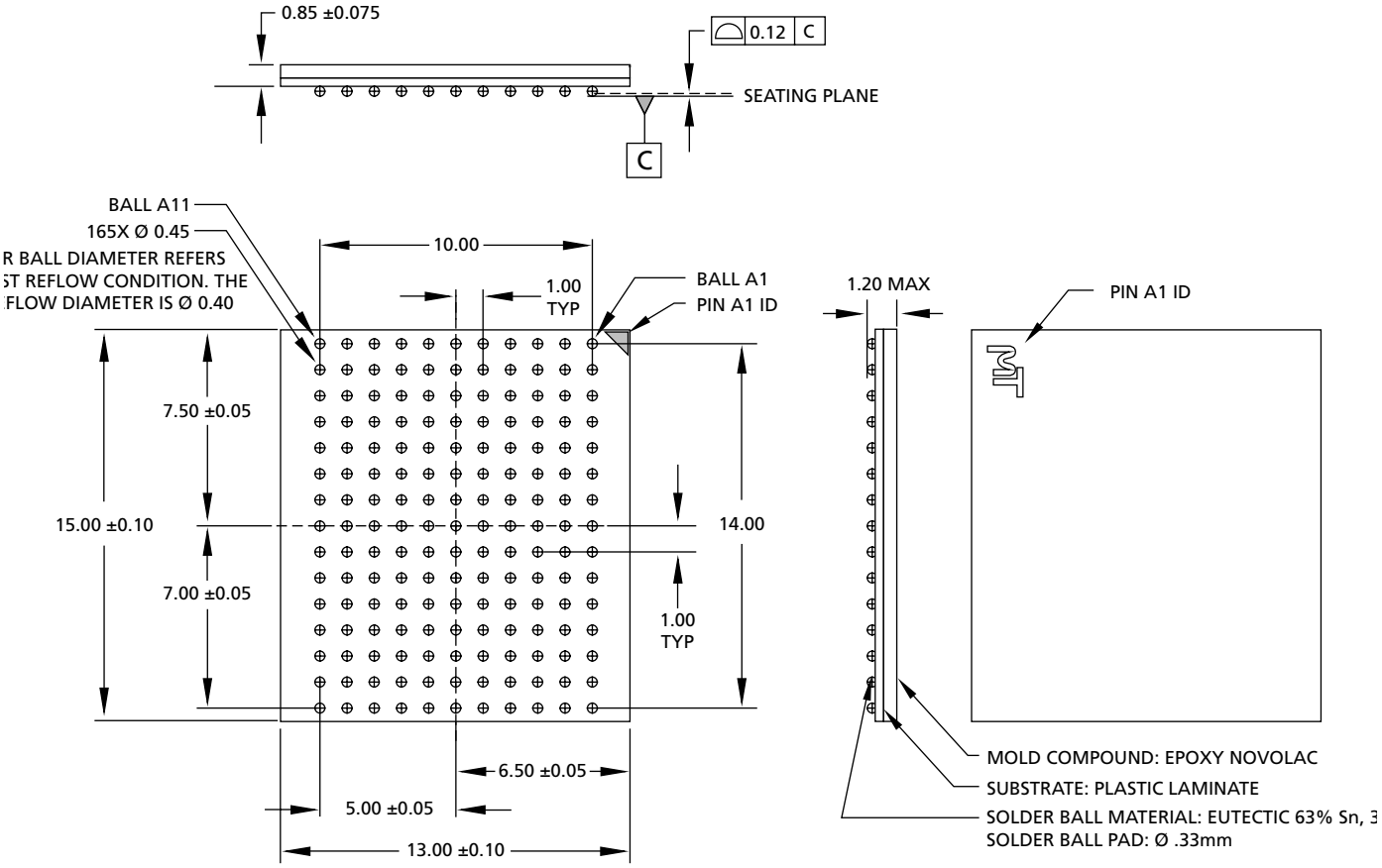
100-PIN PLASTIC TQFP (JEDEC LQFP)



Notes: **1.** All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

165-BALL FBGA



Notes: **1.** All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

DATA SHEET DESIGNATION

Advance: This data sheet contains initial descriptions of products still under development.

REVISION HISTORY

- Rev. A, Pub. 6 /02 ..... 6/02

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