

HIGH-PERFORMANCE PRODUCTS
Description

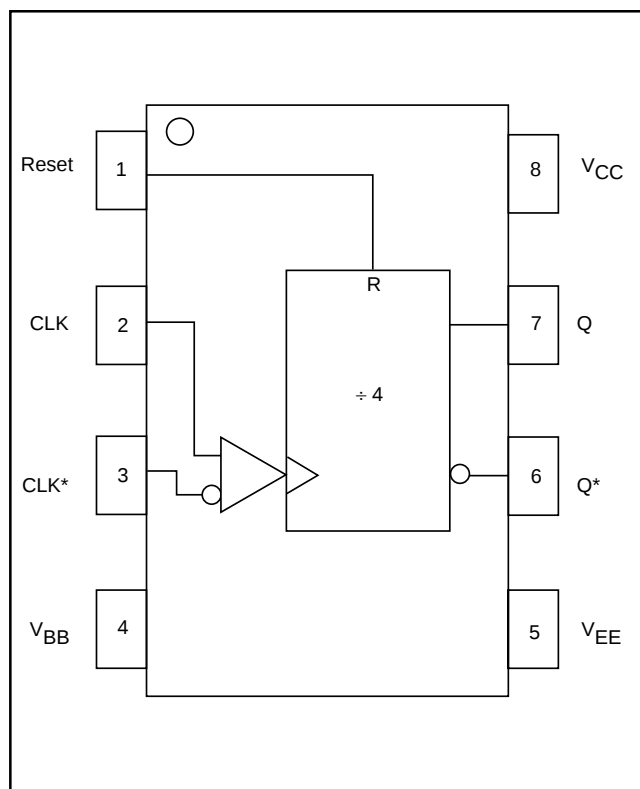
The SK10/100EL33W is a ÷4 Divider. This device is fully compatible with MC10/100EL33 and MC10/100LVEL33.

The SK10/100EL33W provides a V_{BB} output for either single-ended use or as a DC bias for AC coupling to the device. The V_{BB} pin should be used only as a bias for the SK10/100EL33W as its current sink/source capability is limited. Whenever used, the V_{BB} pin should be bypassed to V_{CC} via a 0.01 μ F capacitor.

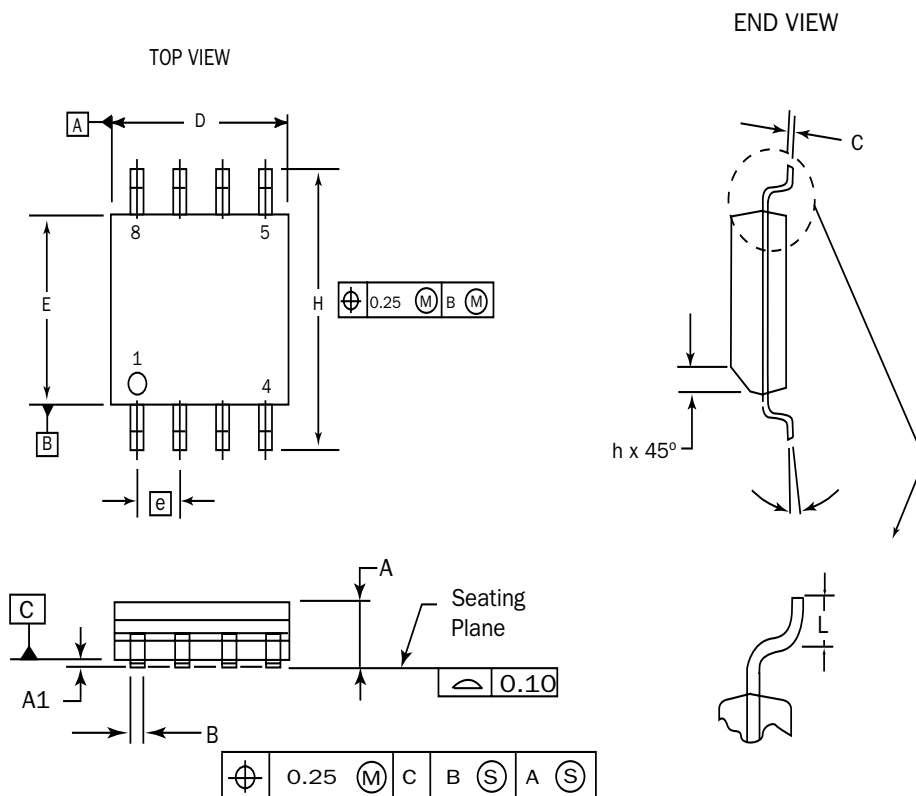
The Reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state. The Reset pin allows for the synchronization of multiple EL33W's in a system.

Features

- Extended Supply Voltage Range: ($V_{EE} = -5.5V$ to $-3.0V$, $V_{CC} = 0V$) or ($V_{CC} = +3.0V$ to $+5.5V$, $V_{EE} = 0V$)
- High Bandwidth Output Transition
- 560 ps (Typ.) Propagation Delay
- V_{BB} Output
- 75K Ω Internal Input Pulldown Resistor
- 4.0 GHz Toggle Frequency
- New Differential Input Common Mode Range
- Fully Compatible with MC10/100EL33 and MC10/100LVEL33
- ESD Protection of >4000V
- Industrial Temperature Range: $-40^{\circ}C$ to $85^{\circ}C$
- Available in 8-Pin SOIC (150 mils) Package
- Flammability Rate: UL-94 code V-0
- Moisture sensitivity: Level 1

Functional Block Diagram

Pin Description

Pin	Function
CLK, CLK*	Differential Clock Inputs
Q, Q*	Differential Clock Outputs
Reset	Asynch Reset
V_{BB}	Reference Output Voltage

8 Pin SOIC Package
8 Lead SOIC Package


DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

NOTES:

1. Dimensions are in millimeters.
2. Dimensions D and E do not include mold protrusion.
3. Maximum mold protrusion 0.15 per side.
4. Dimension B does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.127 total in excess of the B dimension at maximum material condition.

HIGH-PERFORMANCE PRODUCTS
DC Characteristics
SK10/100EL33W DC Electrical Characteristics (Notes 1, 2, 6)
 $(V_{CC} - V_{EE} = 3.0V \text{ to } 5.5V; V_{OUT} \text{ Loaded } 50\Omega \text{ to } V_{CC} - 2.0V)$

Symbol	Characteristic	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input Current (Diff) (SE)	-150		150 150	-150		150 150	-150		150 150	-150		150 150	μA μA
I_{EE}	Power Supply Current 10EL 100EL	16 20	23 27	30 38	16 20	23 27	30 38	16 20	23 27	30 38	16 20	23 27	30 38	mA mA
V_{BB}	Output Reference Voltage ⁵ 10EL 100EL	-1.43 -1.38		-1.30 -1.26	-1.38 -1.38		-1.27 -1.26	-1.35 -1.38		-1.25 -1.26	-1.31 -1.38		-1.19 -1.26	V V

AC Characteristics
SK10/100EL33W AC Characteristics (Notes 1, 2)
 $(V_{CC} - V_{EE} = 3.0V \text{ to } 5.5V; V_{OUT} \text{ Loaded } 50\Omega \text{ to } V_{CC} - 2.0V)$

Symbol	Characteristic	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	3.4	4.2		3.8	4.2		3.8	4.2		3.8	4.2		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q Reset to Q	500 380	570 424	640 470	510 390	555 435	600 480	510 400	560 445	610 490	520 410	585 455	650 500	ps ps
t_{skew}	Duty Cycle Skew			20			20			20			20	ps
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, Q*	110	145	195	110	155	200	120	160	210	120	175	225	ps
V_{PP}^3	Minimum Input Swing	150		1000	150		1000	150		1000	150		1000	mV
V_{CMR}^4	Common Mode Range	$V_{EE} + 1.7$		$V_{CC} - 0.4$	$V_{EE} + 1.7$		$V_{CC} - 0.4$	$V_{EE} + 1.7$		$V_{CC} - 0.4$	$V_{EE} + 1.7$		$V_{CC} - 0.4$	V

HIGH-PERFORMANCE PRODUCTS**AC Characteristics *(continued)*****Notes:**

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to $V_{CC} - 2.0V$ except where otherwise specified on the individual data sheets.
2. 100K circuits are designed to meet the DC specifications shown in the table where transverse airflow greater than 500 lfpm is maintained.
3. Minimum input swing for which AC parameters are guaranteed.
4. CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between $V_{PP(min)}$ and 1V. The lower end of the CMR range varies 1:1 with VEE and is equal to $VEE + 1.7V$.
5. Voltages referenced to $V_{CC} = 0V$.
6. For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
7. For part ordering description, see HPP Part Ordering Information Data Sheet.

Application Notes

AN1003 - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices

AN1005 - Using ECL / LVECL Devices as PECL / LVPECL

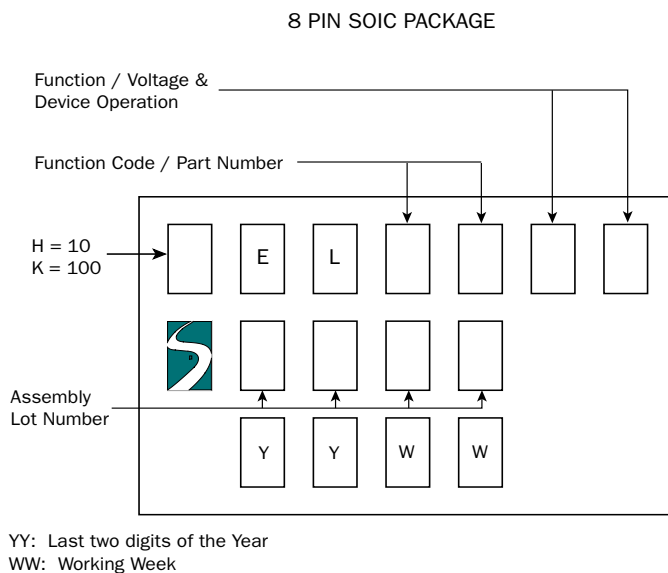
AN1006 - Designing with 10K and 100K ECL / PECL Devices

HIGH-PERFORMANCE PRODUCTS

Ordering Information

Ordering Code	Package ID
SK10EL33WD	8-SOIC
SK10EL33WDT	8-SOIC
SK100EL33WD	8-SOIC
SK100EL33WDT	8-SOIC
SK10EL33WU	Die
SK100EL33WU	Die

Marking Information



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