# Dual Channel Differential VDSL2 Line Driver

## ISL1539

The ISL1539 is to be used for high performance long reach and high speed applications, including ADSL2, ADSL2+, and VDSL2 20dBm.

The ISL1539 is an integral part of the signal chain. The driver has been optimized for flat gain response and reduced harmonic distortion and noise in the bands of interest to improve the overall signal to noise in the system.

These drivers achieve a total harmonic distortion (THD) measurement of typically -60dB MTPR @ 1.1MHz, while consuming typically 10mA per DSL channel of total supply current. This supply current can be set using a resistor on the $I_{ADJ}$ pin. Two other pins ($C_0$ and $C_1$) can also be used to adjust supply current to one of four pre-set modes (full-$I_S$, 3/4-$I_S$, 1/2-$I_S$, and full power-down). The ISL1539 operates on ±5V to ±15V supplies and retains its bandwidth and linearity over the complete supply range.

The device is supplied in the small footprint (4mmx5mm) 24 Ld QFN package and is specified for operation over the full -40°C to +85°C temperature range.

## Features

- 450mA output drive capability
- 44.1$V_{P-P}$ differential output drive into 100Ω
- -85dBc THD @ 1MHz 2$V_{P-P}$
- High slew rate of 1200V/µs differential
- Bandwidth - 80MHz @ $A_V$ = 10
- Current control pins
- Channel separation
  - 80dB @ 500kHz
  - 75dB @ 1MHz
  - 60dB @ 4MHz
- Pb-free (RoHS compliant)

## Applications

- VDSL2 20dBm
- ADSL2++

## Ordering Information

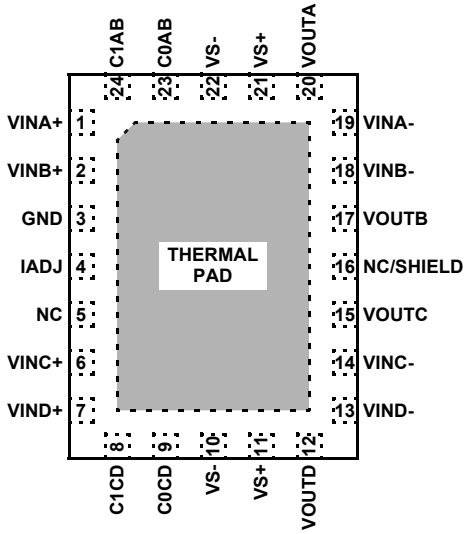
| PART NUMBER (Notes 2, 3) | PART MARKING | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|
| ISL1539IRZ | 1539 IRZ | 24 Ld QFN | MDP0046 |
| ISL1539IRZ-T7 (Note 1) | 1539 IRZ | 24 Ld QFN | MDP0046 |
| ISL1539IRZ-T13 (Note 1) | 1539 IRZ | 24 Ld QFN | MDP0046 |

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL1539. For more information on MSL, please see tech brief TB363

## Pin Configuration

ISL1539
(24 LD QFN)
TOP VIEW



## Absolute Maximum Ratings ($T_A$ = +25°C)

$V_S$+ to $V_S$- Supply Voltage . . . . . -0.3V to +30V
$V_S$+ Voltage to GND . . . . . -0.3V to +30V
$V_S$- Voltage to GND . . . . . -30V to +0.3V
Driver $V_{IN}$+ Voltage . . . . . $V_S$- to $V_S$+
$C_0$, $C_1$ Voltage to GND . . . . . -0.3V to +6V
$I_{ADJ}$ Voltage to GND . . . . . -0.3V to +4V
Current into any Input . . . . . 8mA
Output Current from Driver (Static) . . . . . 50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . . . 3kV
Machine Model (Per EIAJ ED-4701 Method C-111) . . . . . 250V

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 24 Ld QFN Package | 38 | N/A |

Power Dissipation . . . . . See curves on page 8 and page 8
Storage Temperature Range . . . . . -65°C to +150°C
Operating Temperature Range . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . -40°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## Electrical Specifications

$V_S$ = ±12V, $R_F$ = 3kΩ, $R_L$ = 65Ω, $I_{ADJ}$ = $C_0$ = $C_1$ = 0V, $T_A$ = +25°C. Amplifiers tested separately.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 4) | TYP | MAX (Note 4) | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CHARACTERISTICS** | | | | | | |
| $I_S$+ (Full $I_S$) | Positive Supply Current per Amplifier | All outputs at 0V, $C_0$ = $C_1$ = 0V, $R_{ADJ}$ = 0 | 7.5 | 10 | 12.5 | mA |
| $I_S$- (Full $I_S$) | Negative Supply Current per Amplifier | All outputs at 0V, $C_0$ = $C_1$ = 0V, $R_{ADJ}$ = 0 | -12.4 | -9.9 | -7.4 | mA |
| $I_S$+ (3/4 $I_S$) | Positive Supply Current per Amplifier | All outputs at 0V, $C_0$ = 5V, $C_1$ = 0V, $R_{ADJ}$ = 0 | | 7.5 | | mA |
| $I_S$- (3/4 $I_S$) | Negative Supply Current per Amplifier | All outputs at 0V, $C_0$ = 5V, $C_1$ = 0V, $R_{ADJ}$ = 0 | | -7.4 | | mA |
| $I_S$+ (1/2 $I_S$) | Positive Supply Current per Amplifier | All outputs at 0V, $C_0$ = 0V, $C_1$ = 5V, $R_{ADJ}$ = 0 | 3.7 | 5.1 | 6.3 | mA |
| $I_S$- (1/2 $I_S$) | Negative Supply Current per Amplifier | All outputs at 0V, $C_0$ = 0V, $C_1$ = 5V, $R_{ADJ}$ = 0 | -6.2 | -5 | -3.5 | mA |
| $I_S$+ (Power-down) | Positive Supply Current per Amplifier | All outputs at 0V, $C_0$ = $C_1$ = 5V, $R_{ADJ}$ = 0 | | 0.1 | 1.0 | mA |
| $I_S$- (Power-down) | Negative Supply Current per Amplifier | All outputs at 0V, $C_0$ = $C_1$ = 5V, $R_{ADJ}$ = 0 | -1.0 | 0 | | mA |
| $I_{GND}$ | GND Supply Current per Amplifier | All outputs at 0V | | 0.1 | | mA |
| **INPUT CHARACTERISTICS** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | | -2 | +1 | +2 | mV |
| $\Delta V_{OS}$ | $V_{OS}$ Mismatch | | -5 | 0 | +5 | mV |
| $I_B$+ | Non-Inverting Input Bias Current | | -10 | | +10 | µA |
| $I_B$- | Inverting Input Bias Current | | -75 | | +60 | µA |
| $\Delta I_B$- | $I_B$- Mismatch | | -15 | 0 | +15 | µA |
| $R_{OL}$ | Transimpedance | | | 3 | | MΩ |
| $e_N$ | Input Noise Voltage | | | 2.7 | | nV/√Hz |
| $i_N$ | -Input Noise Current | | | 19 | | pA/√Hz |
| $V_{IH}$ | Input High Voltage | $C_0$ and $C_1$ inputs, with signal | 1.8 | | | V |
| | | $C_0$ and $C_1$ inputs, without signal | 1.6 | | | V |
| $V_{IL}$ | Input Low Voltage | $C_0$ and $C_1$ inputs | | | 0.8 | V |
| $I_{IH0}$ , $I_{IH1}$ | Input High Current for $C_0$, $C_1$ | $C_0$ = 5V, $C_1$ = 5V | 10 | | 40 | µA |
| $I_{IL0}$, $I_{IL1}$ | Input Low Current for $C_0$ or $C_1$ | $C_0$ = 0V, $C_1$ = 0V | -15 | | -4.0 | µA |

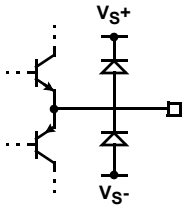
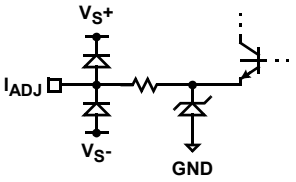
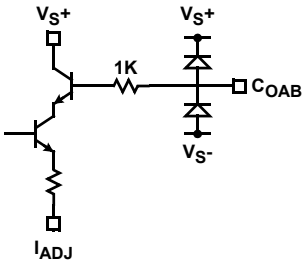
## Electrical Specifications $V_S$ = ±12V, $R_F$ = 3kΩ, $R_L$ = 65Ω, $I_{ADJ}$ = $C_0$ = $C_1$ = 0V, $T_A$ = +25°C. Amplifiers tested separately. **(Continued)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 4) | TYP | MAX (Note 4) | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OUT}$ | Loaded Output Swing ($R_L$ Single-ended to GND) | $R_L$ = 100Ω | | ±11.1 | | V |
| | | $R_L$ = 50Ω(+) | 10.65 | 10.95 | | V |
| | | $R_L$ = 50Ω (-) | | -10.95 | -10.55 | V |
| | | $R_L$ = 25Ω (+) | 9.8 | 10.7 | | V |
| | | $R_L$ = 25Ω (-) | | -10.7 | -9.2 | V |
| $I_{OL}$ | Linear Output Current | $A_V$ = 5, $R_L$ = 10Ω f = 100kHz, THD = -60dBc (10Ω single-ended) | | 450 | | mA |
| $I_{OUT}$ | Output Current | $V_{OUT}$ = 1V, $R_L$ = 1Ω | | 1 | | A |
| **DYNAMIC PERFORMANCE** | | | | | | |
| BW | -3dB Bandwidth | $A_V$ = +10 | | 80 | | MHz |
| HD2 at 200kHz | 2nd Harmonic Distortion at 200kHz | $f_C$ = 200kHz, $R_L$ = 100Ω, $V_{OUT}$ = $2V_{P-P}$ | | -90 | | dBc |
| HD3 at 200kHz | 3rd Harmonic Distortion at 200kHz | $f_C$ = 200kHz, $R_L$ = 100Ω, $V_{OUT}$ = $2V_{P-P}$ | | -94 | | dBc |
| THD at 200kHz | Total Harmonic Distortion at 200kHz | $f_C$ = 200kHz, $R_L$ = 100Ω, $V_{OUT}$ = $2V_{P-P}$ | | -89 | | dBc |
| HD2 at 1MHz | 2nd Harmonic Distortion at 1MHz | $f_C$ = 1MHz, $R_L$ = 100Ω, $V_{OUT}$ = $2V_{P-P}$ | | -86 | | dBc |
| | | $f_C$ = 1MHz, $R_L$ = 25Ω, $V_{OUT}$ = $2V_{P-P}$ | | -80 | | dBc |
| HD3 at 1MHz | 3rd Harmonic Distortion at 1MHz | $f_C$ = 1MHz, $R_L$ = 100Ω, $V_{OUT}$ = $2V_{P-P}$ | | -90 | | dBc |
| | | $f_C$ = 1MHz, $R_L$ = 25Ω, $V_{OUT}$ = $2V_{P-P}$ | | -75 | | dBc |
| THD at 1MHz | Total Harmonic Distortion at 1MHz | $f_C$ = 1MHz, $R_L$ = 100Ω $V_{OUT}$ = $2V_{P-P}$ | | -85 | | dBc |
| MTPR | Multi-Tone Power Ratio | 26kHz to 1.1MHz, $R_{LINE}$ = 100Ω, $P_{LINE}$ = 20.4dBM | | -70 | | dBc |
| SR | Slewrate (single-ended) | $V_{OUT}$ from -8V to +8V measured at ±4V | | 500 | | V/µs |

NOTE:

4. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

# Pin Descriptions

| ISL1539IR (QFN24) | PIN NAME | FUNCTION | CIRCUIT |
|---|---|---|---|
| 1 | VINA+ | Amplifier A non-inverting input |  CIRCUIT 1 |
| 2 | VINB+ | Amplifier B non-inverting input | (Reference Circuit 1) |
| 3 | GND | Ground connection | |
| 4 | IADJ (Note 5) | Supply current control pin for both DSL channels #1 and #2 |  CIRCUIT 2 |
| 5 | NC | Not connected | |
| 6 | VINC+ | Amplifier C non-inverting input | (Reference Circuit 1) |
| 7 | VIND+ | Amplifier D non-inverting input | (Reference Circuit 1) |
| 8 | C1CD (Note 6) | DSL channel #2 current control pin |  CIRCUIT 3 |
| 9 | C0CD (Note 6) | DSL channel #2 current control pin | (Reference Circuit 3) |
| 10, 22 | VS- | Negative supply | |
| 11, 21 | VS+ | Positive supply | |
| 12 | VOUTD | Amplifier D output | (Reference Circuit 1) |
| 13 | VIND- | Amplifier D inverting input | (Reference Circuit 1) |
| 14 | VINC- | Amplifier C inverting input | (Reference Circuit 1) |
| 15 | VOUTC | Amplifier C output | (Reference Circuit 1) |
| 16 | NC/SHIELD | | |
| 17 | VOUTB | Amplifier B output | (Reference Circuit 1) |

## Pin Descriptions (Continued)

| ISL1539IR (QFN24) | PIN NAME | FUNCTION | CIRCUIT |
|---|---|---|---|
| 18 | VINB- | Amplifier B inverting input | (Reference Circuit 1) |
| 19 | VINA- | Amplifier A inverting input | (Reference Circuit 1) |
| 20 | VOUTA | Amplifier A output | (Reference Circuit 1) |
| 23 | C0AB (Note 7) | DSL channel #1 current control pin | (Reference Circuit 3) |
| 24 | C1AB (Note 7) | DSL channel #1 current control pin | (Reference Circuit 3) |

NOTES:

5. $I_{ADJ}$ controls bias current ($I_S$) setting for both DSL channels.
6. Amplifiers C and D comprise DSL channel #2. $C_{0CD}$ and $C_{1CD}$ control $I_S$ settings for DSL channel #2.
7. Amplifiers A and B comprise DSL channel #1. $C_{0AB}$ and $C_{1AB}$ control $I_S$ settings for DSL channel #1.

## Typical Performance Curves

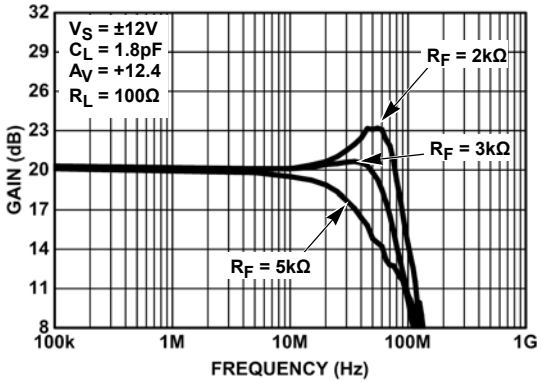



FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS $R_F$ (FULL POWER MODE)

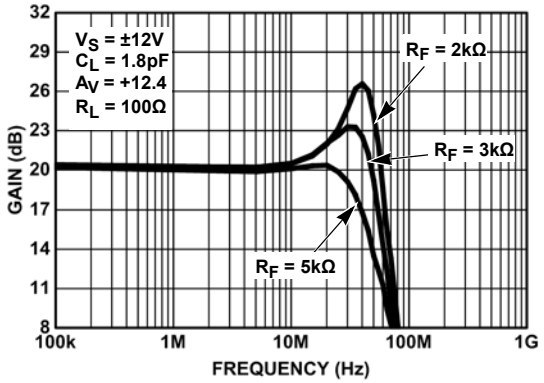



FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS $R_F$ (HALF POWER MODE)

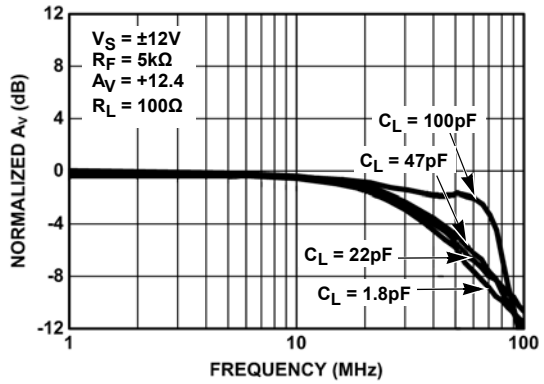



FIGURE 3. FREQUENCY RESPONSE FOR VARIOUS $C_L$ (FULL POWER MODE)

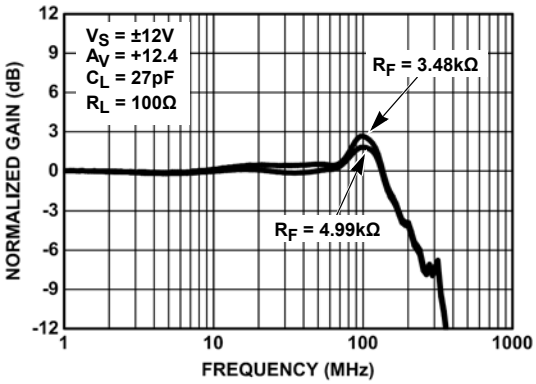



FIGURE 4. COMMON MODE FREQUENCY RESPONSE FOR VARIOUS $R_F$ (FULL POWER MODE)

## Typical Performance Curves (Continued)

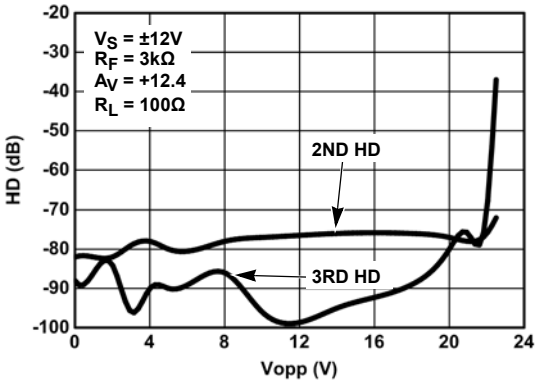



FIGURE 5. 200KHz 2ND AND 3RD HARMONIC DISTORTION vs VOLTAGE OUTPUT (FULL POWER MODE)

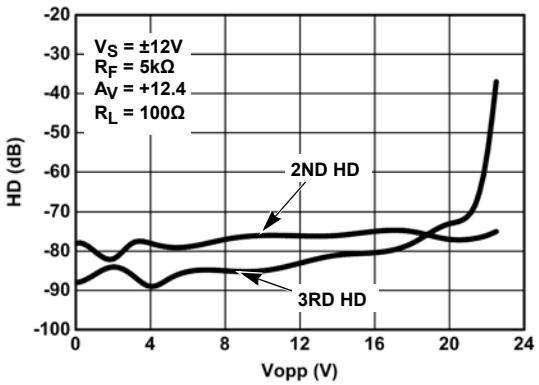



FIGURE 6. 200kHz 2ND AND 3RD HARMONIC DISTORTION vs VOLTAGE OUTPUT (HALF POWER MODE)

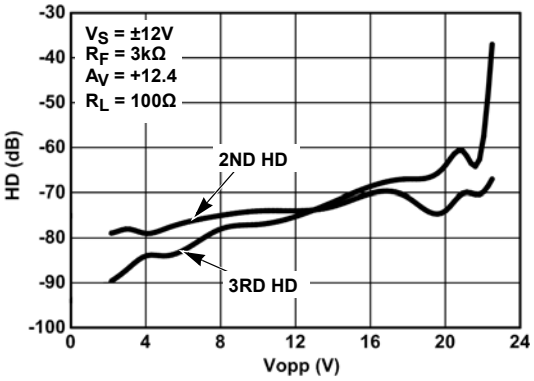



FIGURE 7. 1MHz 2ND AND 3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE (FULL POWER MODE)

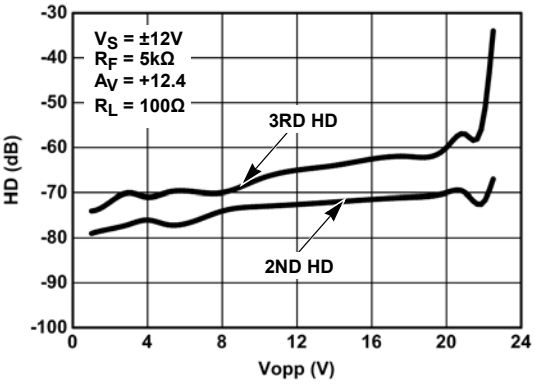



FIGURE 8. 1MHz 2ND AND 3RD HARMONIC DISTORTION vs OUPUT VOLTAGE (HALF POWER MODE)

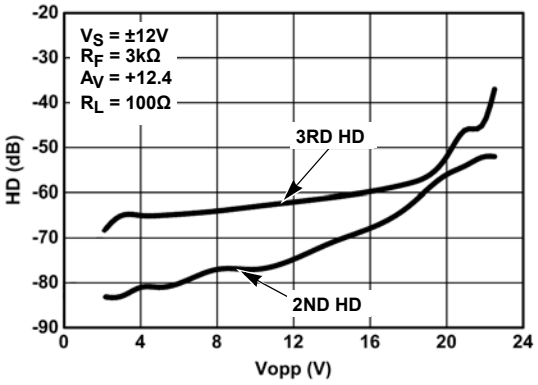



FIGURE 9. 3.75MHz 2ND AND 3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE (FULL POWER MODE)

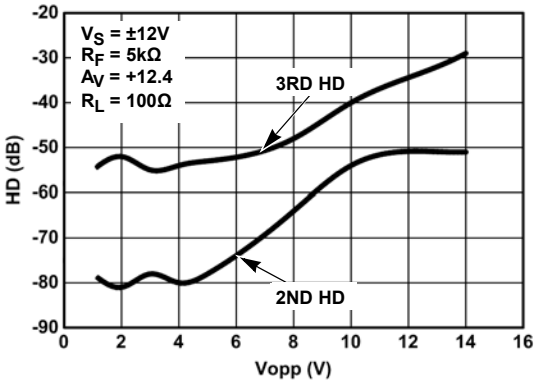



FIGURE 10. 3.75MHz 2ND AND 3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE (HALF POWER MODE)

## Typical Performance Curves (Continued)

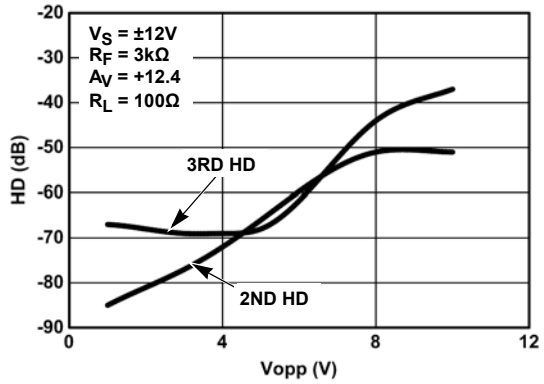



FIGURE 11. 10MHz 2ND AND 3RD HARMONIC DISTORTION vs OUTPUT VOLTAGE (FULL POWER MODE)

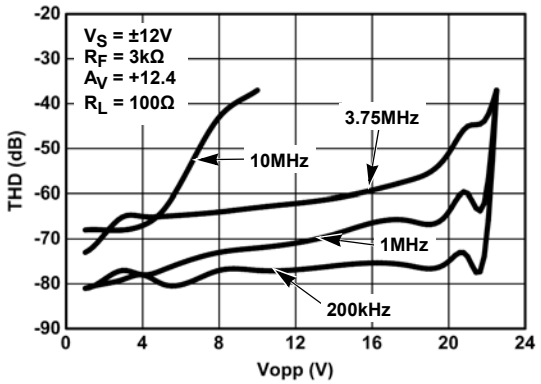



FIGURE 12. TOTAL HARMONIC DISTORTION FOR VARIOUS FREQUENCIES (FULL POWER MODE)

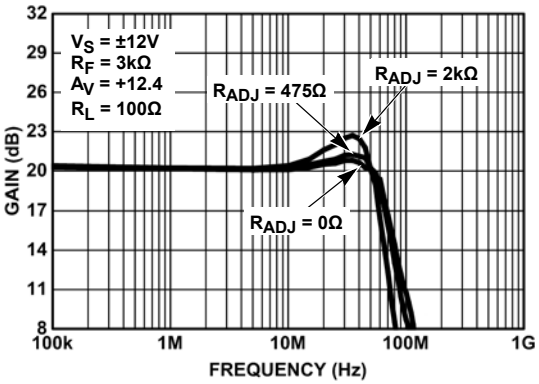



FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS $R_{ADJ}$

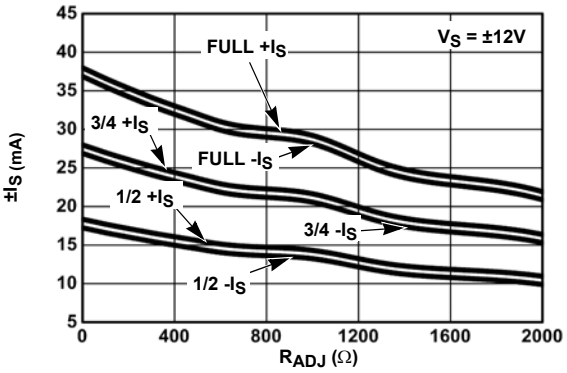



FIGURE 14. SUPPLY CURRENT vs $R_{ADJ}$ FOR VARIOUS POWER MODE

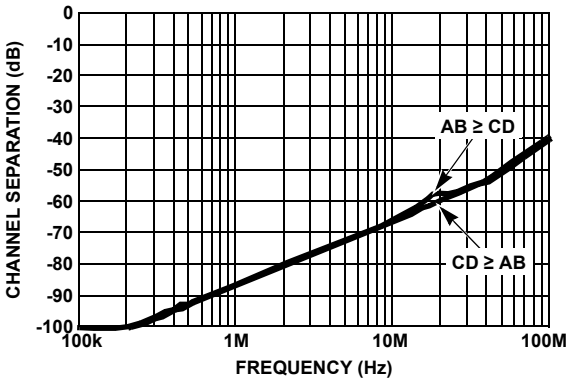



FIGURE 15. CHANNEL SEPARATION vs FREQUENCY

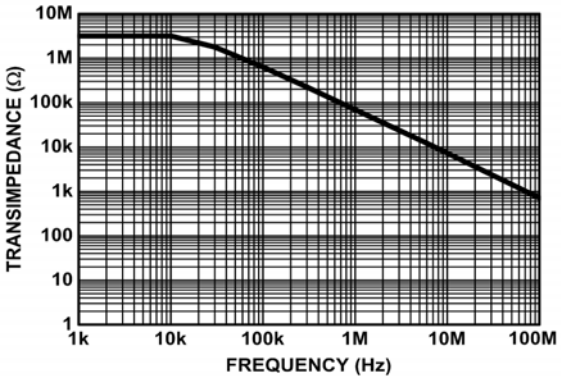



FIGURE 16. TRANSIMPEDANCE

## Typical Performance Curves (Continued)

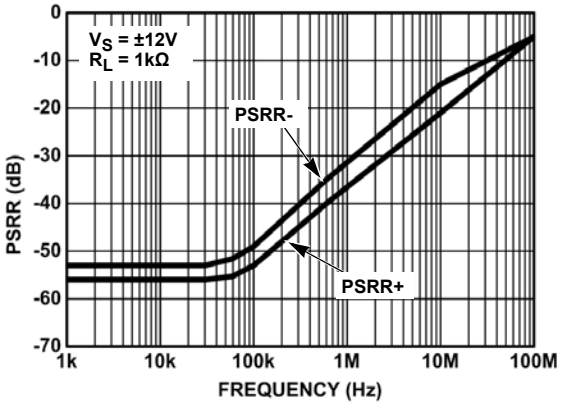



FIGURE 17. PSRR vs FREQUENCY

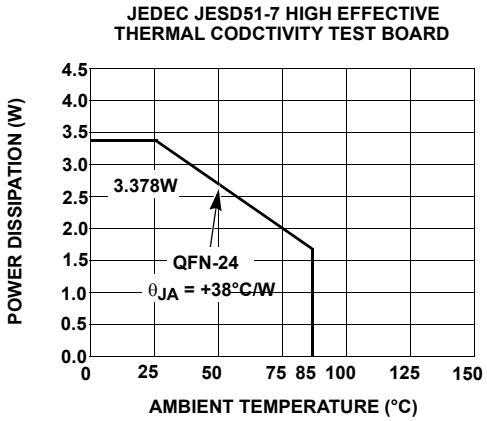



FIGURE 18. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

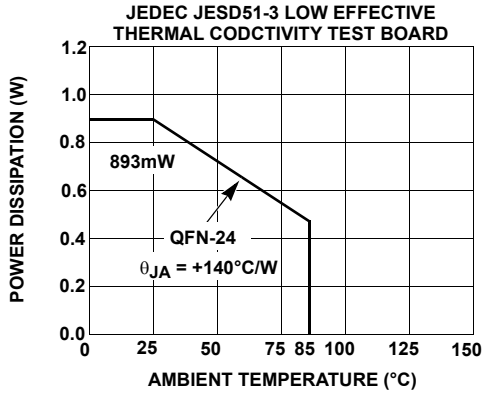



FIGURE 19. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

## Application Information

The ISL1539 consists of two sets of high-power line driver amplifiers that can be connected for full duplex differential line transmission. The amplifiers are designed to be used with signals up to 30MHz and produce low distortion levels. A typical interface circuit is shown in Figure 20.

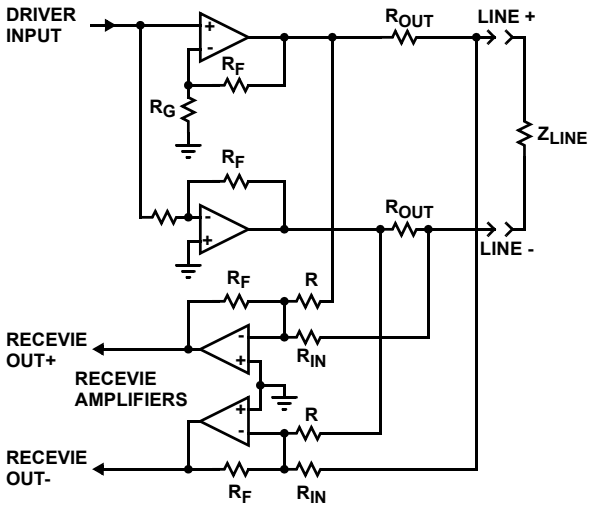



FIGURE 20. TYPICAL LINE INTERFACE CONNECTION

The amplifiers are wired with one in positive gain and the other in a negative gain configuration to generate a differential output for a single-ended input. They will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers RF's need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver.

If a differential signal is available to the drive amplifiers, they may be wired so:

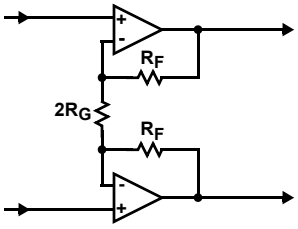



FIGURE 21. DRIVERS WIRED FOR DIFFERENTIAL INPUT

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

## Power Supplies and Dissipation

Due to the high power drive capability of the ISL1539, much attention needs to be paid to power dissipation. The power that needs to be dissipated in the ISL1539 has two main contributors. The first is the quiescent current dissipation. The second is the dissipation of the output stage.

The quiescent power in the ISL1539 is not constant with varying outputs. In reality, 7mA of the 15mA needed to power the drivers is converted in to output current. Therefore, in the equation below we should subtract the average output current, $I_O$, or 7mA, whichever is the lowest. We'll call this term $I_X$.

Therefore, we can determine a quiescent current with Equation 1:

$$P_{Dquiescent} = V_S \times (I_S - 2I_X) \quad \text{(EQ. 1)}$$

where:

- $V_S$ is the supply voltage ($V_S$+ to $V_S$-)
- $I_S$ is the maximum quiescent supply current ($I_S$+ + $I_S$-)
- $I_X$ is the lesser of $I_O$ or 7mA (generally $I_X$ = 7mA)

The dissipation in the output stage has two main contributors. Firstly, we have the average voltage drop across the output transistor and secondly, the average output current. For minimal power dissipation, the user should select the supply voltage and the line transformer ratio accordingly. The supply voltage should be kept as low as possible, while the transformer ratio should be selected so that the peak voltage required from the ISL1539 is close to the maximum available output swing. There is a trade off, however, with the selection of transformer ratio. As the ratio is increased, the receive signal available to the receivers is reduced.

Once the user has selected the transformer ratio, the dissipation in the output stages can be selected with Equation 2:

$$P_{Dtransistors} = 2 \times \overline{I_O} \times \left(\frac{V_S}{2} - \overline{V_O}\right) \quad \text{(EQ. 2)}$$

where:

- $V_S$ is the supply voltage ($V_S$+ to $V_S$-)
- $V_O$ is the average output voltage per channel
- $I_O$ is the average output current per channel

The overall power dissipation ($P_{DISS}$) is obtained by adding $P_{Dquiescent}$ and $P_{Dtransistor}$.

Then, the $\theta_{JA}$ requirement needs to be calculated. This is done using Equation 3:

$$\theta_{JA} = \frac{(T_{JUNCT} - T_{AMB})}{P_{DISS}} \quad \text{(EQ. 3)}$$

where:

- $T_{JUNCT}$ is the maximum die temperature (+150°C)
- $T_{AMB}$ is the maximum ambient temperature
- $P_{DISS}$ is the dissipation calculated above
- $\theta_{JA}$ is the junction to ambient thermal resistance for the package when mounted on the PCB

This $\theta_{JA}$ value is then used to calculate the area of copper needed on the board to dissipate the power.

The IRE and QFN power packages are designed so that heat may be conducted away from the device in an efficient manner. To disperse this heat, the bottom diepad is internally connected to the mounting platform of the die. Heat flows through the diepad into the circuit board copper, then spreads and convects to air. Thus, the ground plane on the component side of the board becomes the heatsink. This has proven to be a very effective technique. $\theta_{JA}$ of +30°C/W can be achieved.

## Single Supply Operation

The ISL1539 can also be powered from a single supply voltage. When operating in this mode, the GND pins can still be connected directly to GND. To calculate power dissipation, the equations in the previous section should be used, with $V_S$ equal to half the supply rail.

## Output Loading

While the drive amplifiers can output in excess of 450mA transiently, the internal metallization is not designed to carry more than 75mA of steady DC current and there is no current-limit mechanism. This allows safely driving rms sinusoidal currents of 2mAx75mA, or 150mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

## Power Supplies

The power supplies should be well bypassed close to the ISL1539. A 3.3µF tantalum capacitor for each supply works well. Since the load currents are differential, they should not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no such ground loops will occur. This scheme is employed in the layout of the EL1537 demonstration board, and documentation can be obtained from the factory.

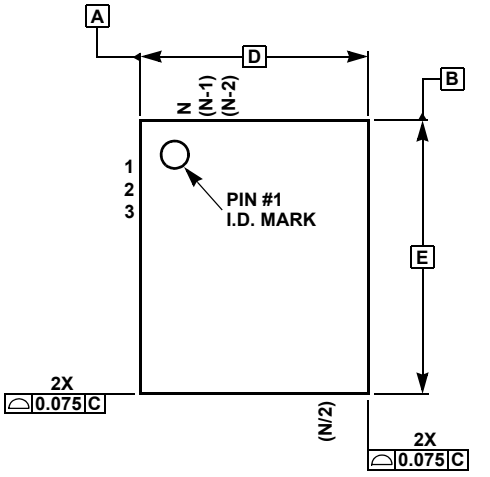
## Power Control Function

The ISL1539 contains two forms of power control operation. Two digital inputs, $C_0$ and $C_1$, can be used to control the supply current of the ISL1539 drive amplifiers. As the supply current is reduced, the ISL1539 will start to exhibit slightly higher levels of distortion and the frequency response will be limited. The four power modes of the ISL1539 are set up as shown in the table1 below.

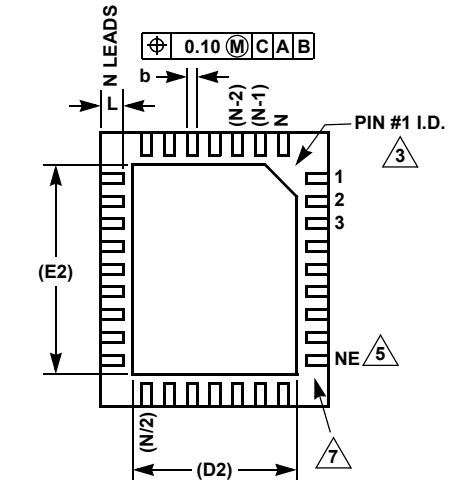
**TABLE 1. POWER MODES OF THE EL15371**

| $C_1$ | $C_0$ | Operation |
|---|---|---|
| 0 | 0 | $I_S$ Full Power Mode |
| 0 | 1 | 3/4-$I_S$ Power Mode |
| 1 | 0 | 1/2-$I_S$ Power Mode |
| 1 | 1 | Power Down |

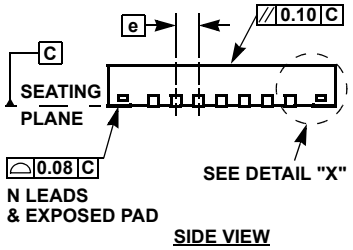
# QFN (Quad Flat No-Lead) Package Family



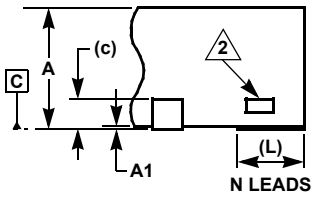

TOP VIEW




BOTTOM VIEW




SIDE VIEW




DETAIL X

## MDP0046

**QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY (COMPLIANT TO JEDEC MO-220)**

| SYMBOL | MILLIMETERS | | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|
| | QFN44 | QFN38 | QFN32 | | | |
| A | 0.90 | 0.90 | 0.90 | 0.90 | ±0.10 | - |
| A1 | 0.02 | 0.02 | 0.02 | 0.02 | +0.03/-0.02 | - |
| b | 0.25 | 0.25 | 0.23 | 0.22 | ±0.02 | - |
| c | 0.20 | 0.20 | 0.20 | 0.20 | Reference | - |
| D | 7.00 | 5.00 | 8.00 | 5.00 | Basic | - |
| D2 | 5.10 | 3.80 | 5.80 | 3.60/2.48 | Reference | 8 |
| E | 7.00 | 7.00 | 8.00 | 6.00 | Basic | - |
| E2 | 5.10 | 5.80 | 5.80 | 4.60/3.40 | Reference | 8 |
| e | 0.50 | 0.50 | 0.80 | 0.50 | Basic | - |
| L | 0.55 | 0.40 | 0.53 | 0.50 | ±0.05 | - |
| N | 44 | 38 | 32 | 32 | Reference | 4 |
| ND | 11 | 7 | 8 | 7 | Reference | 6 |
| NE | 11 | 12 | 8 | 9 | Reference | 5 |

| SYMBOL | MILLIMETERS | | | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|---|
| | QFN28 | QFN24 | QFN20 | | QFN16 | | |
| A | 0.90 | 0.90 | 0.90 | 0.90 | 0.90 | ±0.10 | - |
| A1 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | +0.03/-0.02 | - |
| b | 0.25 | 0.25 | 0.30 | 0.25 | 0.33 | ±0.02 | - |
| c | 0.20 | 0.20 | 0.20 | 0.20 | 0.20 | Reference | - |
| D | 4.00 | 4.00 | 5.00 | 4.00 | 4.00 | Basic | - |
| D2 | 2.65 | 2.80 | 3.70 | 2.70 | 2.40 | Reference | - |
| E | 5.00 | 5.00 | 5.00 | 4.00 | 4.00 | Basic | - |
| E2 | 3.65 | 3.80 | 3.70 | 2.70 | 2.40 | Reference | - |
| e | 0.50 | 0.50 | 0.65 | 0.50 | 0.65 | Basic | - |
| L | 0.40 | 0.40 | 0.40 | 0.40 | 0.60 | ±0.05 | - |
| N | 28 | 24 | 20 | 20 | 16 | Reference | 4 |
| ND | 6 | 5 | 5 | 5 | 4 | Reference | 6 |
| NE | 8 | 7 | 5 | 5 | 4 | Reference | 5 |

Rev 11 2/07

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.