CRYSTAL OSCILLATOR

LOW-JITTER SAW OSCILLATOR

EG - 2121 / 2102CA

- Frequency range : 53.125 MHz to 700 MHz
- Supply voltage : 2.5 V ··· EG-2121CA
  3.3 V ··· EG-2102CA
- Output : Differential LV-PECL or LVDS or HCSL
- Function : Output enable (OE)
- External dimensions : 7.0 × 5.0 × 1.2 mm

- Very low jitter and low phase noise by SAW unit.

Pb Free RoHS Compliant

Product Number (please contact us)
EG-2121CA: Q3805CAx0xxxx00
: X1M000101xxxx00
EG-2102CA: Q3806CA00xxxx00
: X1M000091xxxx00

Actual size

EG-2121CA

EG-2102CA

Specifications (characteristics)

►Differential LV-PECL Output

Item	Symbol	EG-2121CA	EG-2102CA	Conditions / Remarks
		Differential LV-PECL		
Output frequency range	fo	53.125 MHz to 500 MHz	100 MHz to 700 MHz	Please contact us for inquiries regarding available frequencies.
Supply voltage	Vcc	2.5 V ±0.125 V	3.3 V ±0.3 V	
Storage temperature	T_stg	-40 °C to +100 °C		Store as bare product .
Operating temperature *1	T_use	P:0 °C to +70 °C ,R:-5 °C to +85 °C ,S:-20 °C to +70 °C		
Frequency tolerance *1	f_tol	G: ± 50 × 10^{-6} ,H: ±100 × 10^{-6}		
Current consumption	Icc	80 mA Max.	100 mA Max.	OE=Vcc, L_ECL=50 Ω
Disable current	I_dis	20 mA Max.	32 mA Max	OE=GND
Symmetry	SYM	P:40 % to 60 % (fo > 350 MHz)	P:45 % to 55 %	at outputs crossing point
		P:45 % to 55 % (fo ≤ 350 MHz)		
		D:48 % to 52 % (fo ≤ 175 MHz)	D:48 % to 52 % (fo ≤ 350 MHz)	
Output voltage	VOH	1.55 V Typ.	2.35 V Typ.	DC characteristics
		Vcc-1.025 V to Vcc-0.88 V		
	VOL	0.8 V Typ.	1.6 V Typ.	
		Vcc-1.81 V to Vcc-1.62 V		
Output load condition (ECL)	L_ECL	50 Ω		Terminated to Vcc -2.0 V
Input voltage	VIH	70 % Vcc Min.		OE terminal
	VIL	30 % Vcc Max.		
Rise time / Fall time	tr / tf	400 ps Max.		Between 20% and 80% of (VOH-VOL)
Start-up time	t_str	10 ms Max.		Time at minimum supply voltage to be 0 s
Phase Jitter	tPJ	0.8 ps Max.		fo < 100 MHz; Offset frequency: 12 kHz to 20 MHz
		0.5 ps Max.		100 MHz ≤ fo < 200 MHz; Offset frequency: 12 kHz to 20 MHz
		0.3 ps Max.		200 MHz ≤ fo; Offset frequency: 12 kHz to 20 MHz
Frequency aging *2	f_aging	± 10 × 10^{-6} / year Max.		+25 °C, First year, Vcc=2.5 V,3.3 V

*1 As per below table 1.
*2 Except: ***A

►LVDS Output

Item	Symbol	EG-2121CA	EG-2102CA	Conditions / Remarks
		LVDS		
Output frequency range	fo	53.125 MHz to 700 MHz		Please contact us for inquiries regarding available frequencies.
Supply voltage	Vcc	2.5 V ±0.125 V	3.3 V ±0.3 V	
Storage temperature	T_stg	-40 °C to +100 °C		Store as bare product.
Operating temperature *1	T_use	P:0 °C to +70 °C ,R:-5 °C to +85 °C ,S:-20 °C to +70 °C		
Frequency tolerance *1	f_tol	G: ± 50 × 10^{-6} ,H: ±100 × 10^{-6}		
Current consumption	Icc	30 mA Max	45 mA Max.	OE=Vcc, L_LVDS= 100 Ω
Disable current	I_dis	20 mA Max	30 mA Max.	OE=GND
Symmetry	SYM	L:40 % to 60 % (fo > 350 MHz)	L:40 % to 60 % (fo > 350 MHz)	at outputs crossing point
		L:45 % to 55 % (fo ≤ 350 MHz)	L:45 % to 55 % (fo ≤ 350 MHz)	
		V:48 % to 52 % (fo ≤ 175 MHz)	V:48 % to 52 % (fo ≤ 175 MHz)	
Output voltage	VOD	350 mV Typ. 247 mV to 454 mV		VOD1, VOD2; DC characteristics
	dVOD	50 mV Max.		dVOD = | VOD1-VOD2 |
	VOS	1.25 V Typ. 1.125 V to 1.375 V		VOS1, VOS2
	dVOS	150 mV Max.		dVOS = | VOS1-VOS2 |
Output load condition (LVDS)	L_LVDS	100 Ω		Connected between OUT to $\overline{OUT}$
Input voltage	VIH	70 % Vcc Min.		OE terminal
	VIL	30 % Vcc Max.		
Rise time / Fall time	tr / tf	400 ps Max.		Between 20 % and 80 %of Differential Output peek to peek voltage
Start-up time	t_str	10 ms Max.		Time at minimum supply voltage to be 0 s
Phase Jitter	tPJ	0.8 ps Max.		fo < 100 MHz; Offset frequency: 12 kHz to 20 MHz
		0.5 ps Max.		100 MHz ≤ fo < 200 MHz; Offset frequency: 12 kHz to 20 MHz
		0.3 ps Max.		200 MHz ≤ fo; Offset frequency: 12 kHz to 20 MHz
Frequency aging *2	f_aging	± 10 × 10^{-6} / year Max.		+25 °C, First year, Vcc=2.5 V,3.3 V

*1 As per below table 1.
*2 Except: ***A

►HCSL Output

Item	Symbol	EG-2121CA	EG-2102CA	Conditions / Remarks
		HCSL		
Output frequency range	fo	100 MHz to 350 MHz		Please contact us for inquiries regarding available frequencies.
Supply voltage	Vcc	2.5 V ±0.125 V	3.3 V ±0.3 V	
Storage temperature	T_stg	-40 °C to +125 °C		Store as bare product.
Operating temperature	T_use	P:0 °C to +70 °C ,R:-5 °C to +85 °C ,S:-20 °C to +70 °C		
Frequency tolerance *1	f_tol	G: ± 50 × 10^{-6} ,H: ±100 × 10^{-6}		
Current consumption	Icc	80 mA Max.	85 mA Max.	OE=Vcc,L_HCSL=50 Ω
Disable current	I_dis	20 mA Max.	35 mA Max	OE=GND
Symmetry	SYM	45 % to 55 %		at outputs crossing point
Output Voltage	VOH	0.75 V Typ.		DC characteristics
	VOL	-0.3 V Typ.		
Output load condition (HCSL)	L_HCSL	50 Ω		Terminated to GND
Input voltage	VIH	70 % Vcc Min.		OE terminal
	VIL	30 % Vcc Max.		
Rise time / Fall time	t_r / t_f	500 ps Max.		Between 0.175 V and 0.525 V of output
Start-up time	t_str	10 ms Max.		Time at minimum supply voltage to be 0 s
Phase Jitter	t_{PJ}	0.8 ps Max.		fo < 100 MHz; Offset frequency: 12 kHz to 20 MHz
		0.5 ps Max.		100 MHz ≤ fo < 200 MHz
		0.3 ps Max.		200 MHz ≤ fo
Frequency aging *2	f_aging	± 10 × 10^{-6} / year Max.		+25 °C, First year, Vcc=2.5 V,3.3 V

*1 As per below table 1.
*2 Except: ***A

Table 1 Frequency tolerance and aging

Output and Symmetry		P: Differential LV-PECL		D: Differential LV-PECL		L: LVDS		V: LVDS		H: HCSL	
Frequency range		All range		EG-2121CA: fo ≤ 175 MHz EG-2102CA: fo ≤ 350 MHz		All range		fo ≤ 175 MHz		All range	
Aging		A *3	N *4	A *3	N *4	A *3	N *4	A *3	N *4	A *3	N *4
Frequency tolerance and operating temperature	HP: ±100 × 10^{-6} (0°C to +70°C)	PHPA	PHPN	DHPA	DHPN	LHPA	LHPN	VHPA	VHPN	HHPA	HHPN
	HR: ±100 × 10^{-6} (-5°C to +85°C)	PHRA *5	PHRN *5	DHRA *5	DHRN *5	LHRA *5	LHRN *5	VHRA *5	VHRN *5	HHRA	HHRN
	GP: ±50 × 10^{-6} (0°C to +70°C)	PGPA *5	PGPN *5	DGPA *5	DGPN *5	LGPA *5	LGPN *5	VGPA *5	VGPN *5	HGPA	HGPN
	GR: ±50 × 10^{-6} (-5°C to +85°C)	—	PGRN *5	—	DGRN *5	—	LGRN *5	—	VGRN *5	—	HGRN
	HS: ±100 × 10^{-6} (-20°C to +70°C)	PHSA *5	PHSN *5	DHSA *5	DHSN *5	LHSA *5	LHSN *5	VHSA *5	VHSN *5	HHSA	HHSN
	GS: ±50 × 10^{-6} (-20°C to +70°C)	—	PGSN *5	—	DGSN *5	—	LGSN *5	—	VGSN *5	—	HGSN

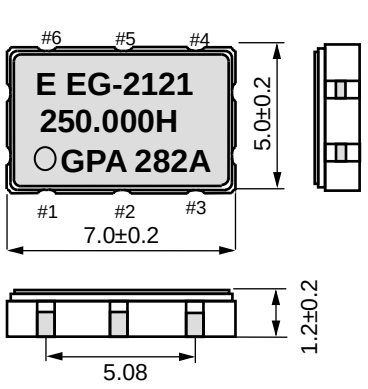
*3 This includes initial frequency tolerance, temperature variation, supply voltage variation, reflow drift, and aging(+25 °C,10 years).
*4 This includes initial frequency tolerance, temperature variation, supply voltage variation, and reflow drift(except aging).
*5 53.125 MHz ≤ fo < 100 MHz : Unavailable.

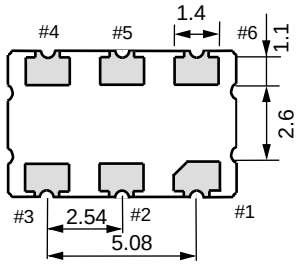
Table 2 Jitter

Item	Symbol	Specifications	Remarks
Jitter *	t_{DJ}	0.2 ps Typ.	Deterministic Jitter
	t_{RJ}	3 ps Typ.	Random Jitter
	t_{RMS}	3 ps Typ.	σ (RMS of total distribution)
	t_{p-p}	25 ps Typ.	Peak to Peak
	t_{acc}	4 ps Typ.	Accumulated Jitter(σ) n=2 to 50000 cycles

* Based on DTS-2075 Digital timing system made from WAVECREST with jitter analysis software VISI6. : Differential LV-PECL, LVDS output
* Based on SIA-3100C signal integrity analyzer made from WAVECREST. : HCSL output

External dimensions (Unit:mm)





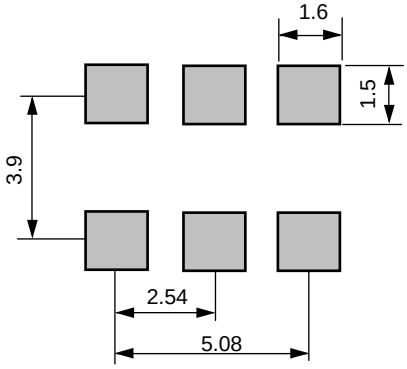
Pin map

Pin	Connection
1	OE
2	N.C.
3	GND
4	OUT
5	$\overline{OUT}$
6	VCC

#3 is connected to the cover.

OE pin = HIGH : Specified frequency output.
OE pin = LOW : Output is high impedance

Footprint (Recommended) (Unit:mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).