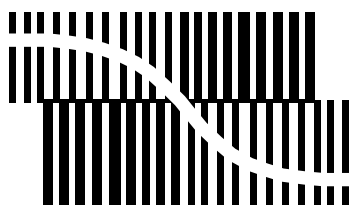# DATA SHEET

BITSTREAM CONVERSION

## UDA1330ATS

## Low-cost stereo filter DAC

Preliminary specification

Supersedes data of 1998 Mar 06

File under Integrated Circuits, IC01

1998 Mar 24

**Philips**
**Semiconductors**

PHILIPS

**PHILIPS**

# Low-cost stereo filter DAC                                UDA1330ATS

## FEATURES

### General

- Low power consumption
- 4.5 to 5.5 V power supply
- Selectable control via L3 microcontroller interface or via static pin control
- System clock frequencies of 256, 384 and 512$f_s$, selectable via the L3 interface or 256$f_s$ and 384$f_s$ clock mode selectable via the static pin control
- Supports sampling frequencies ($f_s$) from 16 to 48 kHz
- Integrated digital filter plus non inverting Digital-to-Analog Converter (DAC)
- No analog post filtering required for DAC
- Slave mode only applications
- Easy application
- Small package size (SSOP16).

### Multiple format input interface

- I$^2$S-bus, MSB-justified and LSB-justified 16, 18 and 20 bits format compatible (in L3 mode)
- I$^2$S-bus and LSB-justified 16, 18 and 20 bits format compatible
- 1$f_s$ input format data rate.

### DAC digital sound processing

- Digital logarithmic volume control via L3 control
- Digital de-emphasis for 32, 44.1 and 48 kHz sampling frequencies via L3 control or 44.1 kHz sampling frequency via static pin control
- Soft mute via static pin control or via L3 interface.

### Advanced audio configuration

- Stereo line output (under L3 volume control)
- High linearity, wide dynamic range, low distortion.
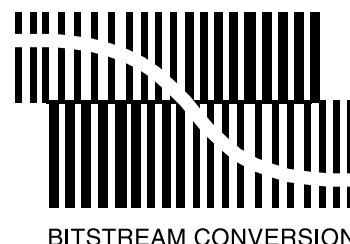
BITSTREAM CONVERSION

## APPLICATIONS

- 5 V PC audio applications
- Car radio applications.

## GENERAL DESCRIPTION

The UDA1330ATS is a single-chip stereo DAC employing bitstream conversion techniques. The UDA1330ATS can be used in two modes, either the L3 mode or the static pin mode.

The UDA1330ATS supports the I$^2$S-bus data format with word lengths of up to 20 bits, the MSB-justified data format with word lengths of up to 20 bits and the LSB-justified serial data format with word lengths of 16, 18 and 20 bits.

In the L3 mode, all digital sound processing features must be controlled via the L3 interface, including the selection of the system clock setting.

In the two static modes, the UDA1330ATS can be operated in the 256$f_s$ and 384$f_s$ system clock mode. The mute, de-emphasis for 44.1 kHz and 4 digital input formats (I$^2$S-bus and 16, 18, and 20 bits LSB formats) can be selected via static pins. The L3 interface cannot be used in this application mode. Volume control is also not available in this mode.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
| --- | --- | --- | --- |
| | NAME | DESCRIPTION | VERSION |
| UDA1330ATS/N1 | SSOP16 | plastic shrink small outline package; 16 leads; body width 4.4 mm | SOT369-1 |

# Low-cost stereo filter DAC

# UDA1330ATS

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DDA}$ | analog supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_{DDD}$ | digital supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $I_{DDA}$ | DAC supply current | | – | 9.5 | – | mA |
| $I_{DDD}$ | digital supply current | | – | 5.5 | – | mA |
| $T_{amb}$ | operating ambient temperature | | –20 | – | +85 | °C |
| **DAC** | | | | | | |
| $V_{o(rms)}$ | output voltage (RMS value) | note 1 | – | 1.45 | – | V |
| (THD + N)/S | total harmonic distortion plus noise-to-signal ratio | at 0 dB | – | –88 | –83 | dB |
| | | at –60 dB; A-weighted | – | –40 | –35 | dB |
| S/N | signal-to-noise ratio | code = 0; A-weighted | – | 100 | –95 | dB |
| $\alpha_{cs}$ | channel separation | | – | 100 | – | dB |
| $T_{amb}$ | operating ambient temperature | | –20 | – | +85 | °C |

**Note**

1. The output voltage scales linearly with the power supply voltage.

## BLOCK DIAGRAM



Fig.1 Block diagram.
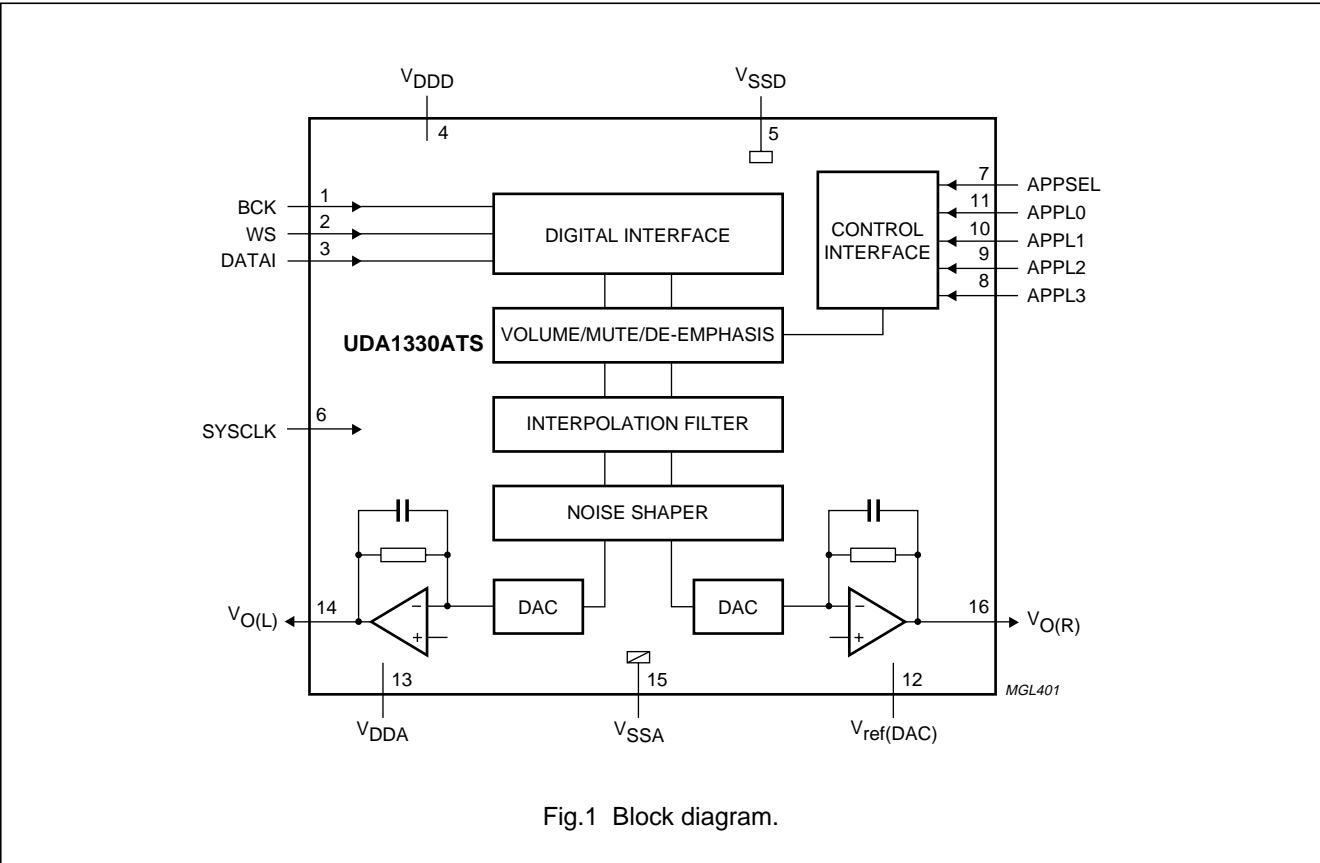
## Low-cost stereo filter DAC

## UDA1330ATS

### PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| BCK | 1 | bit clock input |
| WS | 2 | word select input |
| DATAI | 3 | data input |
| $V_{DDD}$ | 4 | digital power supply |
| $V_{SSD}$ | 5 | digital ground |
| SYSCLK | 6 | system clock input 256, 384 and 512$f_s$ |
| APPSEL | 7 | application mode select input |
| APPL3 | 8 | application input pin 3 |
| APPL2 | 9 | application input pin 2 |
| APPL1 | 10 | application input pin 1 |
| APPL0 | 11 | application input pin 0 |
| $V_{ref(DAC)}$ | 12 | DAC reference voltage |
| $V_{DDA}$ | 13 | analog supply voltage |
| $V_{O(L)}$ | 14 | left output voltage |
| $V_{SSA}$ | 15 | analog ground |
| $V_{O(R)}$ | 16 | right output voltage |
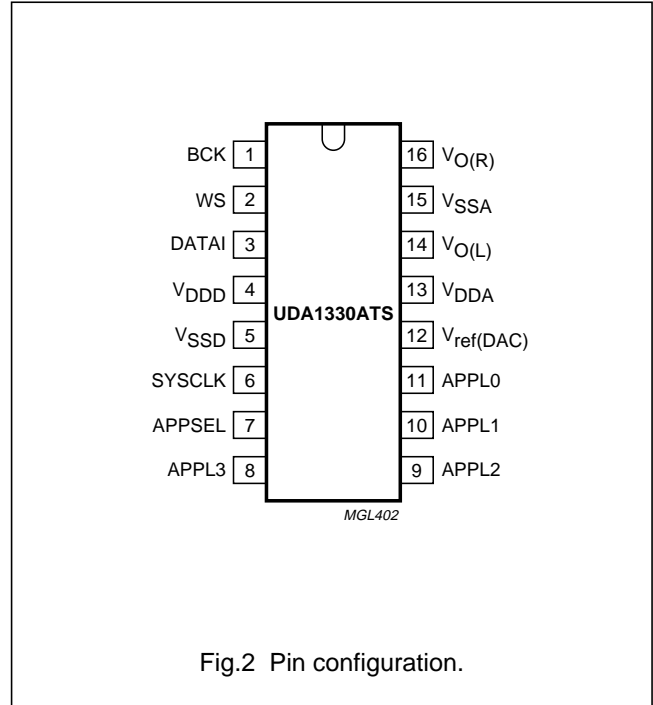


Fig.2  Pin configuration.

### FUNCTIONAL DESCRIPTION

#### System clock

The UDA1330ATS operates in slave mode only. In all applications, therefore, the system devices must provide the system clock. The system frequency is selectable and depends on the mode of operation.

The options are 256, 384 and 512$f_s$ for the L3 mode and 256$f_s$ plus 384$f_s$ for the static mode. The system clock must be locked in frequency to the digital interface input signals.

The UDA1330ATS supports sampling frequencies from 16 to 48 kHz.

#### Application modes

Operation can be set with the tri-value APPSEL pin, to L3 mode (APPSEL = $V_{SSD}$) or to either of two static modes (APPSEL = 0.5$V_{DDD}$ or APPSEL = $V_{DDD}$), see Table 1 for APPL0 to APPL3 pin functions (active = HIGH).

Table 1    Selection modes via APPSEL

| PIN | APPSEL | | |
|---|---|---|---|
| | $V_{SSD}$ | 0.5$V_{DDD}$ (384$f_s$) | $V_{DDD}$ (256$f_s$) |
| APPL0 | TEST | MUTE | MUTE |
| APPL1 | L3CLOCK | DEEM | DEEM |
| APPL2 | L3MODE | SF0 | SF0 |
| APPL3 | L3DATA | SF1 | SF1 |

For example, in static pin control mode, the output signal can be soft muted by setting APPL0 HIGH. De-emphasis can be switched on for 44.1 kHz by setting APPL1 HIGH. APPL1 LOW will disable de-emphasis.

It should be noted that when the L3 interface is used, an L3 initialisation must be done when the IC is powered up.

## Low-cost stereo filter DAC

UDA1330ATS

### Multiple format input interface

L3 MODE

- I²S-bus with data word length of up to 20 bits
- MSB-justified format with data word length up to 20 bits
- LSB-justified format with data word length of 16, 18 or 20 bits.

STATIC PIN MODE

The UDA1330ATS supports the following data input name formats in the static pin mode (via SF0 and SF1):

- I²S-bus with data word length of up to 20 bits
- LSB-justified format with data word length of 16, 18 or 20 bits.

See Table 2, for the static pin codes of the 4 formats, selectable via SF0 and SF1.

The UDA1330ATS also accepts double speed data for double speed data monitoring purposes.

**Table 2**  Input format selection using SF0 and SF1

| FORMAT | SF0 | SF1 |
|---|---|---|
| I²S-bus | 0 | 0 |
| LSB-justified 16 bits | 0 | 1 |
| LSB-justified 18 bits | 1 | 0 |
| LSB-justified 20 bits | 1 | 1 |

The formats are illustrated in Fig.3. Left and right data-channel words are time multiplexed. The WS signal must have a 50% duty factor for all LSB-justified modes.

For the digital data interface the bit clock frequency should be less than or equal to 64 times the word frequency; $f_{BCK} = \leq 64f_{WS}$.

### Pin compatibility

In L3 interface mode the UDA1330ATS can be used on boards that are designed for the UDA1320ATS.

**IMPORTANT**: It should be noted that the UDA1330ATS is designed for 5 V operation while the UDA1320ATS is designed for 3 V operation.

### Interpolation filter (DAC)

The digital filter interpolates from 1 to 128$f_s$ by cascading a recursive filter and an FIR filter, see Table 3.

**Table 3**  Interpolation filter characteristics

| ITEM | CONDITION | VALUE (dB) |
|---|---|---|
| Pass-band ripple | 0 to 0.45$f_s$ | ±0.1 |
| Stop band | >0.55$f_s$ | −50 |
| Dynamic range | 0 to 0.45$f_s$ | 108 |

### Noise shaper

The 3rd-order noise shaper operates at 128$f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter-Stream DAC (FSDAC).

### Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to be analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage scales linearly with the power supply voltage.

INPUT FORMAT I$^2$S-BUS

MSB-JUSTIFIED FORMAT

LSB-JUSTIFIED FORMAT 16 BITS

LSB-JUSTIFIED FORMAT 18 BITS

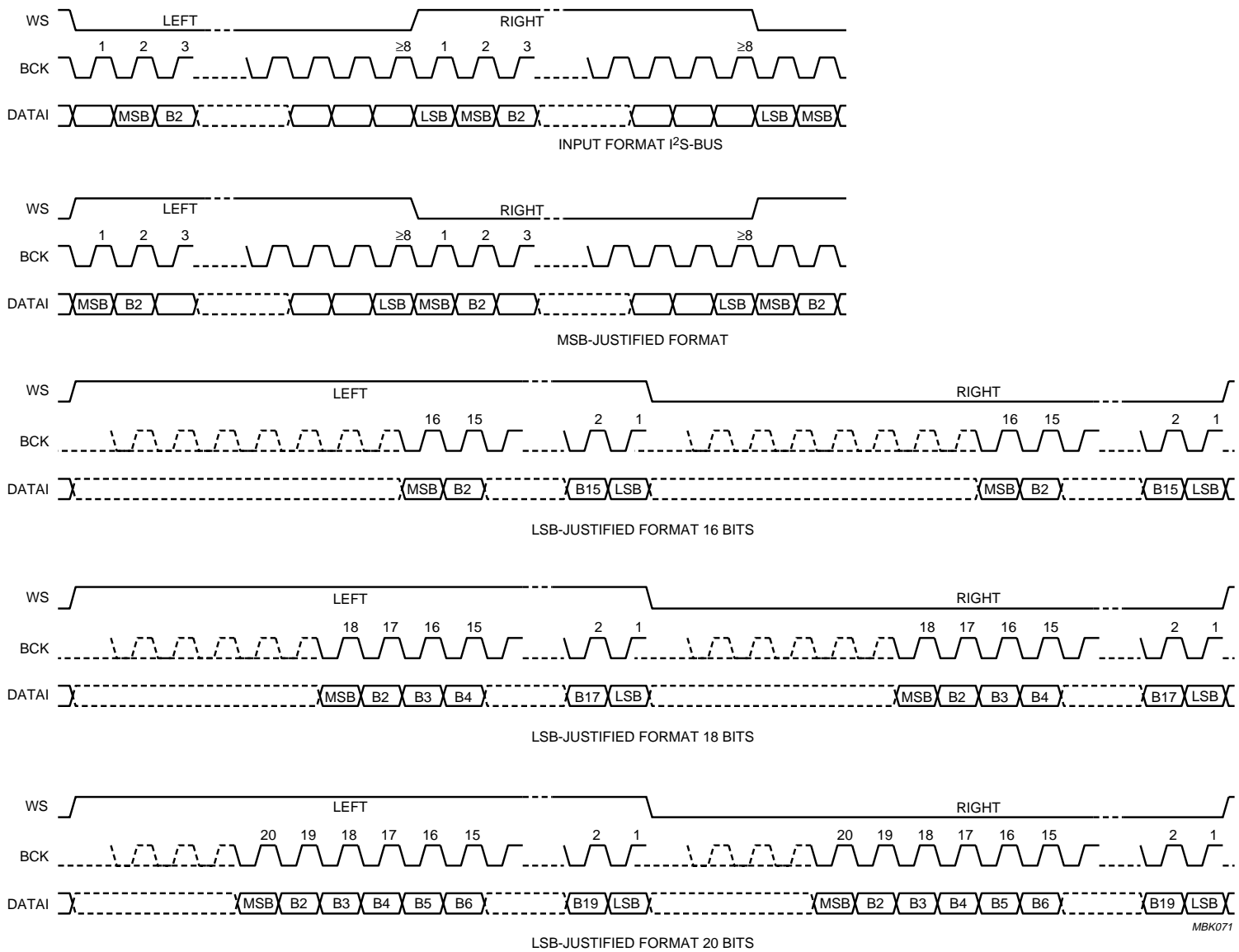LSB-JUSTIFIED FORMAT 20 BITS

MBK071

Fig.3  Serial interface; input format I$^2$S-bus.

Low-cost stereo filter DAC

UDA1330ATS

## L3 INTERFACE DESCRIPTION

### The L3 interface

The following system and digital sound processing features can be controlled in the microcontroller mode of the UDA1330ATS.

- System clock frequency
- Data input format
- De-emphasis for 32, 44.1 and 48 kHz
- Volume
- Soft mute.

The exchange of data and control information between the microcontroller and the UDA1330ATS is accomplished through a serial interface comprising the following pins:

- L3DATA
- L3MODE
- L3CLOCK.

Information transfer through the microcontroller bus is organized in accordance with the L3 format, in which two different modes of operation can be distinguished; address mode and data transfer mode (see Figs 4 and 6).

The address mode is required to select a device communicating via the L3 bus and to define the destination registers for the data transfer mode. Data transfer can only be in one direction, consisting of input to the UDA1330ATS to program sound processing and other functional features.

Data bits 7 to 2 represent a 6-bit device address, bit 7 being the MSB. The address of the UDA1330ATS is 000101 (bit 7 to bit 2). If the UDA1330ATS receives a different address, it will deselect its microcontroller interface logic.

### Data transfer mode

The selected address remains active during subsequent data transfers until the UDA1330ATS receives a new address command. The fundamental timing of data transfers is essentially the same as in the address mode, see Fig.4. The maximum input clock and data rate is $64f_s$. All transfers are by 8-bit bytes. Data will be stored in the UDA1330ATS after reception of a complete byte. See Fig.5 for a multi-byte transfer.

**Table 4**  Selection of data transfer

| BIT 1 | BIT 0 | TRANSFER |
|-------|-------|----------|
| 0 | 0 | DATA (volume, de-emphasis, mute) |
| 0 | 1 | not used |
| 1 | 0 | STATUS (system clock frequency, data input format) |
| 1 | 1 | not used |

The sound feature values are stored in independent registers. The first selection of the registers is achieved by the choice of data type that is transferred ('STATUS' or 'DATA' transfer). This is performed in the address mode using bit 1 and bit 0, see Table 4. The settings that can be controlled with 'STATUS' transfer are given in Table 5, and the settings that can be controlled using 'DATA' transfer are given in Table 6.

The second selection is performed by the 2 MSBs of the data byte (bit 7 and bit 6). The other bits in the data byte (bit 5 to bit 0) is the value that is placed in the selected registers.
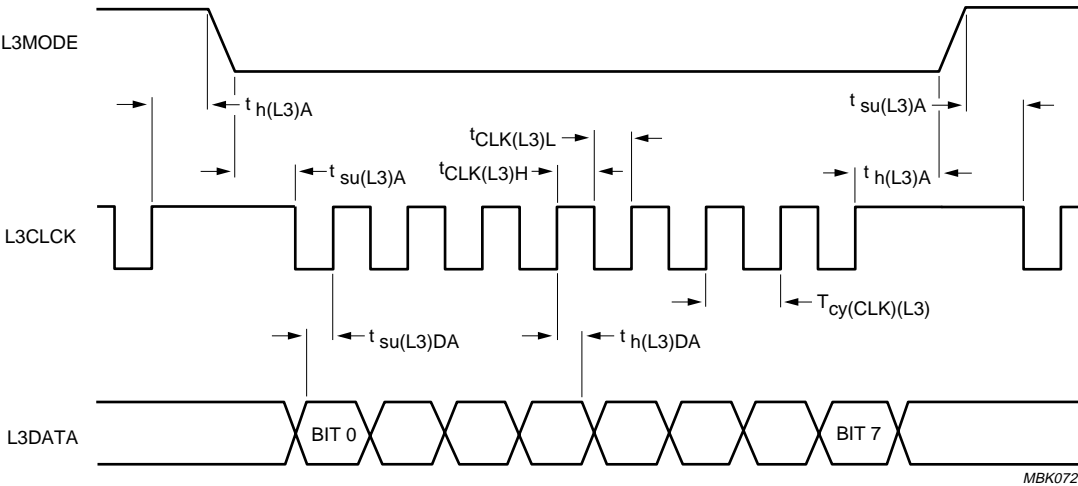
## Low-cost stereo filter DAC

## UDA1330ATS
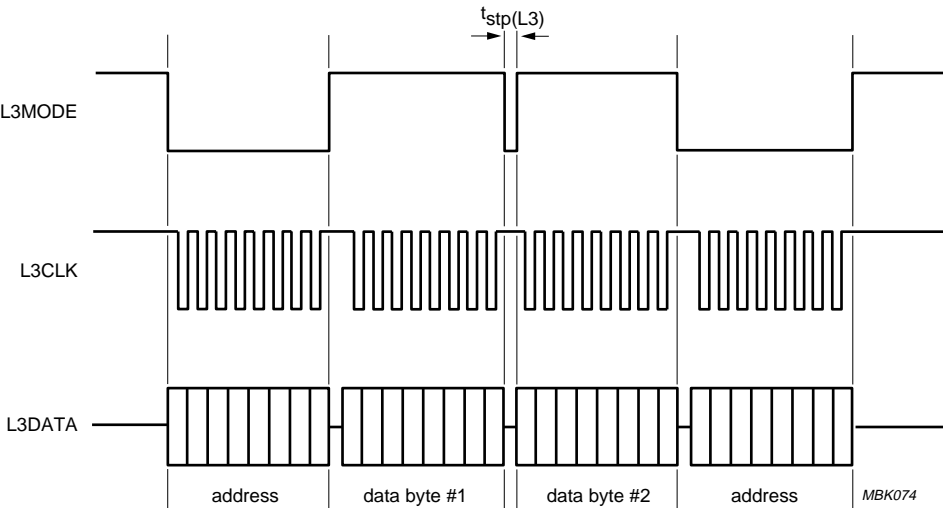


Fig.4  Timing address mode.



Fig.5  Multi-byte transfer.

## Low-cost stereo filter DAC
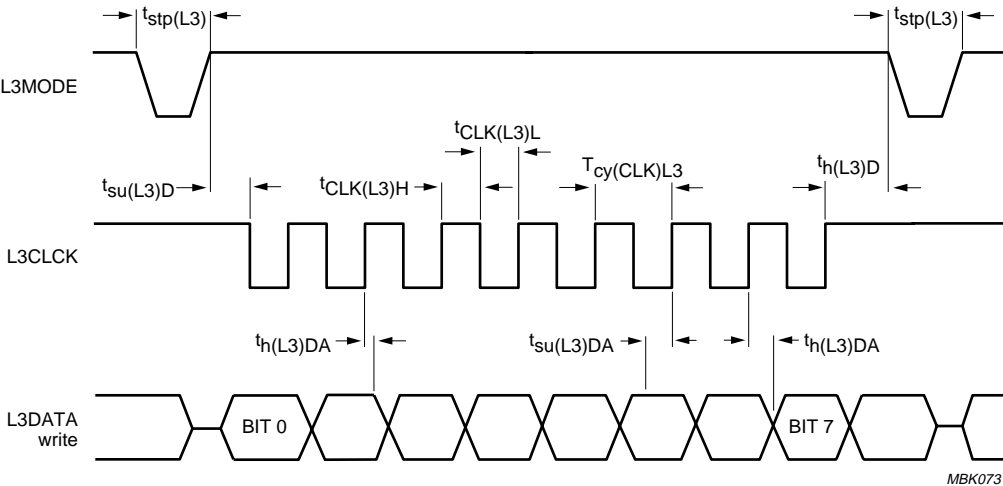
## UDA1330ATS



Fig.6 Timing for data transfer mode.

**Table 5** Data transfer of type 'status'

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | REGISTER SELECTED |
|-------|-------|-------|-------|-------|-------|-------|-------|-------------------|
| 0 | 0 | SC1 | SC0 | IF2 | IF1 | IF0 | 0 | System Clock frequency (1 : 0); data Input Format (2 : 0) |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | reserved |

**Table 6** Data transfer of type 'data'

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | REGISTER SELECTED |
|-------|-------|-------|-------|-------|-------|-------|-------|-------------------|
| 0 | 0 | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 | Volume Control (5 : 0) |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | reserved |
| 1 | 0 | 0 | DE1 | DE0 | MT | 0 | 0 | DE-emphasis (1 : 0); MuTe |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | default setting |

Low-cost stereo filter DAC

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**Programming the features**

When the data transfer of type 'STATUS' is selected, the features SYSTEM CLOCK FREQUENCY and DATA INPUT FORMAT can be controlled.

**System clock frequency:** a 2-bit value to select the used external clock frequency.

**Table 7** System clock settings

| SC1 | SC0 | FUNCTION |
|---|---|---|
| 0 | 0 | $512f_s$ |
| 0 | 1 | $384f_s$ |
| 1 | 0 | $256f_s$ |
| 1 | 1 | not used |

**Data input format:** a 3-bit value to select the data format.

**Table 8** Data input format settings

| IF2 | IF1 | IF0 | FUNCTION |
|---|---|---|---|
| 0 | 0 | 0 | $I^2S$-bus |
| 0 | 0 | 1 | LSB-justified, 16 bits |
| 0 | 1 | 0 | LSB-justified, 18 bits |
| 0 | 1 | 1 | LSB-justified, 20 bits |
| 1 | 0 | 0 | MSB-justified |
| 1 | 0 | 1 | not used |
| 1 | 1 | 0 | not used |
| 1 | 1 | 1 | not used |

When the data transfer of type 'DATA' is selected, the features VOLUME, DE-EMPHASIS and MUTE can be controlled.

**Volume control**: a 6-bit value to program the volume attenuation (VC5 to VC0), 0 to $-\infty$ dB in steps of 1 dB.

**Table 9** Volume settings

| VC5 | VC4 | VC3 | VC2 | VC1 | VC0 | VOLUME (dB) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | −1 |
| 0 | 0 | 0 | 0 | 1 | 1 | −2 |
| : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 0 | 1 | −60 |
| 1 | 1 | 1 | 1 | 1 | 1 | $-\infty$ |

**De-emphasis:** a 2-bit value to enable the digital de-emphasis filter.

**Table 10** De-emphasis settings

| DE1 | DE0 | FUNCTION |
|---|---|---|
| 0 | 0 | no de-emphasis |
| 0 | 1 | de-emphasis, 32 kHz |
| 1 | 0 | de-emphasis, 44.1 kHz |
| 1 | 1 | de-emphasis, 48 kHz |

**Mute:** a 1-bit value to enable the digital mute.

**Table 11** Mute setting

| MT | FUNCTION |
|---|---|
| 0 | no muting |
| 1 | muting |

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DDD}$ | digital supply voltage | note 1 | – | 6.0 | V |
| $V_{DDA}$ | analog supply voltage | note 1 | – | 6.0 | V |
| $T_{xtal(max)}$ | maximum crystal temperature | | – | 150 | °C |
| $T_{stg}$ | storage temperature | | –65 | +125 | °C |
| $T_{amb}$ | operating ambient temperature | | –20 | +85 | °C |
| $V_{es}$ | electrostatic handling | note 2 | –3000 | +3000 | V |
| | | note 3 | –250 | +250 | V |

**Notes**

1. All supply connections must be made to the same power supply.

2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor, except pin 3 which can withstand ESD pulses of –2500 V to +2500 V.

3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

## QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 190 | K/W |

Low-cost stereo filter DAC

UDA1330ATS

## DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = 5.0$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages referenced to ground (pins 5 and 15); unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DDA}$ | DAC analog supply voltage | note 1 | 4.0 | 5.0 | 5.5 | V |
| $V_{DDD}$ | digital supply voltage | note 1 | 4.0 | 5.0 | 5.5 | V |
| $I_{DDA}$ | analog supply current | | – | 9.5 | – | mA |
| $I_{DDD}$ | digital supply current | | – | 5.5 | – | mA |
| **Digital input pins** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | $0.8V_{DDD}$ | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | – | – | $0.2V_{DDD}$ | V |
| $|I_{LI}|$ | input leakage current | | – | – | 1 | μA |
| $C_I$ | input capacitance | | – | – | 10 | pF |
| **DAC** | | | | | | |
| $V_{ref(DAC)}$ | reference voltage | with respect to $V_{SSA}$ | $0.45V_{DDA}$ | $0.5V_{DDA}$ | $0.55V_{DDA}$ | V |
| $I_{O(max)}$ | maximum output current | (THD + N)/S < 0.1%; $R_L = 5$ kΩ | – | 0.36 | – | mA |
| $R_O$ | output resistance | | – | 0.15 | 2.0 | Ω |
| $R_L$ | load resistance | | 3 | – | – | kΩ |
| $C_L$ | load capacitance | note 2 | – | – | 50 | pF |

### Notes

1. All supply connections must be made to the same external power supply unit.

2. When the DAC drives a capacitive load above 50 pF, a series resistance of 100 Ω must be used to prevent oscillations in the output operational amplifier.

## AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = 5.0$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages referenced to ground (pins 5 and 15); unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **DAC** | | | | | | |
| $V_{o(rms)}$ | output voltage (RMS value) | | – | 1.45 | – | V |
| $\Delta V_o$ | unbalance between channels | | – | 0.1 | – | dB |
| (THD + N)/S | total harmonic distortion plus noise-to-signal ratio | at 0 dB | – | −88 | −83 | dB |
| | | at −60 dB; A-weighted | – | −40 | −35 | dB |
| S/N | signal-to-noise ratio | code = 0; A-weighted | – | 100 | −95 | dB |
| $\alpha_{cs}$ | channel separation | | – | 100 | – | dB |
| PSRR | power supply ripple rejection ratio | $f_{ripple} = 1$ kHz; $V_{ripple} = 100$ mV (p-p) | – | 50 | – | dB |

Low-cost stereo filter DAC

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## AC CHARACTERISTICS (DIGITAL)

$V_{DDD}$ = $V_{DDA}$ = 4.5 to 5.5 V; $T_{amb}$ = −20 to +85 °C; $R_L$ = 5 kΩ; all voltages referenced to ground (pins 5 and 15); unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $T_{sys}$ | system clock cycle | $f_{sys}$ = 256$f_s$ | 78 | 88 | 244 | ns |
| | | $f_{sys}$ = 384$f_s$ | 52 | 59 | 162 | ns |
| | | $f_{sys}$ = 512$f_s$ | 39 | 44 | 122 | ns |
| $t_{CLK(sys)L}$ | LOW-level system clock pulse width | $f_{sys}$ < 19.2 MHz | 0.30$T_{sys}$ | – | 0.70$T_{sys}$ | ns |
| | | $f_{sys}$ ≥ 19.2 MHz | 0.40$T_{sys}$ | – | 0.60$T_{sys}$ | ns |
| $t_{CLK(sys)H}$ | HIGH-level system clock pulse width | $f_{sys}$ < 19.2 MHz | 0.30$T_{sys}$ | – | 0.70$T_{sys}$ | ns |
| | | $f_{sys}$ ≥ 19.2 MHz | 0.40$T_{sys}$ | – | 0.60$T_{sys}$ | ns |
| **Serial input data timing** (see Fig.7) | | | | | | |
| $T_{cy(CLK)(bit)}$ | bit clock period | | 300 | – | – | ns |
| $t_{CLKH(bit)}$ | bit clock HIGH time | | 100 | – | – | ns |
| $t_{CLKL(bit)}$ | bit clock LOW time | | 100 | – | – | ns |
| $t_r$ | rise time | | – | – | 20 | ns |
| $t_f$ | fall time | | – | – | 20 | ns |
| $t_{su(i)(D)}$ | data input set-up time | | 20 | – | – | ns |
| $t_{h(i)(D)}$ | data input hold time | | 0 | – | – | ns |
| $t_{su(WS)}$ | word selection set-up time | | 20 | – | – | ns |
| $t_{h(WS)}$ | word selection hold time | | 10 | – | – | ns |
| **Microcontroller interface timing** (see Figs 4 and 6) | | | | | | |
| $T_{cy(CLK)(L3)}$ | L3CLK | | 500 | – | – | ns |
| $t_{CLK(L3)H}$ | L3CLK HIGH period | | 250 | – | – | ns |
| $t_{CLK(L3)L}$ | L3CLK LOW period | | 250 | – | – | ns |
| $t_{su(L3)A}$ | L3MODE set-up time | addressing mode | 190 | – | – | ns |
| $t_{h(L3)A}$ | L3MODE hold time | addressing mode | 190 | – | – | ns |
| $t_{su(L3)D}$ | L3MODE set-up time | data transfer mode | 190 | – | – | ns |
| $t_{h(L3)D}$ | L3MODE hold time | data transfer mode | 190 | – | – | ns |
| $t_{su(L3)DA}$ | L3DATA set-up time | data transfer and addressing mode | 190 | – | – | ns |
| $t_{h(L3)DA}$ | L3DATA hold time | data transfer and addressing mode | 30 | – | – | ns |
| $t_{stp(L3)}$ | L3MODE halt time | | 190 | – | – | ns |
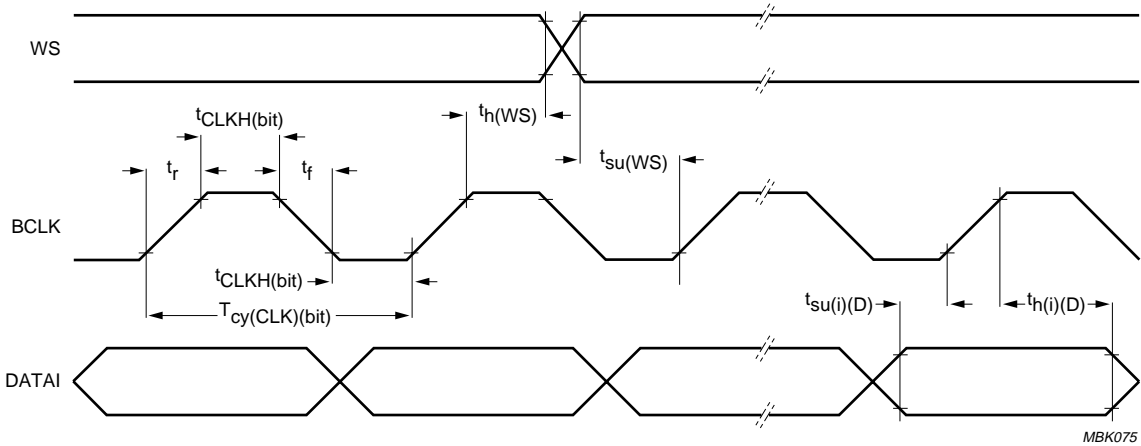
Fig.7 Serial interface timing.

## Low-cost stereo filter DAC

## UDA1330ATS

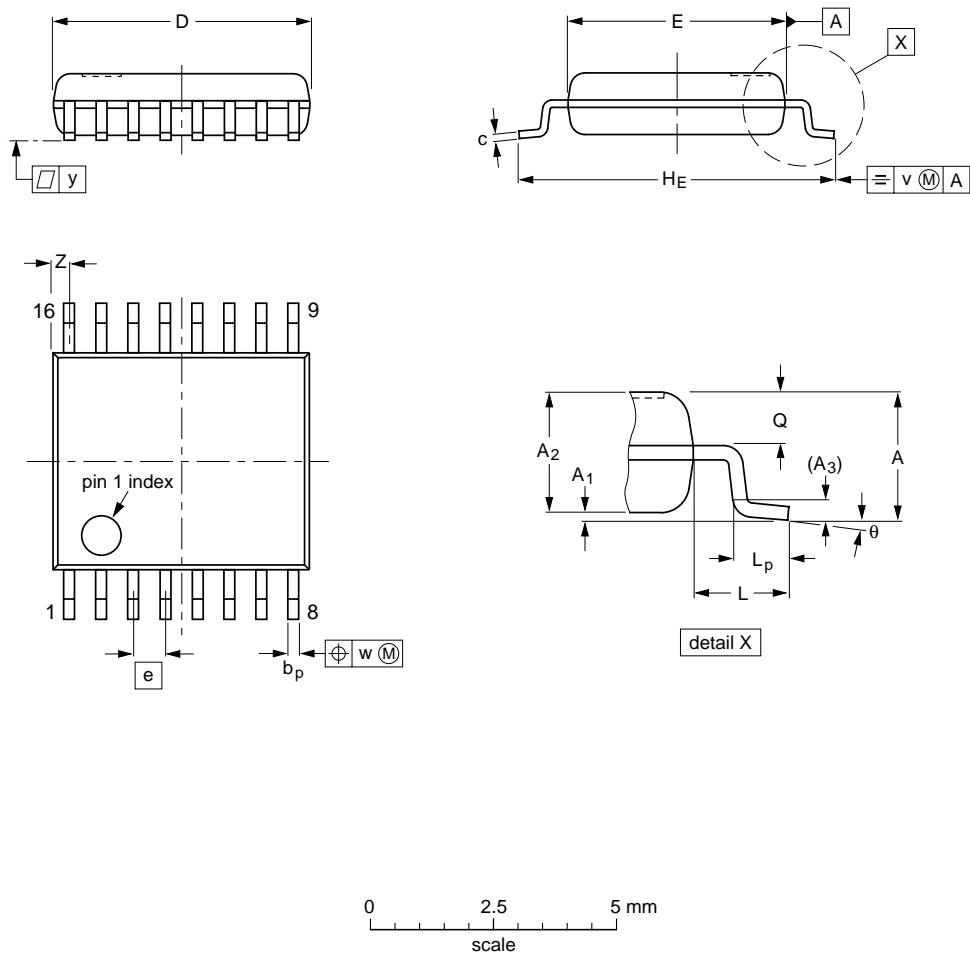### APPLICATION INFORMATION



Fig.8  Application diagram.
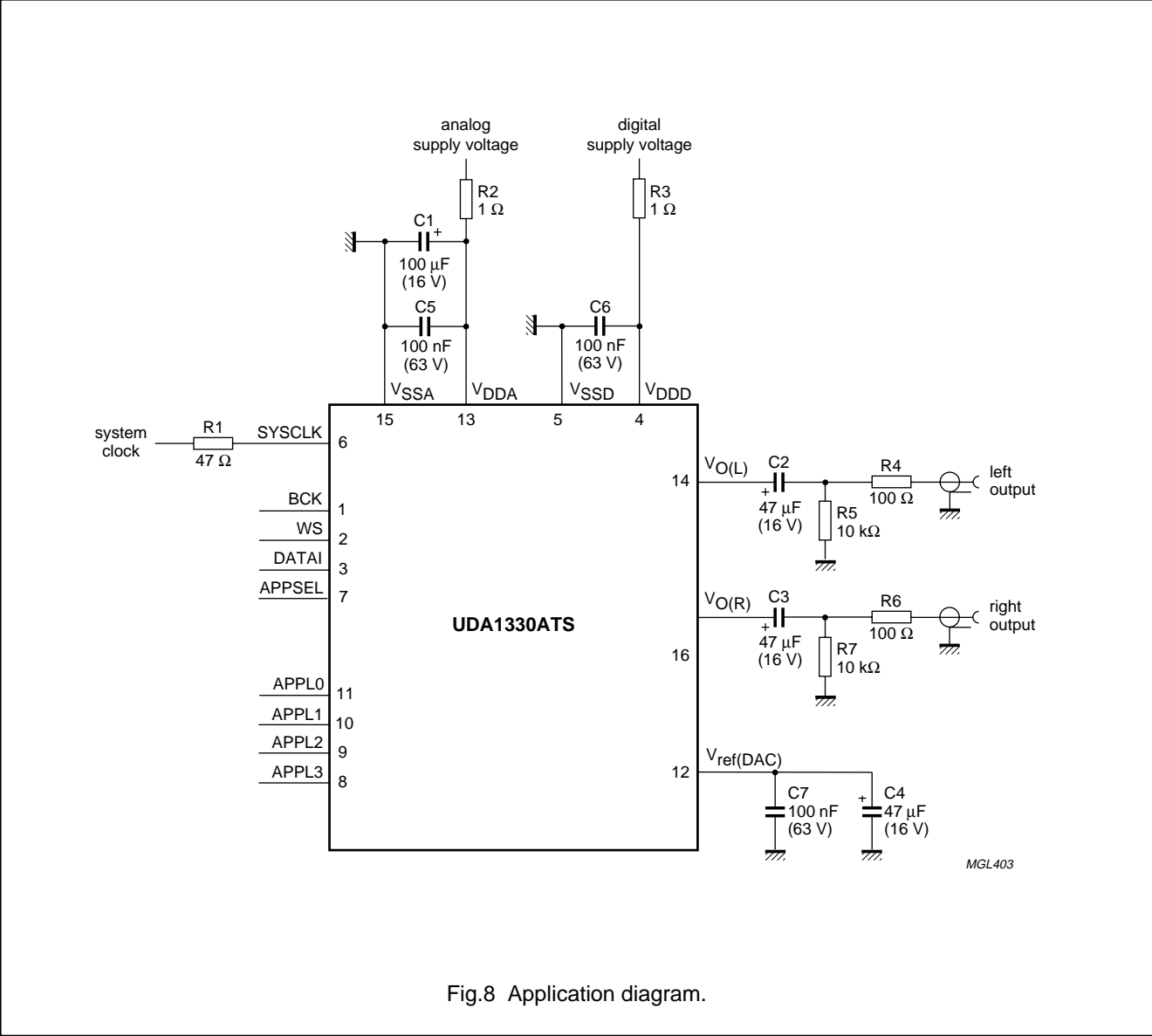
# Low-cost stereo filter DAC

# UDA1330ATS

## PACKAGE OUTLINE

**SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm**

**SOT369-1**



```
0        2.5        5 mm
|____|____|____|____|
          scale
```

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A1 | A2 | A3 | bp | c | D(1) | E(1) | e | HE | L | Lp | Q | v | w | y | Z(1) | θ |
|------|--------|-----|-----|------|------|------|------|------|------|------|------|------|------|-----|------|-----|------|------|
| mm | 1.5 | 0.15 0.00 | 1.4 1.2 | 0.25 | 0.32 0.20 | 0.25 0.13 | 5.30 5.10 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1.0 | 0.75 0.45 | 0.65 0.45 | 0.2 | 0.13 | 0.1 | 0.48 0.18 | 10° 0° |

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|---|---------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT369-1 | | | | | | ~~94-04-20~~ 95-02-04 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

### Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

**Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1)**.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**DEFINITIONS**

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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