Signetics

Logic Products

74LS168A, 74LS169A, S168A, S169A
4-Bit Bidirectional Counters

4-Bit Up/Down Synchronous Counter
Product Specification

FEATURES
- **Synchronous counting and loading**
- **Up/down counting**
- **Modulo 16 binary counter — '169A**
- **BCD decade counter — '168A**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**

DESCRIPTION
The '168A is a synchronous, presettable BCD decade up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS168A	32MHz	20mA
74S168A	70MHz	100mA
74LS169A	32MHz	20mA
74S169A	70MHz	100mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS168AN, N74S168AN N74LS169AN, N74S169AN
Plastic SO	N74LS169AD, N74LS169AD, N74S169AD

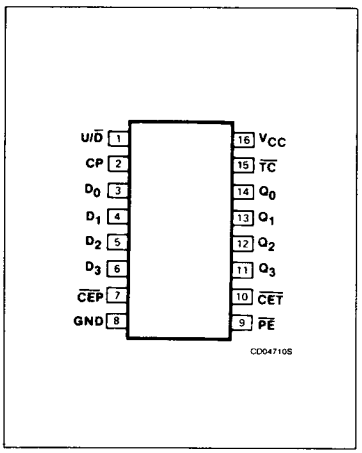
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

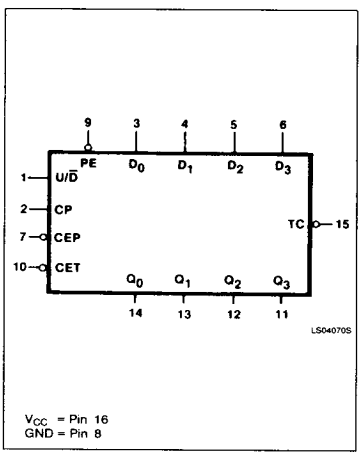
PINS	DESCRIPTION	74S	74LS
$\overline{PE}$	Input	1Sul	2LSul
$\overline{CET}$	Input	2Sul	1LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE:
Where a 74S unit load (Sul) is understood to be 50μA I_{IH} and −2.0mA I_{IL} and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

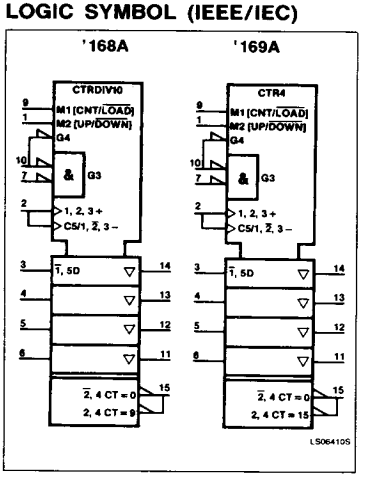
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



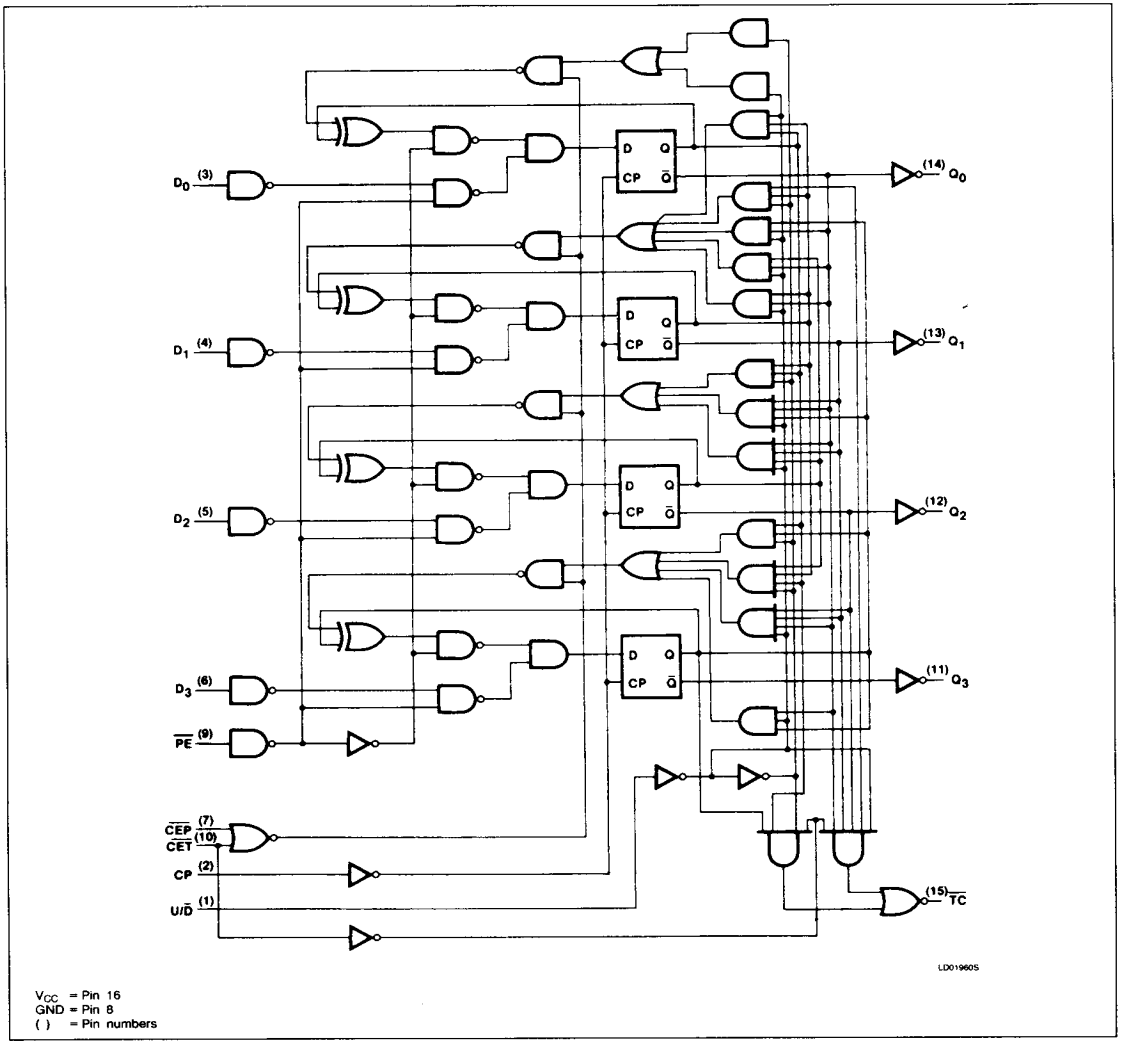
The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next LOW-to-HIGH transition of the clock.

The direction of counting is controlled by the Up/Down (U/$\overline{D}$) input; a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET} \cdot \overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure A for the fast synchronous multistage counting connections.

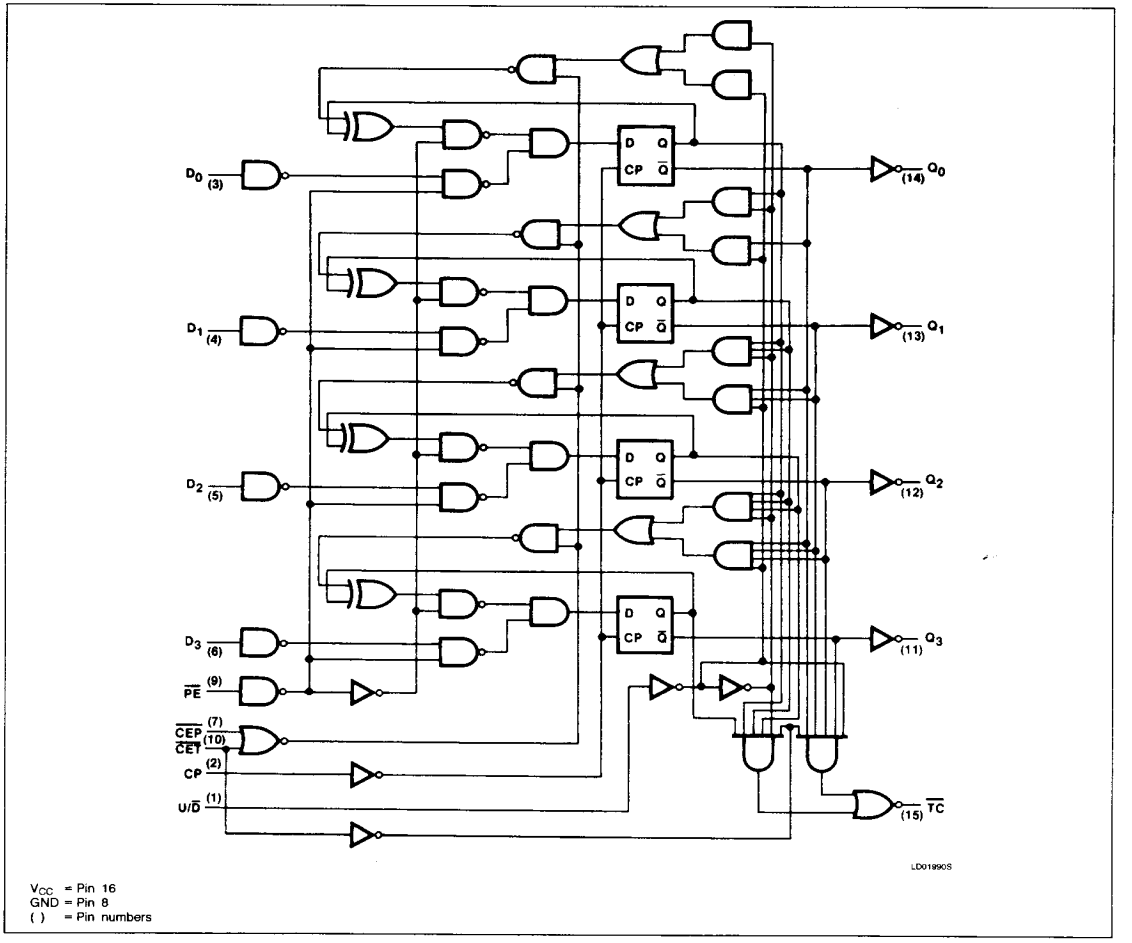
The '169A is identical except that it is a Modulo 16 counter.

LOGIC DIAGRAM, '168A



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

LOGIC DIAGRAM, '169A



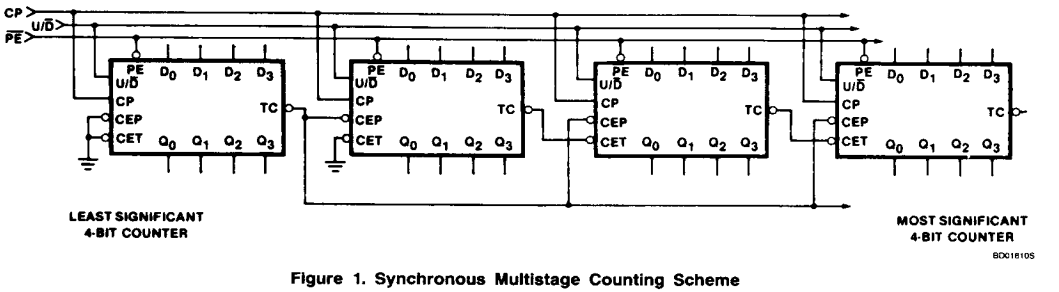


Figure 1. Synchronous Multistage Counting Scheme

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel Load	↑	X	X	X	l	i	L	(1)
	↑	X	X	X	i	h	H	(1)
Count Up	↑	h	l	l	h	X	Count Up	(1)
Count Down	↑	l	l	l	h	X	Count Down	(1)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

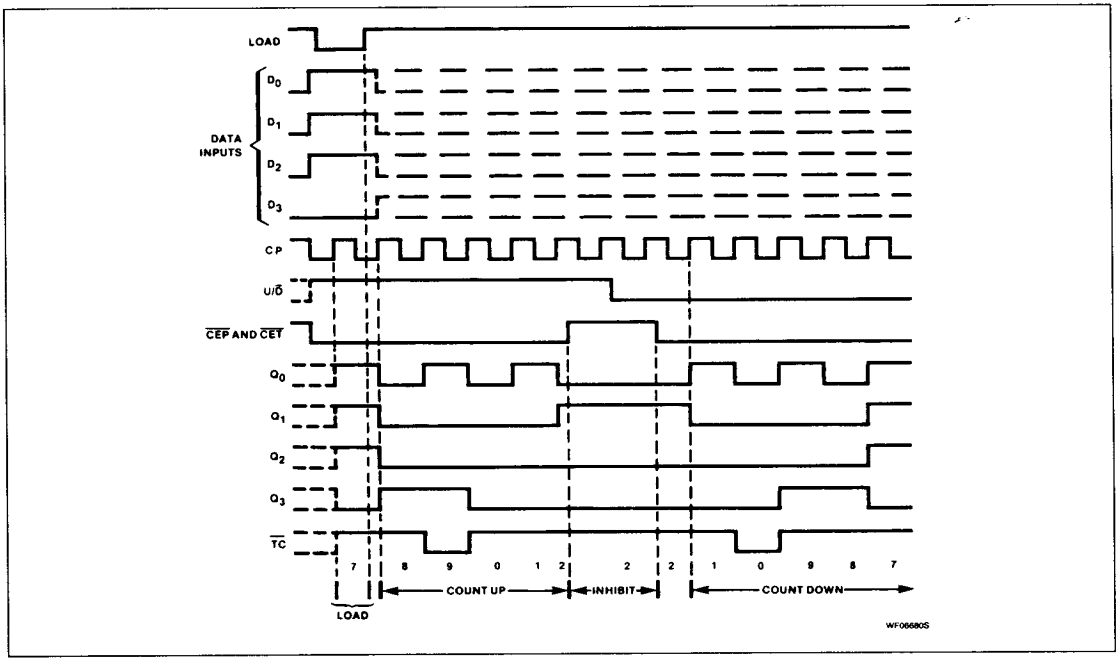
H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

NOTE:
1. The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169A. The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168A.

WAVEFORM (Typical Load, Count, and Inhibit Sequences)

Illustrated below is the following sequence for the '168A. The operation of the '169A is similar.

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



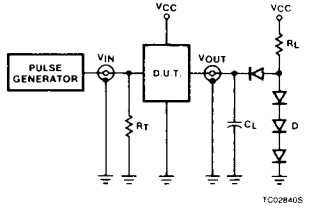
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

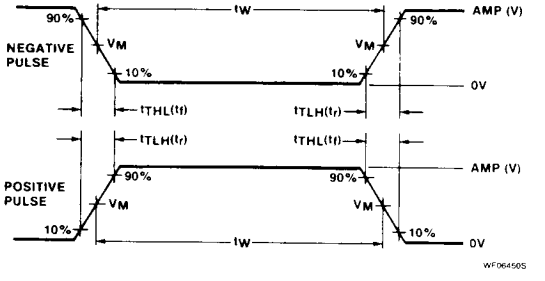
PARAMETER		74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	HIGH-level output current			−400			−1000	μA
I_{OL}	LOW-level output current			8			20	mA
T_A	Operating free-air temperature	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS





Test Circuit For 74 Totem-Pole Outputs

V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74LS168A, 169A			74S168A, 169A			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX			2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX			0.35	0.5			0.5	V
			I_{OL} = 4mA (74LS)			0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V	$\overline{PE}$ input			40				μA
				Other inputs			0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	$\overline{PE}$ input			0.2			100	mA
				$\overline{CET}$ input			20			100	μA
				Other inputs			20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	$\overline{PE}$ input			−0.8				mA
				Other inputs			−0.4				mA
			V_I = 0.5V	$\overline{CET}$ input						−4.0	mA
				Other inputs						−2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−20		−100	−40		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				20	34		55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after applying a momentary 4.5V, then ground to the Clock input with all other inputs grounded and outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74LS		74S				UNIT
			C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω U/$\overline{D}$ = HIGH		C_L = 15pF, R_L = 280Ω U/$\overline{D}$ = LOW		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		40		40		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Q output	Waveform 1		20 23		12 15		12 15	ns
t_{PLH} t_{PHL}	Propagation delay Clock to $\overline{TC}$	Waveform 1		35 35		17 15		15 25	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2		14 14		11 15		11 15	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ control to $\overline{TC}$[(b)]	Waveform 3		25 29		15 15		10 20	ns

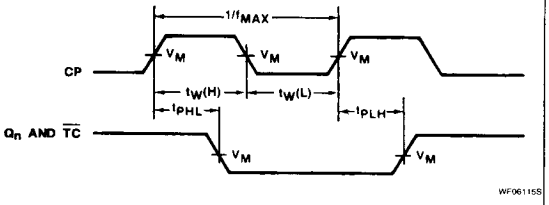
NOTE:
b. Propagation delay time from up/down to terminal count must be measured with the counter at either a minimum or a maximum count. As the logic level of the Up/Down input is changed, the Terminal Count output will follow. If the count is minimum (0), the Terminal Count output transition will be in phase. If the count is maximum (9 for '168A or 15 for 169A, the Terminal Count output will be out of phase.

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

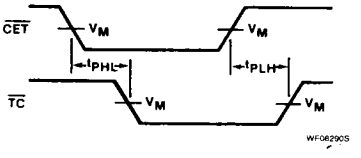
PARAMETER		TEST CONDITIONS	74LS		74S		UNIT
			Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	25		10		ns
t_s	Setup time, data to clock	Waveform 4	20		6		ns
t_h	Hold time, data to clock	Waveform 4	0		1		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 4	25		9		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 4	0		0		ns
t_s	Setup time, $\overline{CEP}$ & $\overline{CET}$ to clock	Waveform 5	20		16		ns
t_h	Hold time, $\overline{CEP}$ & $\overline{CET}$ to clock	Waveform 5	0		0		ns
t_s	Setup time, U/$\overline{D}$ to clock	Waveform 6	30		20		ns
t_h	Hold time, U/$\overline{D}$ to clock	Waveform 6	0		0		ns

AC WAVEFORMS



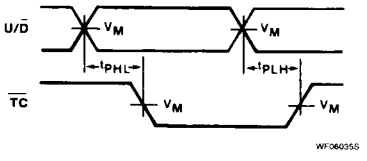
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 1. Clock To Output Delays And Clock Pulse Width



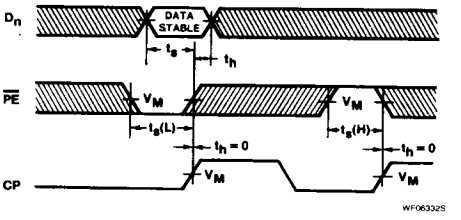
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 2. Propagation Delays CET Input To Terminal Count Output



V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

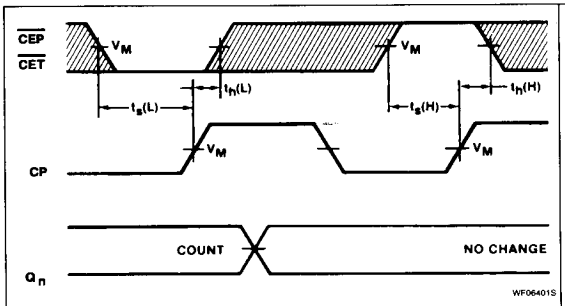
Waveform 3. Propagation Delays U/D Control To Terminal Count Output



V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

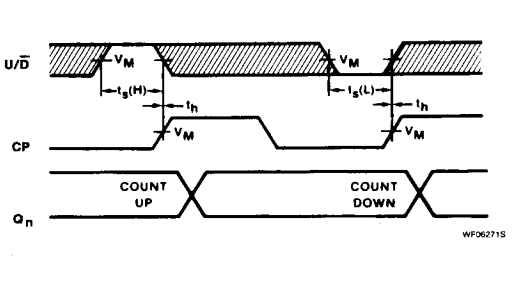
Waveform 4. Parallel Data And Parallel Enable Set-up And Hold Times

AC WAVEFORMS (Continued)



V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5. Count Enable Set-up And Hold Times



V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 6. Up/Down Control Set-up And Hold Times

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