

Precision Switchmode Pulse Width Modulation Control Circuit

TL594

The TL594 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control.

Features

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator with Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push-Pull or Single-Ended Operation
- Undervoltage Lockout
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant*

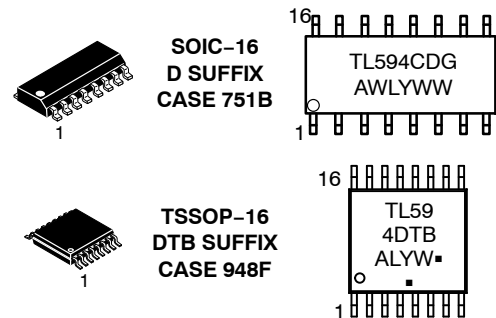
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	V
Collector Output Current (Each Transistor) (Note 1)	I_{C1}, I_{C2}	500	mA
Amplifier Input Voltage Range	V_{IR}	-0.3 to +42	V
Power Dissipation @ $T_A \leq 45^\circ\text{C}$	P_D	1000	mW
Thermal Resistance Junction-to-Ambient (PDIP) Junction-to-Air (TSSOP) Junction-to-Ambient (SOIC)	$R_{\theta JA}$	80 140 135	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$
Operating Ambient Temperature Range TL594CD, CN, CDTB	T_A	-40 to 85	$^\circ\text{C}$
Derating Ambient Temperature	T_A	45	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

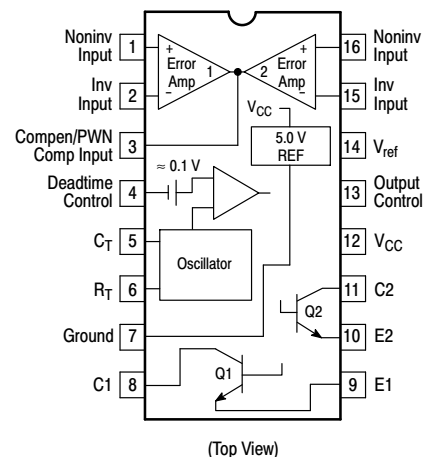
1. Maximum thermal limits must be observed.

MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	–	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	–	–	200	mA
Amplified Input Voltage	V_{in}	0.3	–	$V_{CC} - 2.0$	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	30	500	k Ω
Timing Capacitor	C_T	0.0047	0.001	10	μ F
Oscillator Frequency	f_{osc}	1.0	40	300	kHz
PWM Input Voltage (Pins 3, 4, 13)	–	0.3	–	5.3	V

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15$ V, $C_T = 0.01$ μ F, $R_T = 12$ k Ω , unless otherwise noted.)For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
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REFERENCE SECTION

Reference Voltage ($I_O = 1.0$ mA, $T_A = 25^\circ\text{C}$) ($I_O = 1.0$ mA)	V_{ref}	4.925 4.9	5.0 –	5.075 5.1	V
Line Regulation ($V_{CC} = 7.0$ V to 40 V)	Reg_{line}	–	2.0	25	mV
Load Regulation ($I_O = 1.0$ mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Short Circuit Output Current ($V_{ref} = 0$ V)	I_{SC}	15	40	75	mA

OUTPUT SECTION

Collector Off-State Current ($V_{CC} = 40$ V, $V_{CE} = 40$ V)	$I_{C(off)}$	–	2.0	100	μ A
Emitter Off-State Current ($V_{CC} = 40$ V, $V_C = 40$ V, $V_E = 0$ V)	$I_{E(off)}$	–	–	–100	μ A
Collector-Emitter Saturation Voltage (Note 1) Common-Emitter ($V_E = 0$ V, $I_C = 200$ mA) Emitter-Follower ($V_C = 15$ V, $I_E = -200$ mA)	$V_{SAT(C)}$ $V_{SAT(E)}$	– –	1.1 1.5	1.3 2.5	V
Output Control Pin Current Low State ($V_{OC} \leq 0.4$ V) High State ($V_{OC} = V_{ref}$)	I_{OCL} I_{OCH}	– –	0.1 2.0	– 20	μ A
Output Voltage Rise Time Common-Emitter (See Figure 13) Emitter-Follower (See Figure 14)	t_r	– –	100 100	200 200	ns
Output Voltage Fall Time Common-Emitter (See Figure 13) Emitter-Follower (See Figure 14)	t_f	– –	40 40	100 100	ns

ERROR AMPLIFIER SECTION

Input Offset Voltage (V_O (Pin 3) = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current (V_O (Pin 3) = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias Current (V_O (Pin 3) = 2.5 V)	I_{IB}	–	–0.1	–1.0	μ A
Input Common Mode Voltage Range ($V_{CC} = 40$ V, $T_A = 25^\circ\text{C}$)	V_{ICR}	0 to $V_{CC} - 2.0$			V
Inverting Input Voltage Range	$V_{IR(INV)}$	–0.3 to $V_{CC} - 2.0$			V
Open Loop Voltage Gain ($\Delta V_O = 3.0$ V, $V_O = 0.5$ V to 3.5 V, $R_L = 2.0$ k Ω)	A_{VOL}	70	95	–	dB
Unity-Gain Crossover Frequency ($V_O = 0.5$ V to 3.5 V, $R_L = 2.0$ k Ω)	f_C	–	700	–	kHz
Phase Margin at Unity-Gain ($V_O = 0.5$ V to 3.5 V, $R_L = 2.0$ k Ω)	ϕ_m	–	65	–	deg.
Common Mode Rejection Ratio ($V_{CC} = 40$ V)	CMRR	65	90	–	dB
Power Supply Rejection Ratio ($\Delta V_{CC} = 33$ V, $V_O = 2.5$ V, $R_L = 2.0$ k Ω)	PSRR	–	100	–	dB
Output Sink Current (V_O (Pin 3) = 0.7 V)	I_{O-}	0.3	0.7	–	mA
Output Source Current (V_O (Pin 3) = 3.5 V)	I_{O+}	–2.0	–4.0	–	mA

1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, unless otherwise noted.)

For typical values $T_A = 25^\circ\text{C}$, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
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PWM COMPARATOR SECTION (Test Circuit Figure 11)

Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	3.6	4.5	V
Input Sink Current ($V_{Pin\ 3} = 0.7\text{ V}$)	I_{L-}	0.3	0.7	–	mA

DEADTIME CONTROL SECTION (Test Circuit Figure 11)

Input Bias Current (Pin 4) ($V_{Pin\ 4} = 0\text{ V}$ to 5.25 V)	$I_{IB}\text{ (DT)}$	–	–2.0	–10	μA
Maximum Duty Cycle, Each Output, Push–Pull Mode ($V_{Pin\ 4} = 0\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$) ($V_{Pin\ 4} = 0\text{ V}$, $C_T = 0.001\text{ }\mu\text{F}$, $R_T = 30\text{ k}\Omega$)	DC_{max}	45 –	48 45	50 –	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	– 0	2.8 –	3.3 –	V

OSCILLATOR SECTION

Frequency ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 30\text{ k}\Omega$) ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, $T_A = 25^\circ\text{C}$) ($C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, $T_A = T_{low}$ to T_{high})	f_{osc}	– 9.2 9.0	40 10 –	– 10.8 12	kHz
Standard Deviation of Frequency* ($C_T = 0.001\text{ }\mu\text{F}$, $R_T = 30\text{ k}\Omega$)	σf_{osc}	–	1.5	–	%
Frequency Change with Voltage ($V_{CC} = 7.0\text{ V}$ to 40 V , $T_A = 25^\circ\text{C}$)	$\Delta f_{osc}\text{ (}\Delta V\text{)}$	–	0.2	1.0	%
Frequency Change with Temperature ($\Delta T_A = T_{low}$ to T_{high} , $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$)	$\Delta f_{osc}\text{ (}\Delta T\text{)}$	–	4.0	–	%

UNDERVOLTAGE LOCKOUT SECTION

Turn–On Threshold (V_{CC} Increasing, $I_{ref} = 1.0\text{ mA}$) $T_A = 25^\circ\text{C}$ $T_A = T_{low}$ to T_{high}	V_{th}	4.0 3.5	5.2 –	6.0 6.5	V
Hysteresis TL594C,I TL594M	V_H	100 50	150 150	300 300	mV

TOTAL DEVICE

Standby Supply Current (Pin 6 at V_{ref} , All other inputs and outputs open) ($V_{CC} = 15\text{ V}$) ($V_{CC} = 40\text{ V}$)	I_{CC}	– –	8.0 8.0	15 18	mA
Average Supply Current ($V_{Pin\ 4} = 2.0\text{ V}$, $C_T = 0.01\text{ }\mu\text{F}$, $R_T = 12\text{ k}\Omega$, $V_{CC} = 15\text{ V}$, See Figure 11)		–	11	–	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^N (X_n - \bar{X})^2}{N - 1}}$

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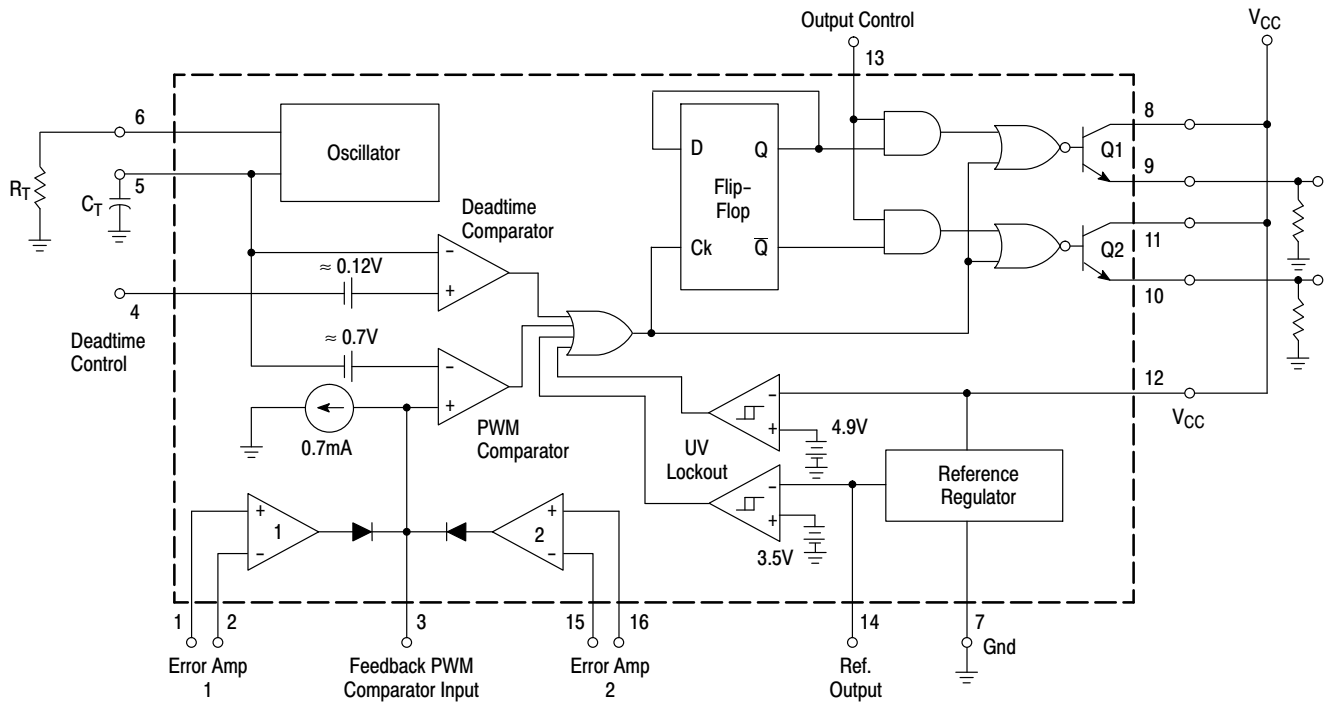


Figure 1. Representative Block Diagram

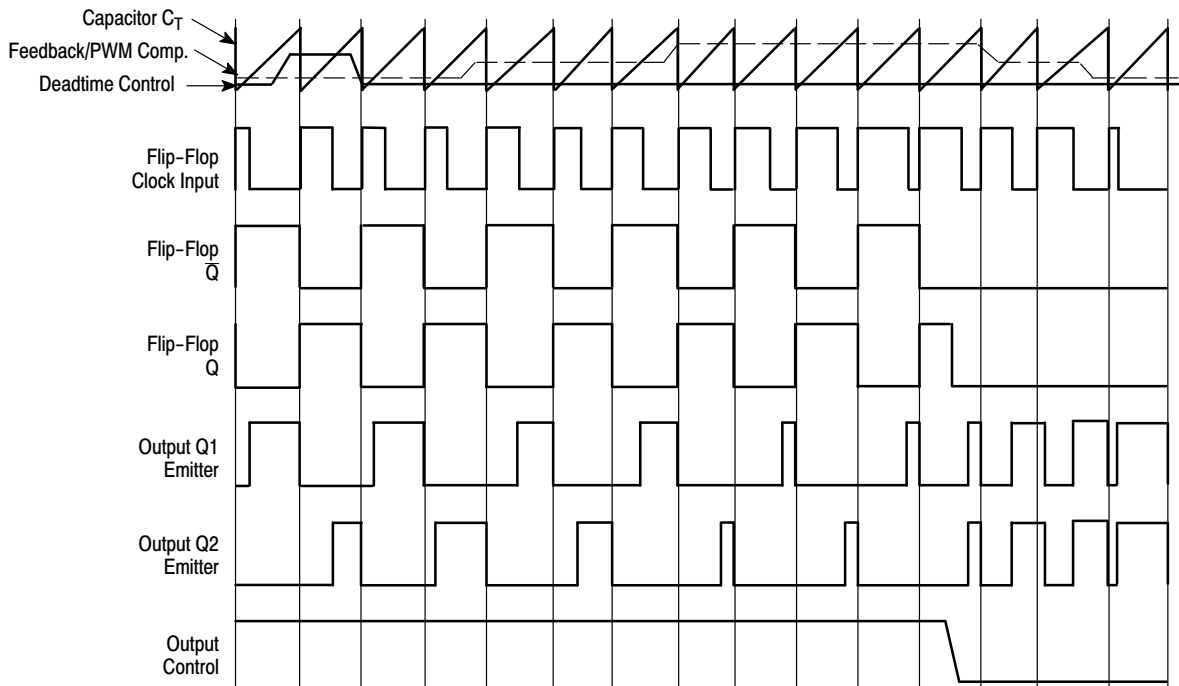


Figure 2. Timing Diagram

APPLICATIONS INFORMATION

Description

The TL594 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T . The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime-control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a

common-mode input range from -0.3 V to $(V_{CC} - 2)$ V, and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

Functional Table

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}} =$
Grounded	Single-ended PWM @ Q1 and Q2	1.0
@ V_{ref}	Push-pull Operation	0.5

When capacitor C_T is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL594 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of $\pm 1.5\%$ with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C .

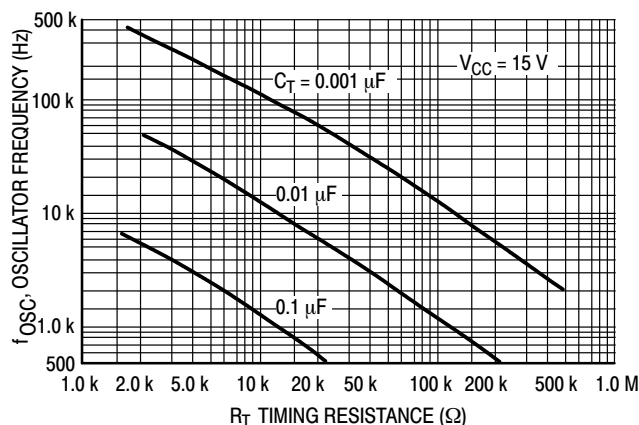


Figure 3. Oscillator Frequency versus Timing Resistance

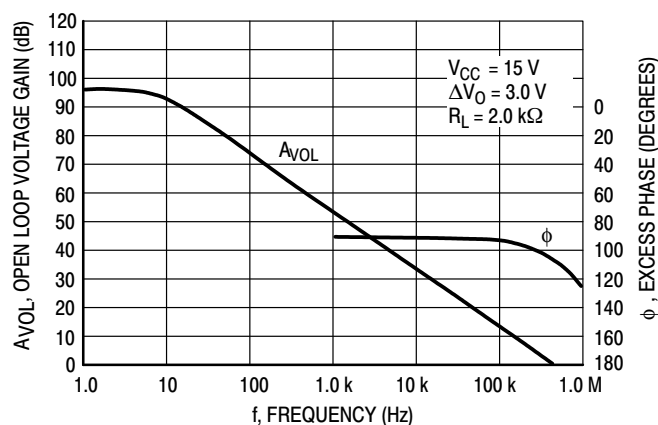


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

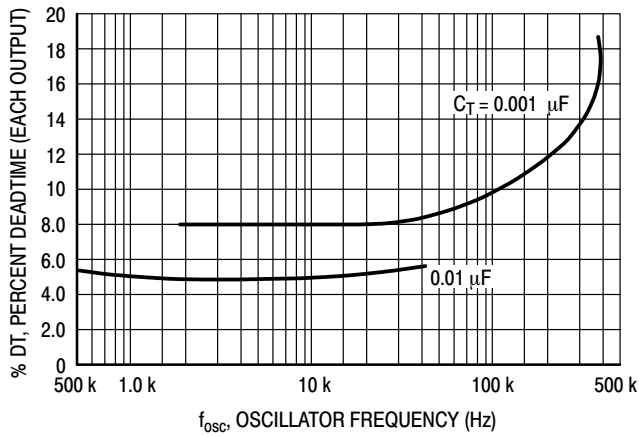


Figure 5. Percent Deadtime versus Oscillator Frequency

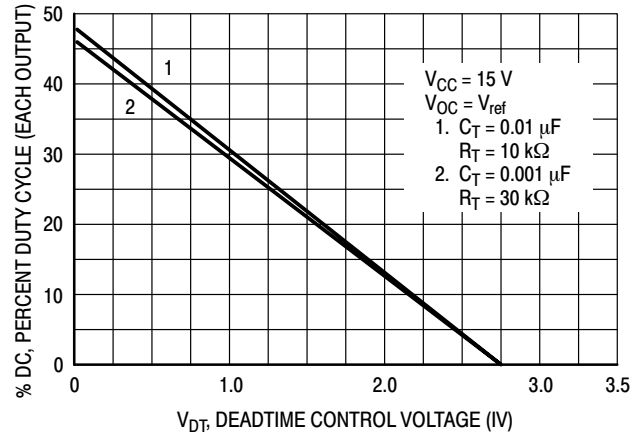


Figure 6. Percent Duty Cycle versus Deadtime Control Voltage

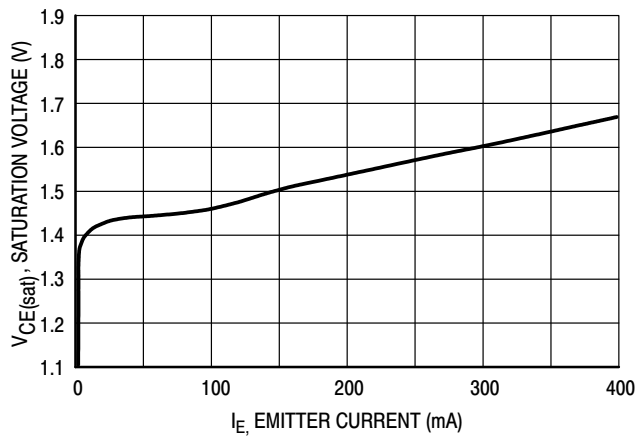


Figure 7. Emitter-Follower Configuration Output Saturation Voltage versus Emitter Current

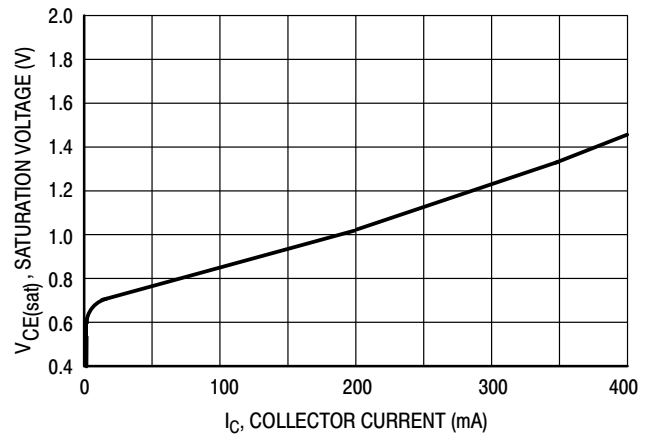


Figure 8. Common-Emitter Configuration Output Saturation Voltage versus Collector Current

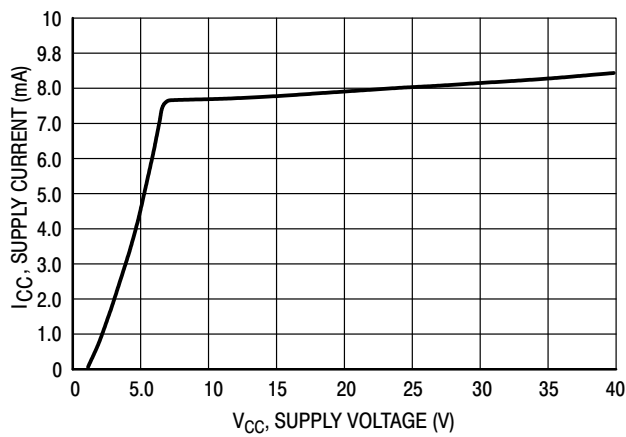


Figure 9. Standby Supply Current versus Supply Voltage

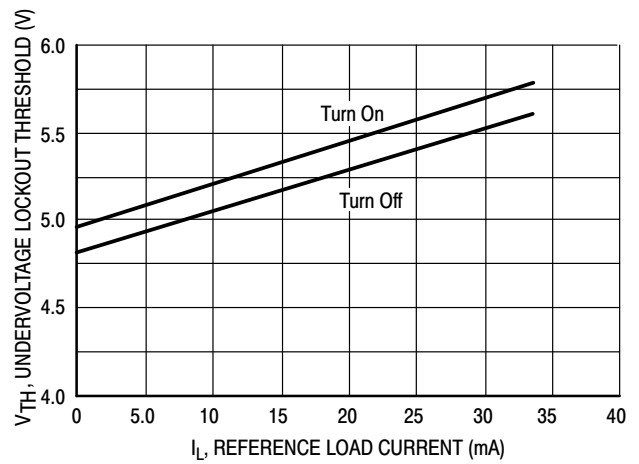


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

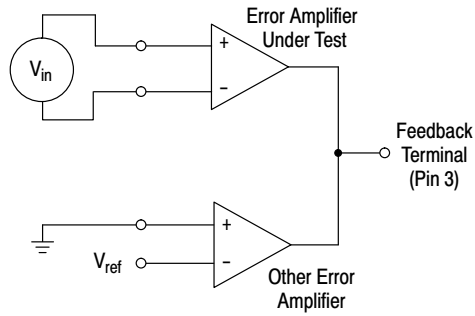


Figure 11. Error-Amplifier Characteristics

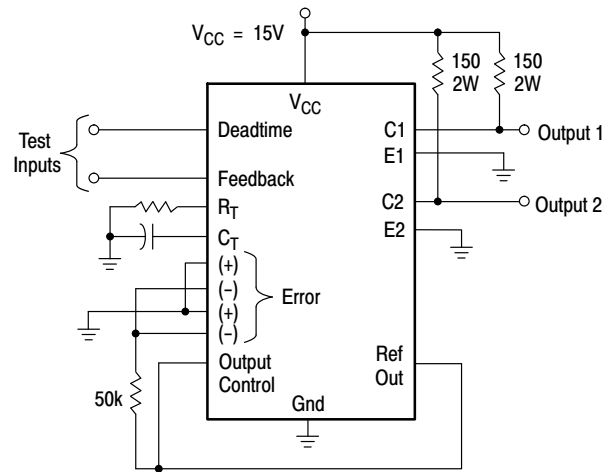


Figure 12. Deadtime and Feedback Control Circuit

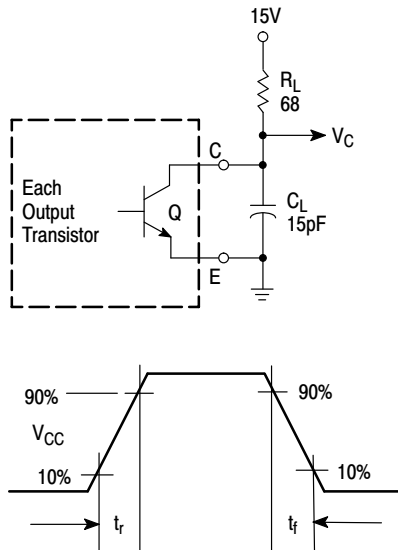


Figure 13. Common-Emitter Configuration Test Circuit and Waveform

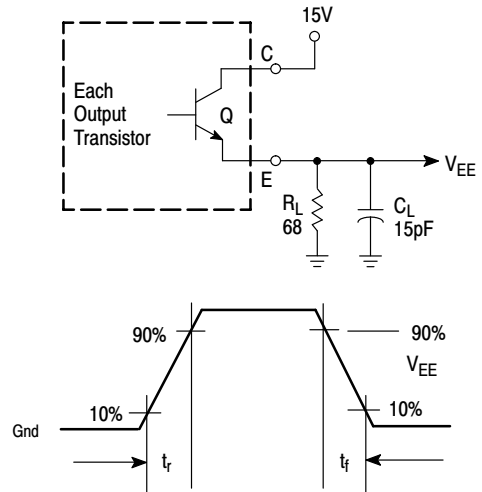


Figure 14. Emitter-Follower Configuration Test Circuit and Waveform

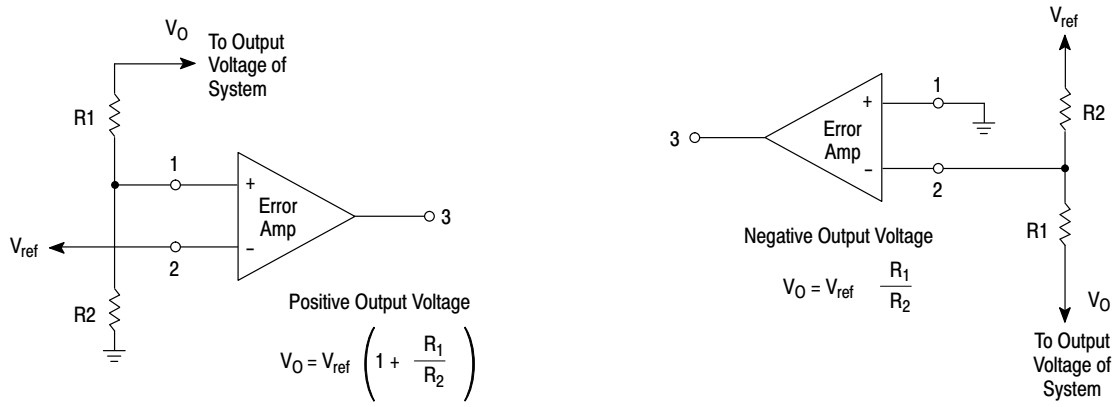


Figure 15. Error-Amplifier Sensing Techniques

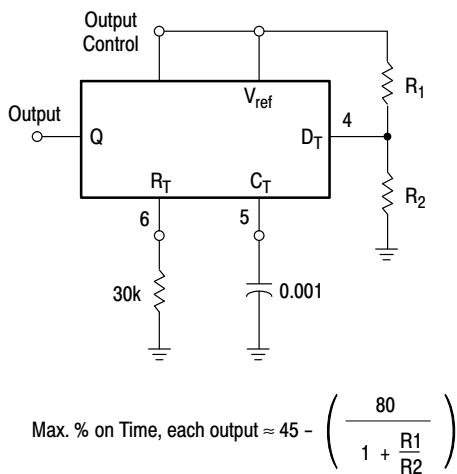


Figure 16. Deadtime Control Circuit

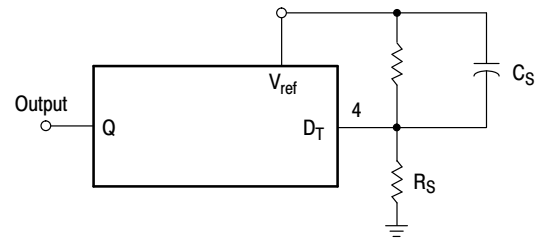


Figure 17. Soft-Start Circuit

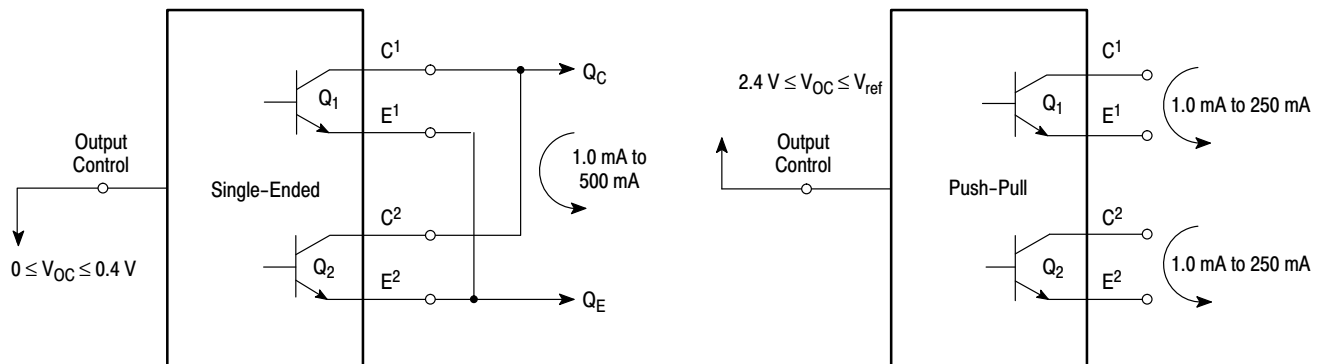


Figure 18. Output Connections for Single-Ended and Push-Pull Configurations

TL594

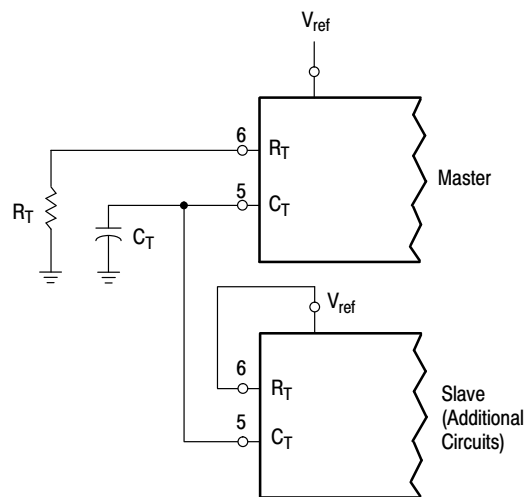


Figure 19. Slaving Two or More Control Circuits

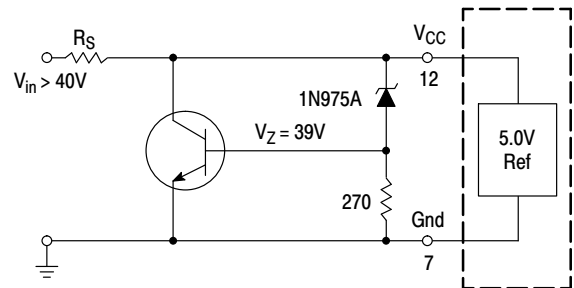


Figure 20. Operation with $V_{in} > 40\text{ V}$ Using External Zener

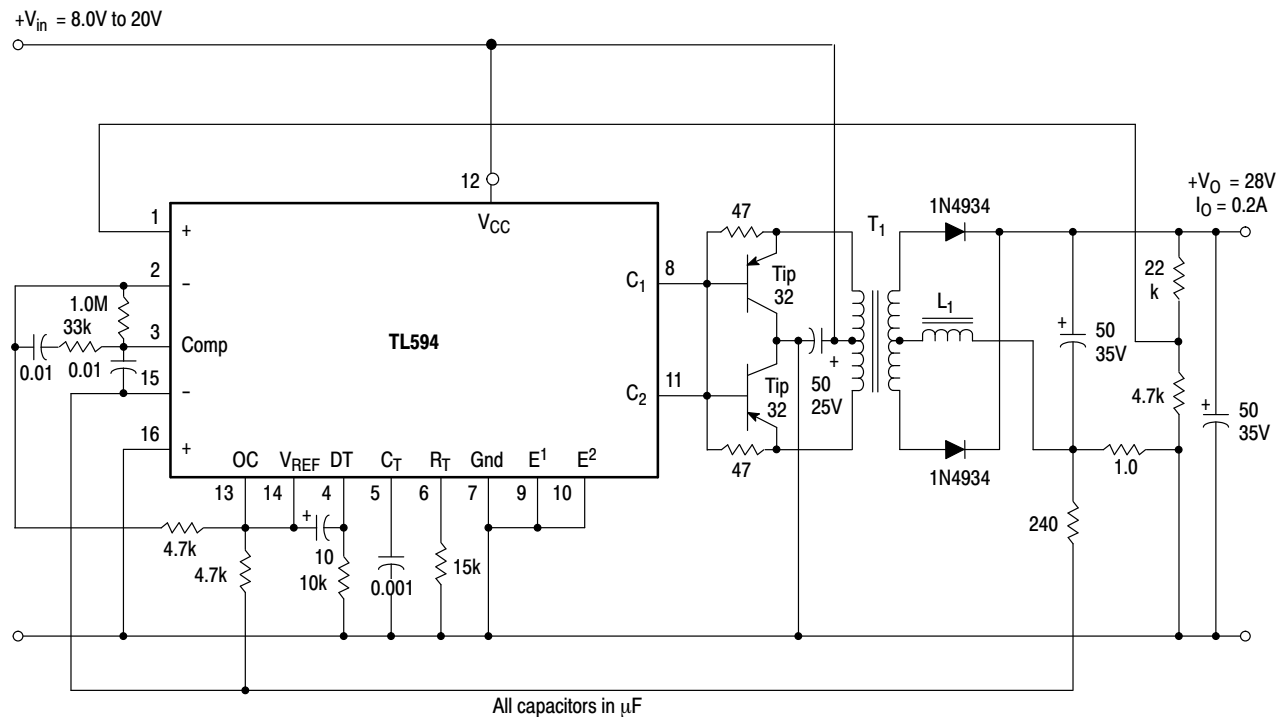


Figure 21. Pulse Width Modulated Push-Pull Converter

Test	Conditions	Results	L1 - 3.5 mH @ 0.3 A T1 - Primary: 20T C.T. #28 AWG Secondary: 120T C.T. #36 AWG Core: Ferroxcube 1408P-L00-3CB
Line Regulation	$V_{in} = 10\text{ V to }40\text{ V}$	14 mV 0.28%	
Load Regulation	$V_{in} = 28\text{ V}, I_O = 1.0\text{ mA to }1.0\text{ A}$	3.0 mV 0.06%	
Output Ripple	$V_{in} = 28\text{ V}, I_O = 1.0\text{ A}$	65 mVpp P.A.R.D.	
Short Circuit Current	$V_{in} = 28\text{ V}, R_L = 0.1\ \Omega$	1.6 A	
Efficiency	$V_{in} = 28\text{ V}, I_O = 1.0\text{ A}$	71%	

TL594

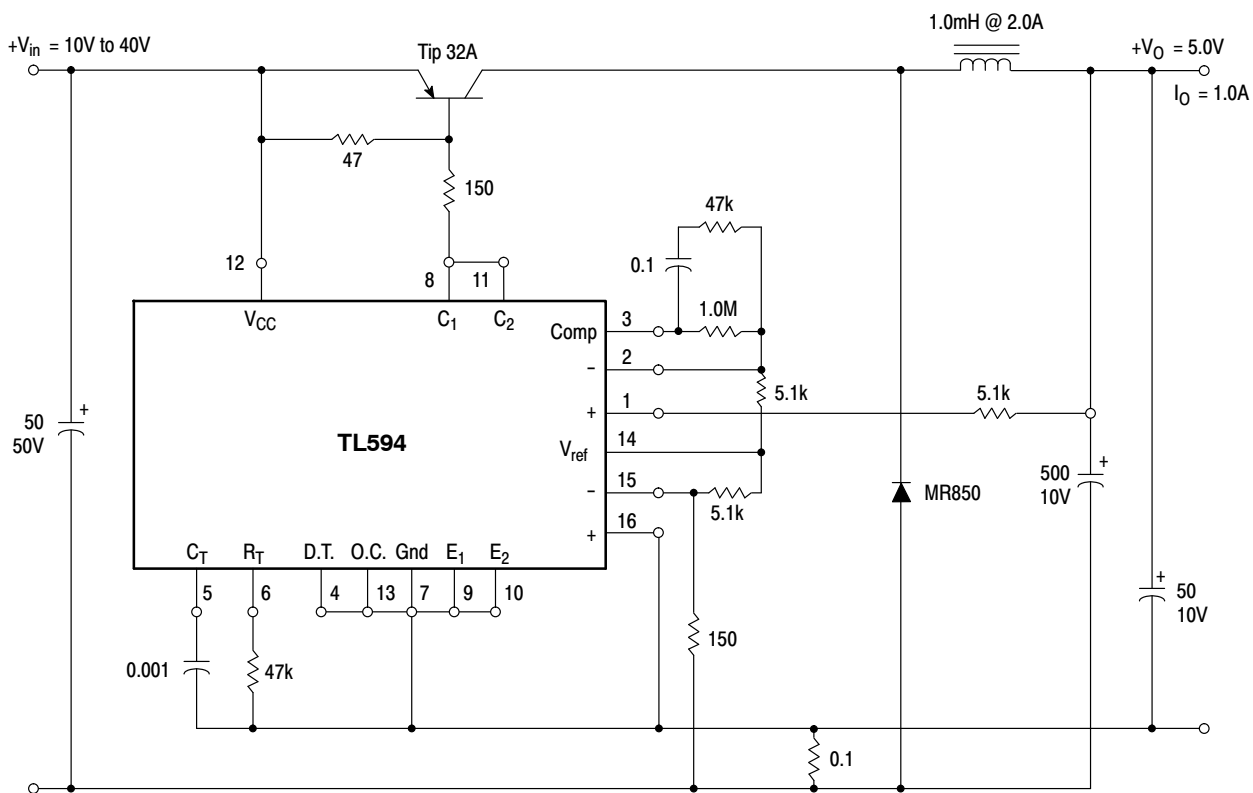


Figure 22. Pulse Width Modulated Step-Down Converter

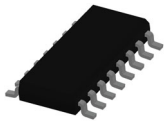
Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 40 \text{ V}$	3.0 mV 0.01%
Load Regulation	$V_{in} = 12.6 \text{ V}, I_O = 0.2 \text{ mA to } 200 \text{ mA}$	5.0 mV 0.02%
Output Ripple	$V_{in} = 12.6 \text{ V}, I_O = 200 \text{ mA}$	40 mVpp P.A.R.D.
Short Circuit Current	$V_{in} = 12.6 \text{ V}, R_L = 0.1 \Omega$	250 mA
Efficiency	$V_{in} = 12.6 \text{ V}, I_O = 200 \text{ mA}$	72%

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping [†]
TL594CDR2G	−40 to 85°C	SOIC−16 (Pb−Free)	2500 Tape & Reel
TL594CDTBR2G	−40 to 85°C	TSSOP−16*	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

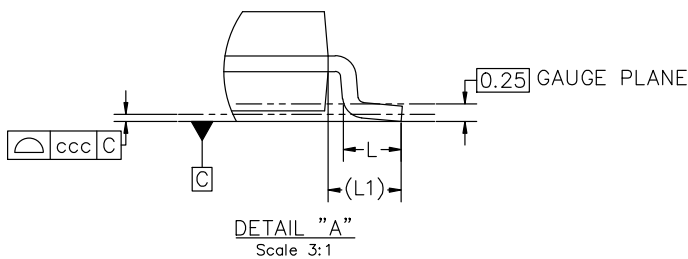
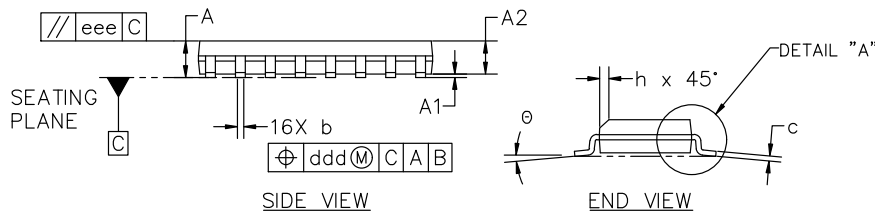
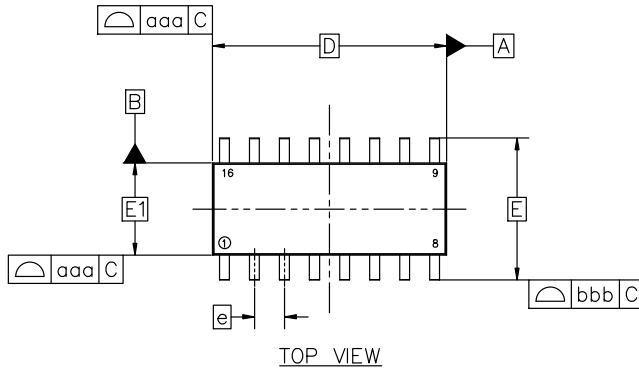


SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

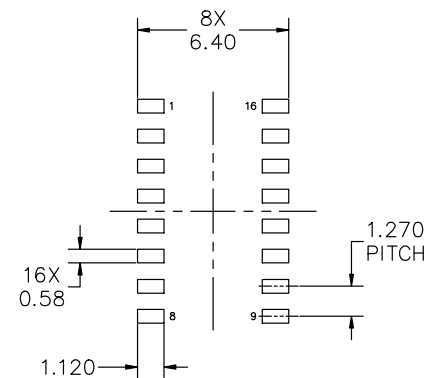
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NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE onsemi SOLDERING
AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D

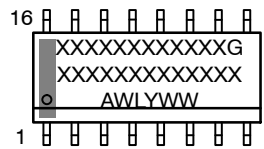
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DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P	PAGE 1 OF 2

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SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC
MARKING DIAGRAM*

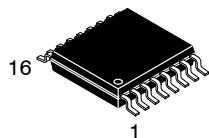


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

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TSSOP-16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

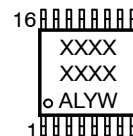

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***


*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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