

512K x 32 Static RAM

Features

- **High speed**
— $t_{AA} = 8 \text{ ns}$
- **Low active power**
— 1080 mW (max.)
- **Operating voltages of $3.3 \pm 0.3\text{V}$**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ features**
- **Available in non Pb-free 119-ball PBGA package**

Functional Description

The CY7C1062AV33 is a high-performance CMOS Static RAM organized as 524,288 words by 32 bits.

Writing to the device is accomplished by enabling the chip ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW) and forcing the Write Enable (WE) input LOW. If Byte Enable A ($\overline{B}_A$) is LOW, then data from I/O

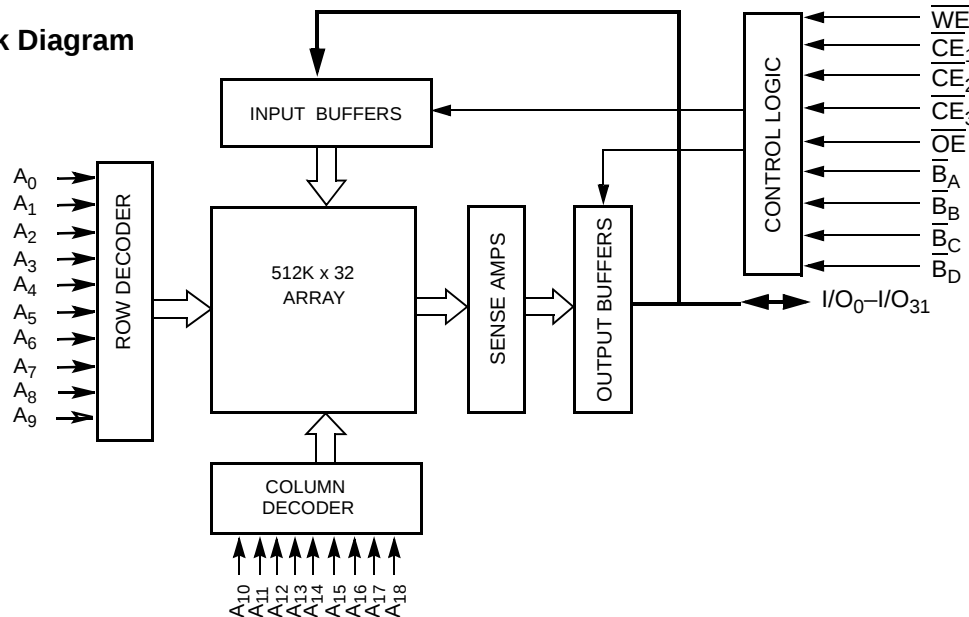
pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₈). If Byte Enable B ($\overline{B}_B$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₈). Likewise, $\overline{B}_C$ and $\overline{B}_D$ correspond with the I/O pins I/O₁₆ to I/O₂₃ and I/O₂₄ to I/O₃₁, respectively.

Reading from the device is accomplished by enabling the chip ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW) while forcing the Output Enable ($\overline{OE}$) LOW and Write Enable (WE) HIGH. If the first Byte Enable ($\overline{B}_A$) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte Enable B ($\overline{B}_B$) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. Similarly, $\overline{B}_C$ and $\overline{B}_D$ correspond to the third and fourth bytes. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O₀ through I/O₃₁) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$, $\overline{CE}_2$ or $\overline{CE}_3$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the byte selects are disabled ($\overline{B}_A$ -D HIGH), or during a write operation ($\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ LOW, and WE LOW).

The CY7C1062AV33 is available in a 119-ball pitch ball grid array (PBGA) package.

Logic Block Diagram



Selection Guide

		-8	-10	-12	Unit
Maximum Access Time		8	10	12	ns
Maximum Operating Current	Com'I	300	275	260	mA
	Ind'I	300	275	260	
Maximum CMOS Standby Current	Com'I/Ind'I	50	50	50	mA

Pin Configurations^[1, 2]
119-ball PBGA
(Top View)

	1	2	3	4	5	6	7
A	I/O ₁₆	A	A	A	A	A	I/O ₀
B	I/O ₁₇	A	A	$\overline{CE}_1$	A	A	I/O ₁
C	I/O ₁₈	$\overline{B}_c$	$\overline{CE}_2$	NC	$\overline{CE}_3$	$\overline{B}_a$	I/O ₂
D	I/O ₁₉	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₃
E	I/O ₂₀	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₄
F	I/O ₂₁	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₅
G	I/O ₂₂	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₆
H	I/O ₂₃	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₇
J	NC	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	DNU
K	I/O ₂₄	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₈
L	I/O ₂₅	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₉
M	I/O ₂₆	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₀
N	I/O ₂₇	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₁₁
P	I/O ₂₈	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁₂
R	I/O ₂₉	A	$\overline{B}_d$	NC	$\overline{B}_b$	A	I/O ₁₃
T	I/O ₃₀	A	A	$\overline{WE}$	A	A	I/O ₁₄
U	I/O ₃₁	A	A	$\overline{OE}$	A	A	I/O ₁₅

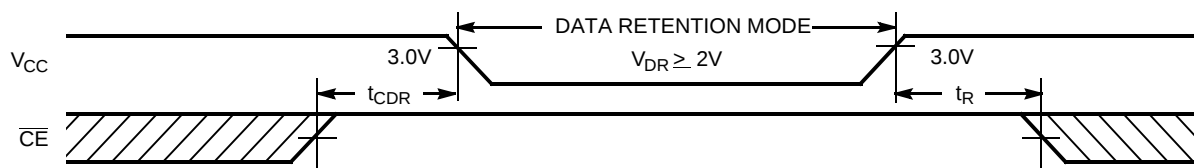
Notes:

1. NC pins are not connected on the die.
2. DNU pins have to be left floating or tied to VSS to ensure proper application.

- CY7C1062AV33**

AC Switching Characteristics Over the Operating Range^[6]

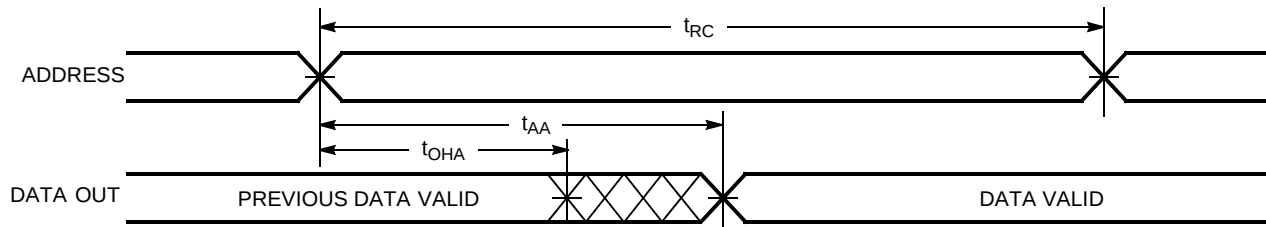
Parameter	Description	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{power}	V _{CC} (typical) to the first access ^[7]	1		1		1		ms
t _{RC}	Read Cycle Time	8		10		12		ns
t _{AA}	Address to Data Valid		8		10		12	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	$\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, or $\overline{\text{CE}}_3$ LOW to Data Valid		8		10		12	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		5		5		6	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low-Z ^[8]	1		1		1		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High-Z ^[8]		5		5		6	ns
t _{LZCE}	$\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, or $\overline{\text{CE}}_3$ LOW to Low-Z ^[8]	3		3		3		ns
t _{HZCE}	$\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, or $\overline{\text{CE}}_3$ HIGH to High-Z ^[8]		5		5		6	ns
t _{PU}	$\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, or $\overline{\text{CE}}_3$ LOW to Power-up ^[9]	0		0		0		ns
t _{PD}	$\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, or $\overline{\text{CE}}_3$ HIGH to Power-down ^[9]		8		10		12	ns
t _{DBE}	Byte Enable to Data Valid		5		5		6	ns
t _{LZBE}	Byte Enable to Low-Z ^[8]	1		1		1		ns
t _{HZBE}	Byte Disable to High-Z ^[8]		5		5		6	ns
Write Cycle ^[10, 11]								
t _{WC}	Write Cycle Time	8		10		12		ns
t _{SCE}	$\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, or $\overline{\text{CE}}_3$ LOW to Write End	6		7		8		ns
t _{AW}	Address Set-up to Write End	6		7		8		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	6		7		8		ns
t _{SD}	Data Set-up to Write End	5		5.5		6		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low-Z ^[8]	3		3		3		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High-Z ^[8]		5		5		6	ns
t _{BW}	Byte Enable to End of Write	6		7		8		ns

Data Retention Waveform

Notes:

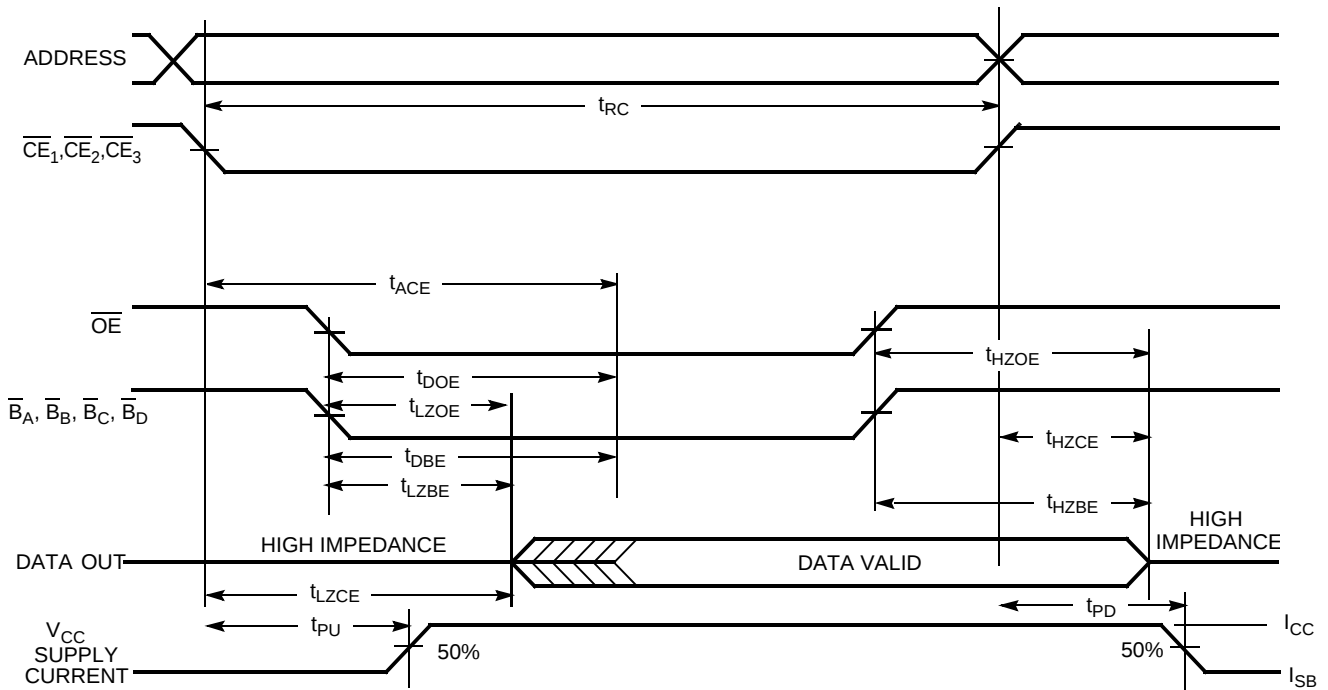
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{\text{OL}}/I_{\text{OH}}$ and transmission line loads. Test conditions for the read cycle use output loading as shown in (a) of AC Test Loads, unless specified otherwise.
- This part has a voltage regulator that steps down the voltage from 3V to 2V internally. t_{power} time has to be provided initially before a read/write operation is started.
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} , and t_{LZOE} , t_{LZCE} , t_{LZWE} , and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}_1$ LOW, $\overline{\text{CE}}_2$ HIGH, $\overline{\text{CE}}_3$ LOW, and $\overline{\text{WE}}$ LOW. The chip enables must be active and $\overline{\text{WE}}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Read Cycle No. 1^[12, 13]

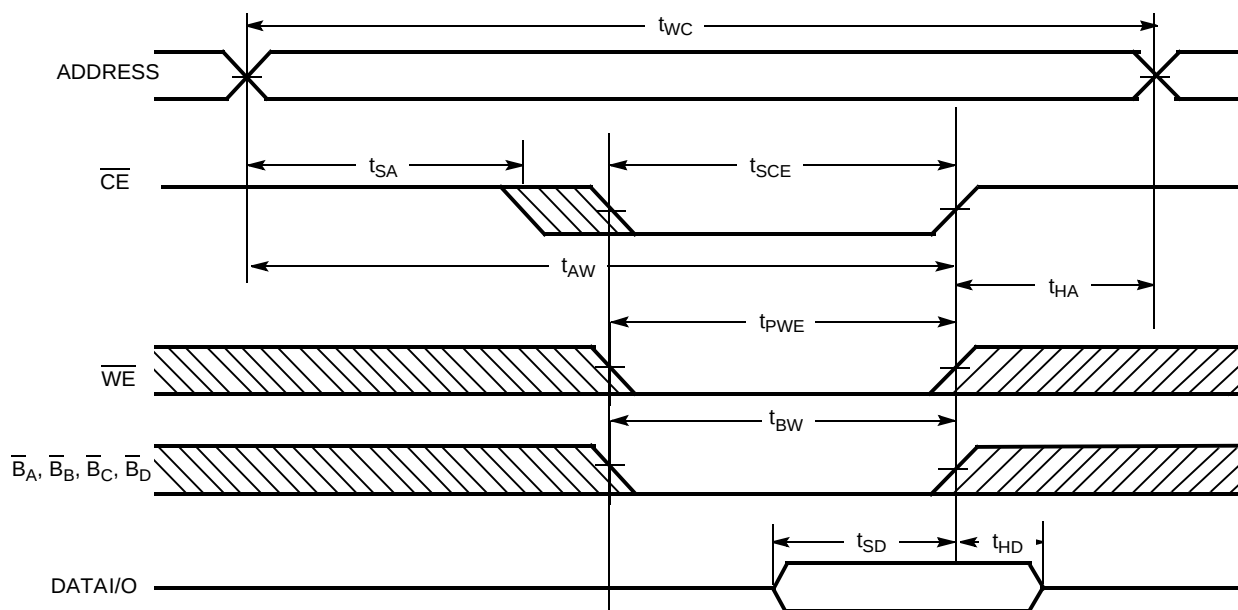
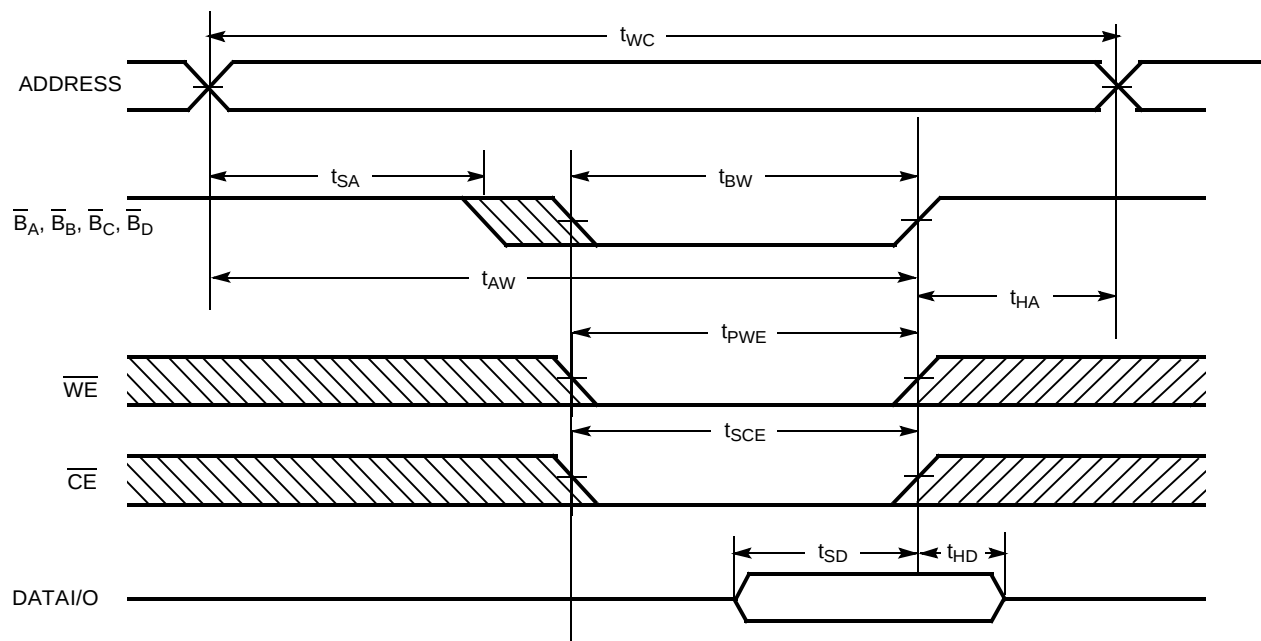


Read Cycle No. 2 ($\overline{OE}$ Controlled)^[13, 14]



Notes:

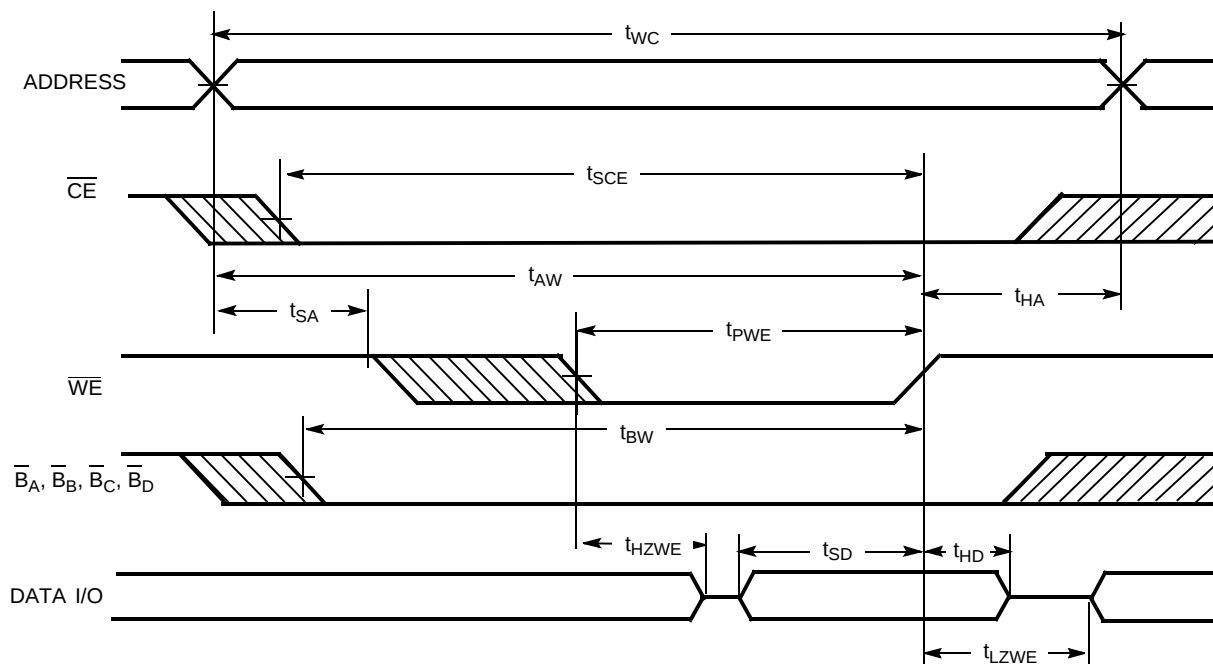
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D = V_{IL}$.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[15, 16, 17]

Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)^[15, 16, 17]

Notes:

15. $\overline{\text{CE}}$ indicates a combination of all three chip enables. When ACTIVE LOW, $\overline{\text{CE}}$ indicates the $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, and $\overline{\text{CE}}_3$ are LOW.

16. Data I/O is high-impedance if $\overline{\text{OE}}$ or $\overline{\text{B}}_{\text{A}}, \overline{\text{B}}_{\text{B}}, \overline{\text{B}}_{\text{C}}, \overline{\text{B}}_{\text{D}} = V_{\text{IH}}$.

17. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)

Truth Table

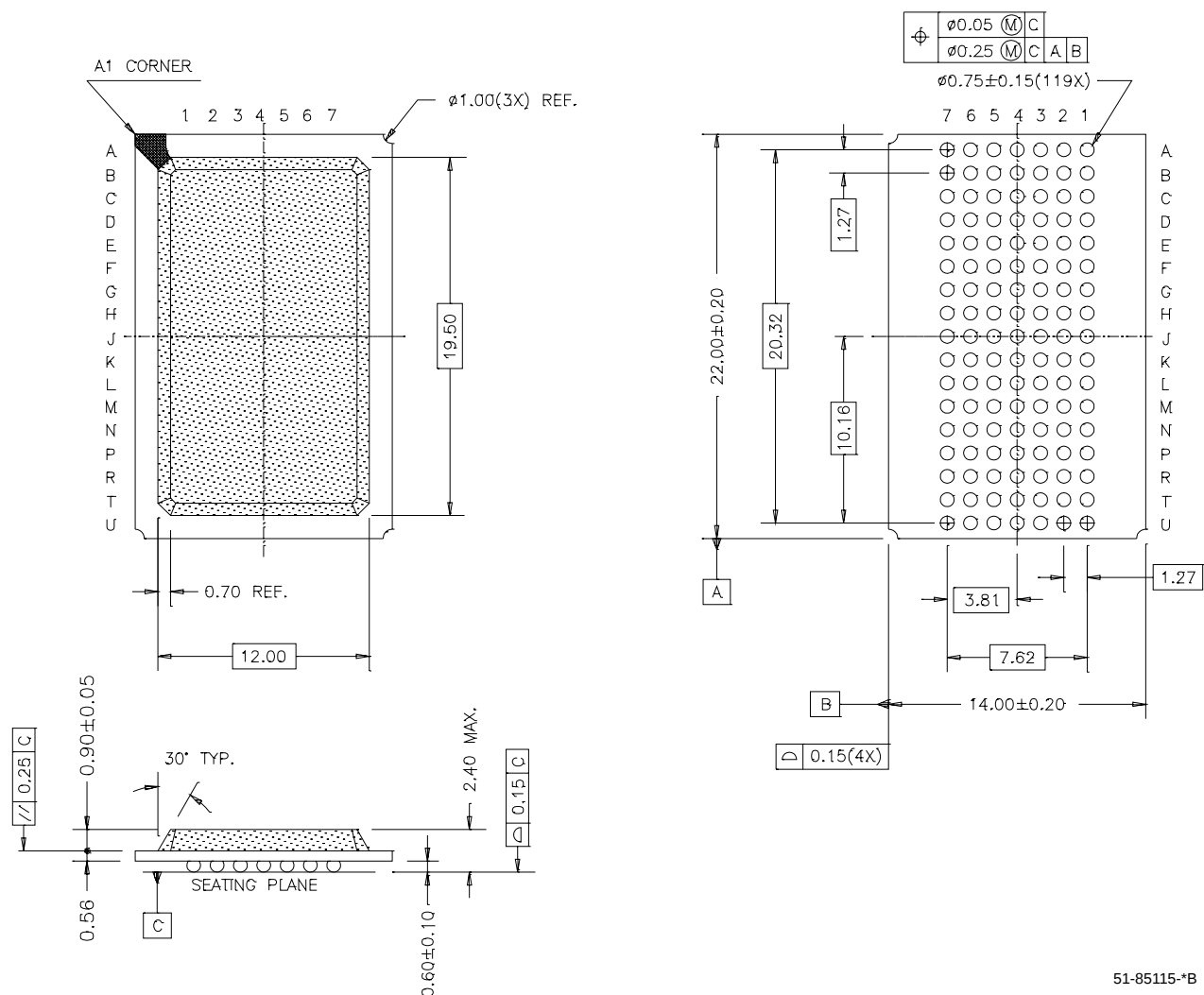
$\overline{CE}_1$	$\overline{CE}_2$	$\overline{CE}_3$	$\overline{OE}$	$\overline{WE}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	I/O ₀ – I/O ₇	I/O ₈ – I/O ₁₅	I/O ₁₆ – I/O ₂₃	I/O ₂₄ – I/O ₃₁	Mode	Power
H	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I _{SB})
X	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I _{SB})
X	X	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I _{SB})
L	L	L	L	H	L	L	L	L	Data Out	Data Out	Data Out	Data Out	Read All Bits	(I _{CC})
L	L	L	L	H	L	H	H	H	Data Out	High-Z	High-Z	High-Z	Read Byte A Bits Only	(I _{CC})
L	L	L	L	H	H	L	H	H	High-Z	Data Out	High-Z	High-Z	Read Byte B Bits Only	(I _{CC})
L	L	L	L	H	H	H	L	H	High-Z	High-Z	Data Out	High-Z	Read Byte C Bits Only	(I _{CC})
L	L	L	L	H	H	H	H	L	High-Z	High-Z	High-Z	Data Out	Read Byte D Bits Only	(I _{CC})
L	L	L	X	L	L	L	L	L	Data In	Data In	Data In	Data In	Write All Bits	(I _{CC})
L	L	L	X	L	L	H	H	H	Data In	High-Z	High-Z	High-Z	Write Byte A Bits Only	(I _{CC})
L	L	L	X	L	H	L	H	H	High-Z	Data In	High-Z	High-Z	Write Byte B Bits Only	(I _{CC})
L	L	L	X	L	H	H	L	H	High-Z	High-Z	Data In	High-Z	Write Byte C Bits Only	(I _{CC})
L	L	L	X	L	H	H	H	L	High-Z	High-Z	High-Z	Data In	Write Byte D Bits Only	(I _{CC})
L	L	L	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Selected, Outputs Disabled	(I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C1062AV33-8BGC	51-85115	119-ball (14 x 22 x 2.4 mm) PBGA	Commercial
10	CY7C1062AV33-10BGC			Industrial
	CY7C1062AV33-10BGI			
12	CY7C1062AV33-12BGC			Commercial
	CY7C1062AV33-12BGI			Industrial

Package Diagram

119-ball PBGA (14 x 22 x 2.4 mm) (51-85115)



51-85115-*B

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Document History Page

Document Title: CY7C1062AV33 512K x 32 Static RAM Document Number: 38-05137				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109752	02/27/02	HGK	New Data Sheet
*A	117059	09/19/02	DFP	Removed 15-ns bin and added 8-ns bin. Changed CE_2 TO CE_2 . Changed C_{IN} – input capacitance – from 6 pF to 8 pF. Changed C_{OUT} – output capacitance – from 8 pF to 10 pF.
*B	119389	10/07/02	DFP	Updated I_{CC} , T_{sd} , and T_{doe} parameters. Removed note 7 (I_Z/h_Z comment).
*C	120384	11/13/02	DFP	Final Data Sheet. Removed note 2. Added note 3 to “AC Test Loads and Waveforms” and note 7 to t_{pu} and t_{pd} .
*D	124440	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA
*E	329638	See ECN	RKF	Removed CE_2 waveform showing Active High signal timing on Page #5, and included it with the CE_1 , CE_3 waveform Corrected Truth Table on page 7 with CE_2 active low information
*F	492137	See ECN	NXR	Included note #1 and 2 on page #2 Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated Ordering Information Table