

# M59350FP

## Watchdog Timer IC with Built-in 5 V Constant-Voltage Power Supply

REJ03F0016-0100Z

Rev.1.00

Aug.25.2003

### Description

The M59350FP is an IC developed for use as a watchdog timer with a built-in 5 V constant-voltage power supply. It is provided with functions for power-on reset, constant voltage monitoring, and watchdog timer operation, and can be used as a power supply circuit for various systems. Because it employs a 15-pin flat package, it is ideal for compact system designs.

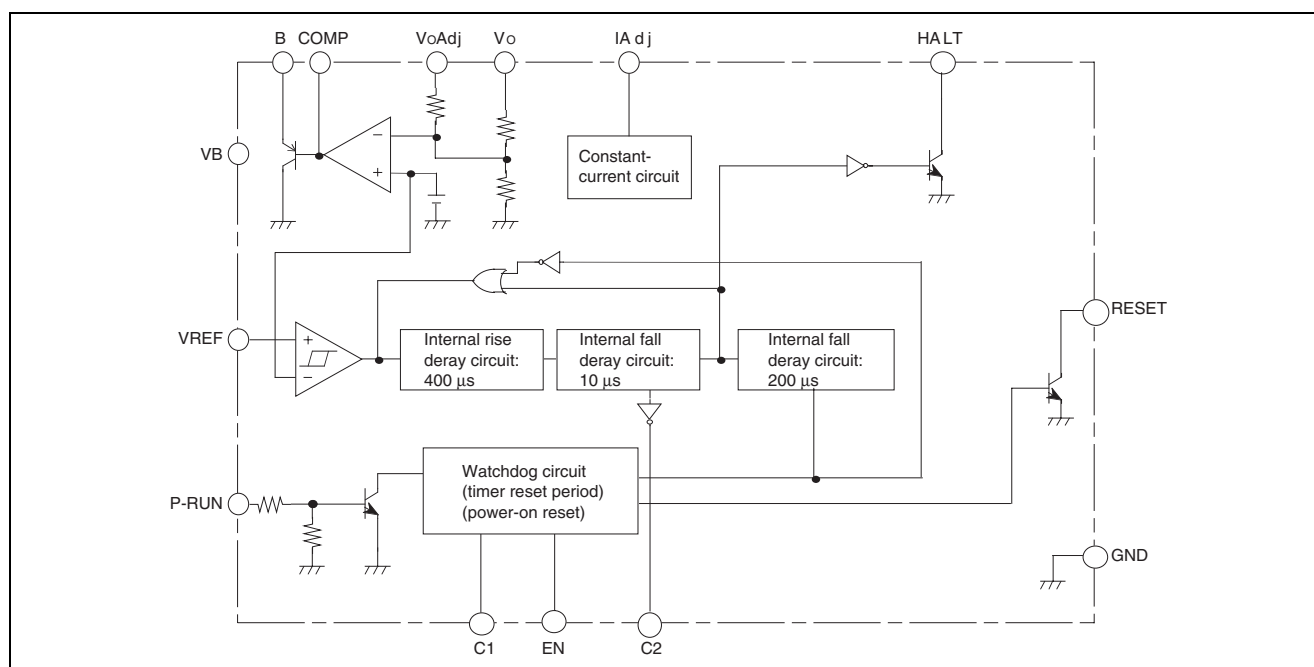
### Features

- Built-in power-on reset circuit
- Built-in 5 V constant-voltage power supply
- Built-in 5 V constant-voltage power supply monitoring circuit
- Built-in watchdog timer circuit
- Compact flat package (SOP, 14P2N, 1.27 mm pitch)

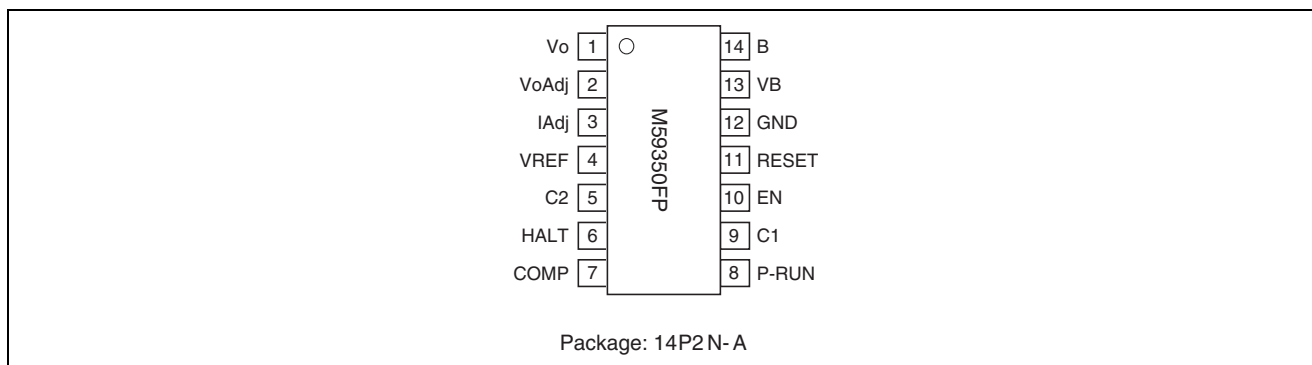
### Application

- ECU power supply circuit for automotive use
- Other automotive applications

### System Block Diagram



## Pin Arrangement (top view)



## Pin Description

| Pin no. | Pin symbol | Function                                                                                                                                                                                                                                                                                                          |
|---------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [1]     | Vo         | By connecting an external PNP transistor,<br>pin [1] (VO): 5 V constant voltage output<br>pin [1] (VO): PNP transistor collector connection<br>pin [13] (VB): PNP transistor emitter + power supply connection<br>pin [14] (B): PNP transistor base connection<br>(pin [1]: grounded via capacitor (100 $\mu$ F)) |
| [13]    | VB         |                                                                                                                                                                                                                                                                                                                   |
| [14]    | B          |                                                                                                                                                                                                                                                                                                                   |
| [2]     | VoAdj      |                                                                                                                                                                                                                                                                                                                   |
| [3]     | IAdj       | By connecting a load, adjusts pin [1] (V) constant voltage: 5 V                                                                                                                                                                                                                                                   |
| [4]     | VREF       | Sets charge/discharge current of capacitors to set time (C1, C2 within IC)                                                                                                                                                                                                                                        |
| [5]     | C2         | Monitors voltage, compares with set voltage to control pin [6] (HALT), pin [11] (RESET) output                                                                                                                                                                                                                    |
| [6]     | HALT       | Delay time from decision that pin [4] (VREF) is "L" until pin [6] (HALT) outputs "L" is set through the grounding capacitance (when open, the IC Built-in capacitance results in a delay time of 10 $\mu$ s)                                                                                                      |
| [7]     | COMP       | Outputs pin [4] (VREF) voltage monitoring result                                                                                                                                                                                                                                                                  |
| [8]     | P-RUN      | Pin for connection of constant-voltage power supply (Vo) phase compensation capacitance                                                                                                                                                                                                                           |
| [9]     | C1         | Detects voltage and period of input clock signal, controls pin [11] (RESET) output                                                                                                                                                                                                                                |
| [10]    | EN         | Sets the power-on reset time (T3), watchdog time (T2), watchdog reset pulse width (T1) time through the grounding capacitance                                                                                                                                                                                     |
| [11]    | RESET      | Halts the watchdog function on input of "L" level (open: H input fixed)                                                                                                                                                                                                                                           |
| [12]    | GND        | Outputs judgment result of pin [4] (VREF) voltage monitoring, pin [8] (P-RUN) input clock signal                                                                                                                                                                                                                  |
|         |            | GND                                                                                                                                                                                                                                                                                                               |

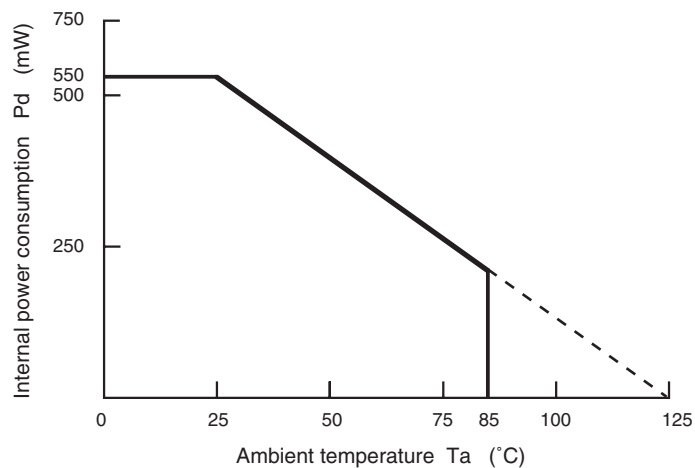
## Absolute Maximum Ratings

(Unless otherwise specified, Ta = 25°C)

| Pin no.   | Symbol           | Item                       | Test conditions | Ratings      | Unit |
|-----------|------------------|----------------------------|-----------------|--------------|------|
| [13]      | V <sub>B</sub>   | Power supply voltage       |                 | −0.3 to 36   | V    |
| [13]      | V <sub>B</sub>   | Power supply surge voltage | t ≤ 200 ms      | −0.3 to 36.5 | V    |
| [14]      | I <sub>B</sub>   | Bias current               |                 | 30           | mA   |
| [6], [11] | V <sub>OUT</sub> | Output voltage             |                 | −0.3 to 36   | V    |
| [6], [11] | I <sub>OUT</sub> | Output current             |                 | 10           | mA   |
| [8], [10] | V <sub>IN</sub>  | Input voltage              |                 | −0.3 to 16   | V    |
| [8], [10] | I <sub>IN</sub>  | Input current              |                 | −2.0 to 2.0  | mA   |
|           | Pd               | Power dissipation          | Ta = 25°C       | 550          | mW   |
|           | Topr             | Operating temperature      |                 | −40 to +85   | °C   |
|           | Tstg             | Storage temperature        |                 | −55 to +125  | °C   |

Note: All voltages are relative to the IC GND pin voltage (0 V). All current directions are positive when flowing into the IC (unmarked, or marked with a +), and are negative when flowing out (marked −).

## Thermal Reduction Rate Curve (Maximum Rating)



## Recommended Operating Conditions

(Unless otherwise specified, Ta = −40 to +85°C)

| Pin No.   | Symbol           | Item                        | Conditions | Ratings             | Unit |
|-----------|------------------|-----------------------------|------------|---------------------|------|
| [13]      | V <sub>B</sub>   | Power supply voltage        |            | 6 to 16             | V    |
| [1]       | V <sub>O</sub>   | Output power supply voltage |            | 4.5 to 5.5          | V    |
| [8], [10] | V <sub>IN</sub>  | Input voltage               |            | 0 to V <sub>O</sub> | V    |
| [8], [10] | V <sub>OUT</sub> | Output voltage              |            | 0 to V <sub>O</sub> | V    |

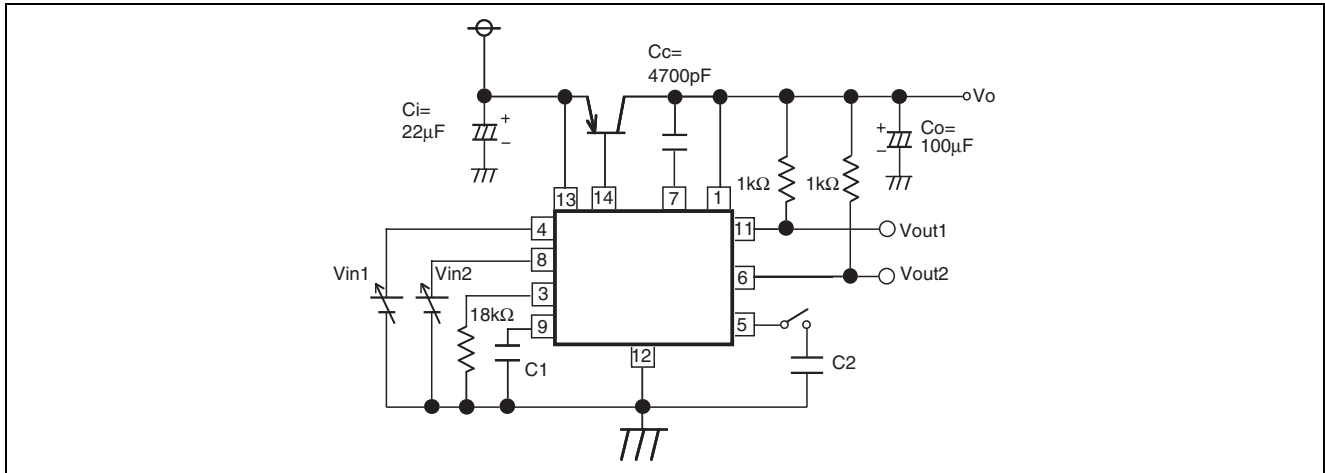
## Electrical Characteristics

(Unless otherwise specified, Ta = -40 to +85°C, Io = 50 mA, Ci = 22 µF, Co = 100 µF, C1 = 0.47 µF, Cc = 4700 pF, RIAdj = 18 kΩ)

| Symbol | Item                                          | Measurement conditions    | Units |       |       | Unit |
|--------|-----------------------------------------------|---------------------------|-------|-------|-------|------|
|        |                                               |                           | min.  | typ.  | max.  |      |
| IB     | Bias current                                  | Note1                     | —     | 9     | 20    | mA   |
| VO     | Output voltage                                | Steady-state              | 4.75  | 5.0   | 5.25  | V    |
| VON    |                                               | VoAdj pin grounded        | 5.2   | 5.5   | 6.0   | V    |
| Reg-IN | Input stability                               | Vcc = 7 to 36 V           | —     | 0.1   | 0.2   | %/V  |
| Reg-L  | Load stability                                | Io = 1 to 500 mA          | —     | 40    | 200   | mV   |
| VREF   | Reference voltage                             |                           | 1.200 | 1.265 | 1.330 | V    |
| ΔVTH1  | Threshold voltage hysteresis                  | Note2: VTH1 set to 4.35 V | 20    | 50    | 100   | mV   |
| IVREF  | VREF input current                            |                           | —     | —     | 10    | µA   |
| VsatH  | HALT output saturation voltage                | IHALT = 5 mA              | —     | 0.2   | 0.6   | V    |
| VsatR  | RESET output saturation voltage               | IRESET = 5 mA             | —     | 0.2   | 0.6   | V    |
| ILHAL  | HALT output leakage current                   | VHALT = 5 V               | —     | —     | 10    | µA   |
| ILR    | RESET output leakage current                  | VRESET = 5 V              | —     | —     | 10    | µA   |
| VL-EN  | ENL input voltage                             |                           | —     | —     | 0.6   | V    |
| IL-EN  | ENL input current                             | VIN – EN = 0 V            | —     | –250  | –500  | µA   |
| IIN-P  | P-RUN input current                           | VIN – P = 5 V             | 100   | 200   | 400   | µA   |
| VIN-PH | P-RUN H input voltage                         |                           | 2.5   | —     | —     | V    |
| VIN-PL | P-RUN L input voltage                         |                           | —     | —     | 0.3   | V    |
| T1(RW) | Watchdog reset pulse width                    | C1 = 0.22 µF              | 0.23  | 0.46  | 0.69  | ms   |
|        |                                               | C1 = 0.47 µF              | 0.5   | 1     | 1.5   | ms   |
| T2(RW) | Watchdog time (reset pulse interval)          | C1 = 0.22 µF              | 7.3   | 14.6  | 21.9  | ms   |
|        |                                               | C1 = 0.47 µF              | 15    | 30    | 45    | ms   |
| T3(R)  | RESET output delay time (power-on reset time) | C1 = 0.22 µF              | 14.6  | 29.2  | 44.0  | ms   |
|        |                                               | C1 = 0.47 µF              | 30    | 60    | 90    | ms   |
| T4(R)  | RESET output delay time                       |                           | 75    | 200   | 450   | µA   |
| T5(H)  | HALT output delay time                        |                           | 150   | 400   | 900   | µA   |
| T6(H)  | HALT output delay time                        | C2: open                  | 3     | 10    | 25    | µA   |
|        |                                               | C2 = 4700 pF±10%          | 1     | 2     | 3     | ms   |
| VB-MIN | VB minimum operating voltage                  | Note3, Ta = 25°C          | —     | —     | 2.0   | V    |
| VO-MIN | Vo minimum operating voltage                  | Note4, Ta = 25°C          | —     | 0.8   | 1.0   | V    |
| ID     | Driving current                               | Note5, Ta = 40 to 85°C    | 8     | —     | —     | mA   |

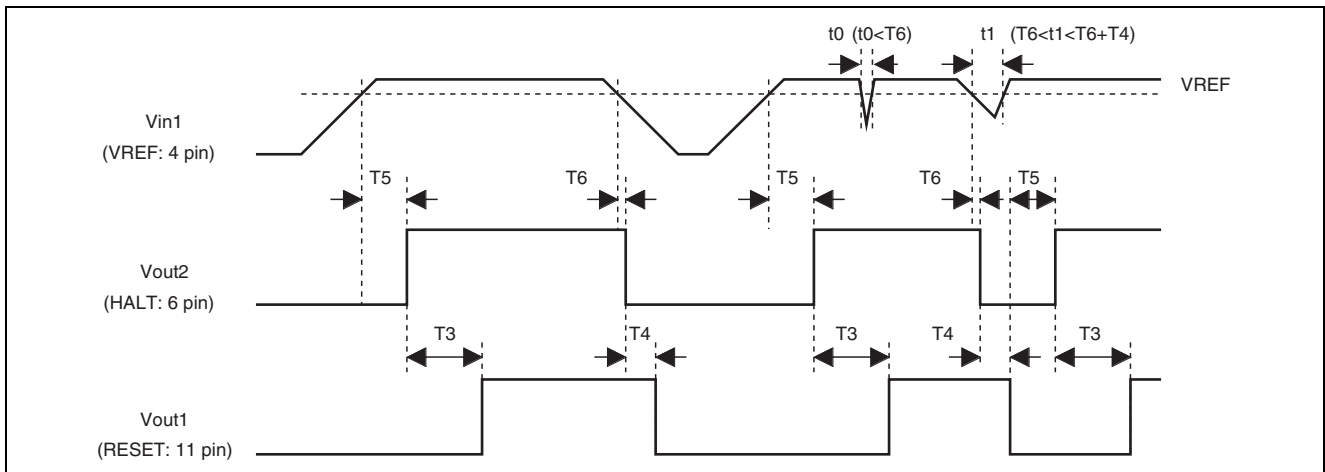
- Notes: 1. The bias current IB is the sum of all currents flowing into the pins [1], [7], [13], [14].  
 2. VTH1 is the threshold voltage relative to VREF, and is set using an external resistance.  
 3. The minimum operating voltage of VB for the operation of various functions  
 4. The minimum operating voltage Vo at which the HALT output and RESET output can be held at L (when the HALT and RESET output pull-up resistance is 1 kΩ)  
 5. B (pin [14]) driving current capacity

## Power Supply Monitoring/Watchdog Timer Timing Diagram



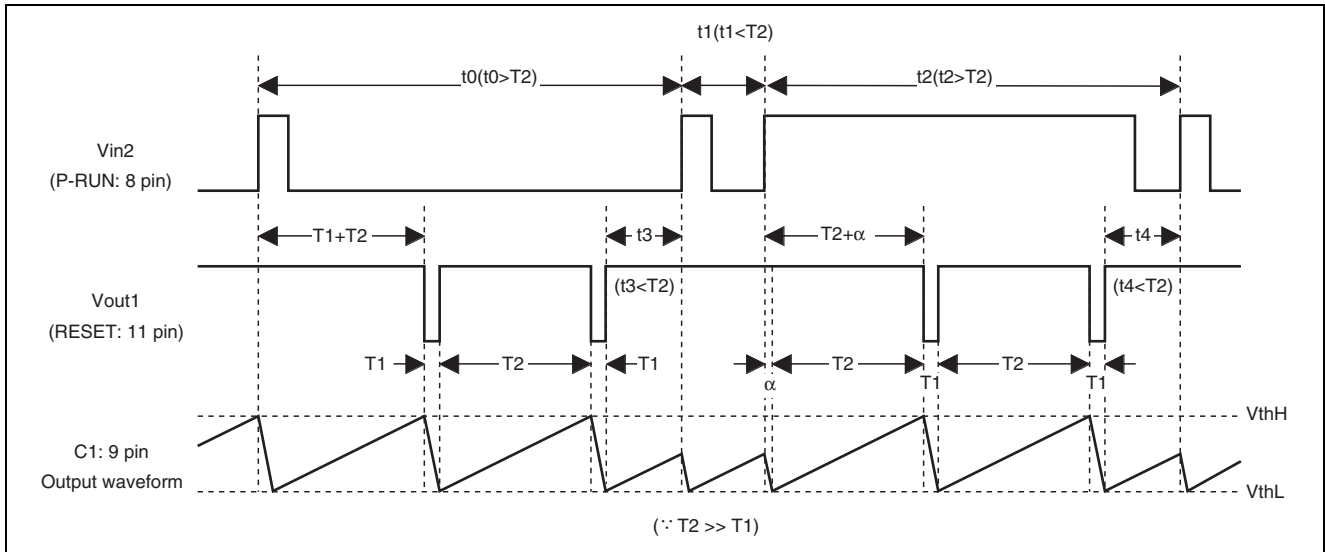
## Power Supply Monitor Timing Diagram

(When a normal pulse is input to P-RUN (pin [8]))

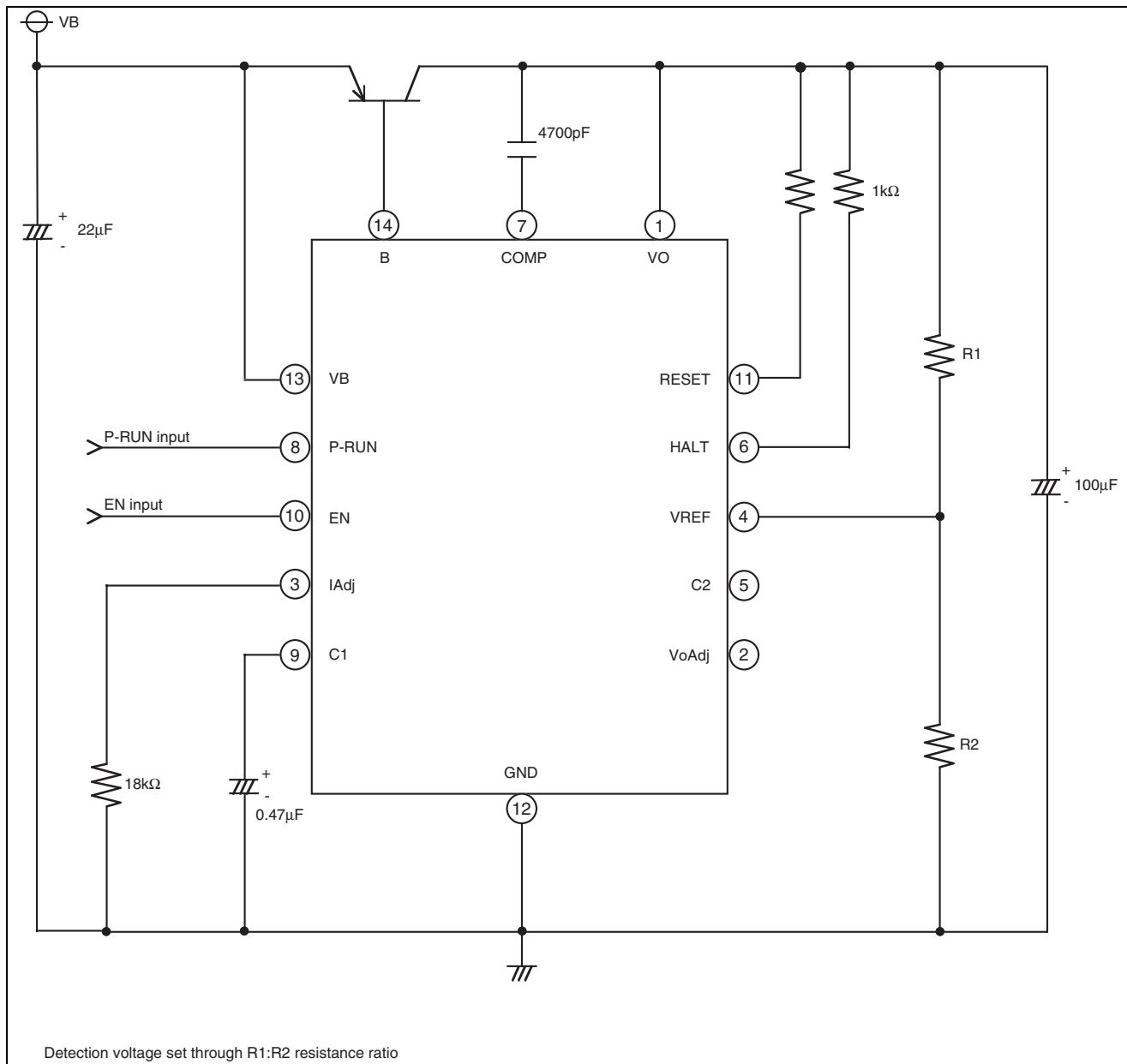


## Watchdog Timer Timing Chart (H input to Vin1 (pin [4], VREF))

(When "L" is input to pin [10] (EN), watchdog function halted)



## Application Example



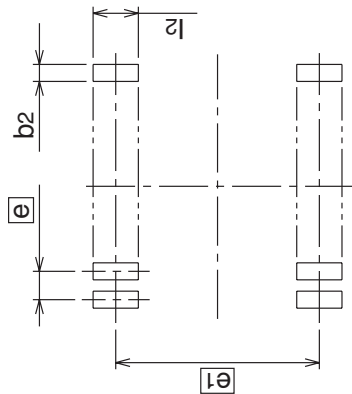
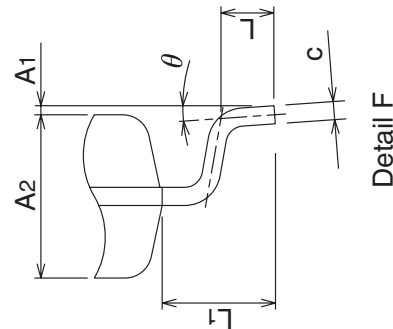
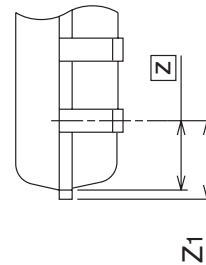
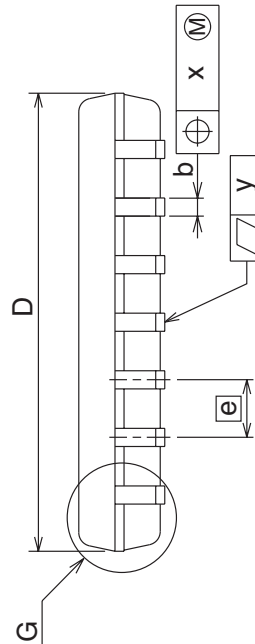
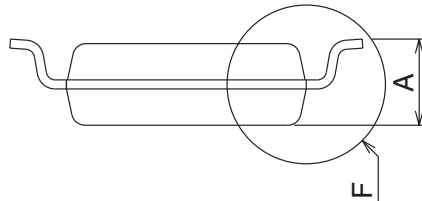
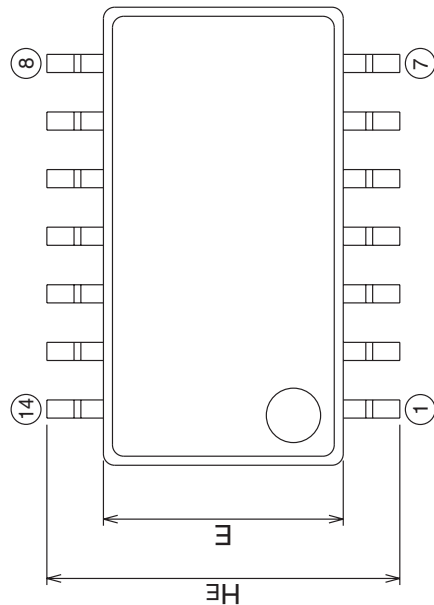
Package Dimensions

14P2N-A

(MMP)

Plastic 14pin 300mil SOP

| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
|-------------------|------------|-----------|---------------|
| SOP14-P-300-1.27  | —          | 0.2       | Cu Alloy      |



Recommended Mount Pad

| Symbol | Dimension in Millimeters |      |      |
|--------|--------------------------|------|------|
|        | Min                      | Nom  | Max  |
| A      | —                        | —    | 2.1  |
| A1     | 0                        | 0.1  | 0.2  |
| A2     | —                        | 1.8  | —    |
| b      | 0.35                     | 0.4  | 0.5  |
| c      | 0.18                     | 0.2  | 0.25 |
| D      | 10.0                     | 10.1 | 10.2 |
| E      | 5.2                      | 5.3  | 5.4  |
| e      | —                        | 1.27 | —    |
| HE     | 7.5                      | 7.8  | 8.1  |
| L      | 0.4                      | 0.6  | 0.8  |
| L1     | —                        | 1.25 | —    |
| Z      | —                        | 1.24 | —    |
| Z1     | —                        | —    | 1.39 |
| x      | —                        | —    | 0.25 |
| y      | —                        | —    | 0.1  |
| θ      | 0°                       | —    | 8°   |
| b2     | —                        | 0.76 | —    |
| el     | —                        | 7.62 | —    |
| l2     | 1.27                     | —    | —    |

## Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.  
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



### RENESAS SALES OFFICES

<http://www.renesas.com>

**Renesas Technology America, Inc.**  
450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited.**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom  
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

**Renesas Technology Europe GmbH**  
Dornacher Str. 3, D-85622 Feldkirchen, Germany  
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

**Renesas Technology Hong Kong Ltd.**  
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2375-6836

**Renesas Technology Taiwan Co., Ltd.**  
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology (Shanghai) Co., Ltd.**  
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China  
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

**Renesas Technology Singapore Pte. Ltd.**  
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001