Document Title

4Bank x 1M x 16bits Synchronous DRAM

Revision History

Revision No.	History	Draft Date	Remark
1.0	First Version Release	Nov. 2004	
	1. Changed tOH: 2.0 --> 2.5 [tCK = 7 & 7.5 (CL3) Product]		
1.1	1. Changed Input High/Low Voltage (Page 08) 2. Changed DC characteristics (Page 09) - IDD2NS: 18mA -> 15mA - IDD5:210 / 195 / 180mA -> 170 / 160 / 150mA [Speed 200 / 166 / 143 / 133MHz] 3. Changed Clock High / Low pulse width Time (Page 11) 4. Changed tAC Time (Page11) 5. Changed tRRD Time (Page12)	Dec. 2004	
1.2	1. Corrected Revision No.: 2.0 -> 1.1 2. Deleted Remark at Revision History 3. Corrected AC OPERATING CONDITION - CL 50pF -> 30pF 4. Changed DC OPERATING CONDITION - VIH MAX VDDQ+2.0 -> VDDQ+0.3 and Typ 3.3 -> 3.0 - VIL MIN VSSQ-2.0 -> -0.3	Dec. 2004	
1.3	1. Modified note for Super Low Power in ORDERING INFORMATION	Jan. 2005	
1.4	1. Corrected PIN ASSIGNMENT A12 to NC	Jan. 2005	
1.5	1. Corrected comments for overshoot and undershoot	Feb. 2005	

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DESCRIPTION

The Hynix HY57V641620E(L/S)T(P) series is a 67,108,864bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY57V641620E(L/S)T(P) is organized as 4banks of 1,048,576x16.

HY57V641620E(L/S)T(P) is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a '2N' rule)

FEATURES

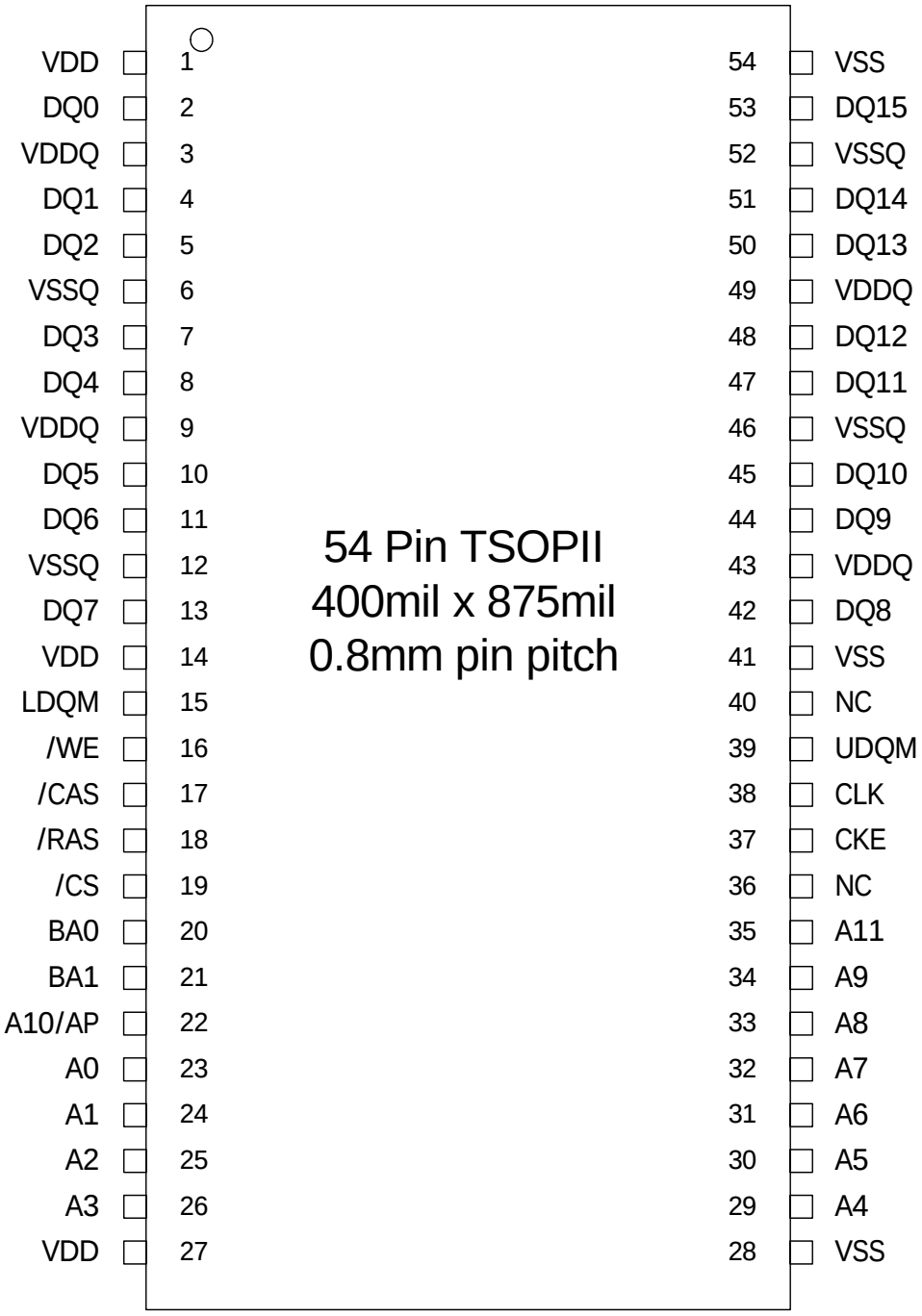
- Voltage: VDD, VDDQ 3.3V supply voltage
- All device pins are compatible with LVTTL interface
- 54 Pin TSOPII (Lead or Lead Free Package)
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM, LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 Refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency; 2, 3 Clocks
- Burst Read Single Write operation

ORDERING INFORMATION

Part No.	Clock Frequency	Organization	Interface	Package
HY57V641620E(L/S)T(P)-5	200MHz	4Banks x 1Mbits x16	LVTTL	54 Pin TSOPII
HY57V641620E(L/S)T(P)-6	166MHz			
HY57V641620E(L/S)T(P)-7	143MHz			
HY57V641620E(L/S)T(P)-H	133MHz			

Note: 1. HY57V641620ET Series: Normal power, Leaded.
2. HY57V641620ELT Series: Low power, Leaded.
3. HY57V641620EST Series: Super Low power, Leaded.
4. HY57V641620ETP Series: Normal power, Lead Free.
5. HY57V641620ELTP Series: Low power, Lead Free.
6. HY57V641620ESTP Series: Super Low Power, Lead Free

PIN ASSIGNMENTS

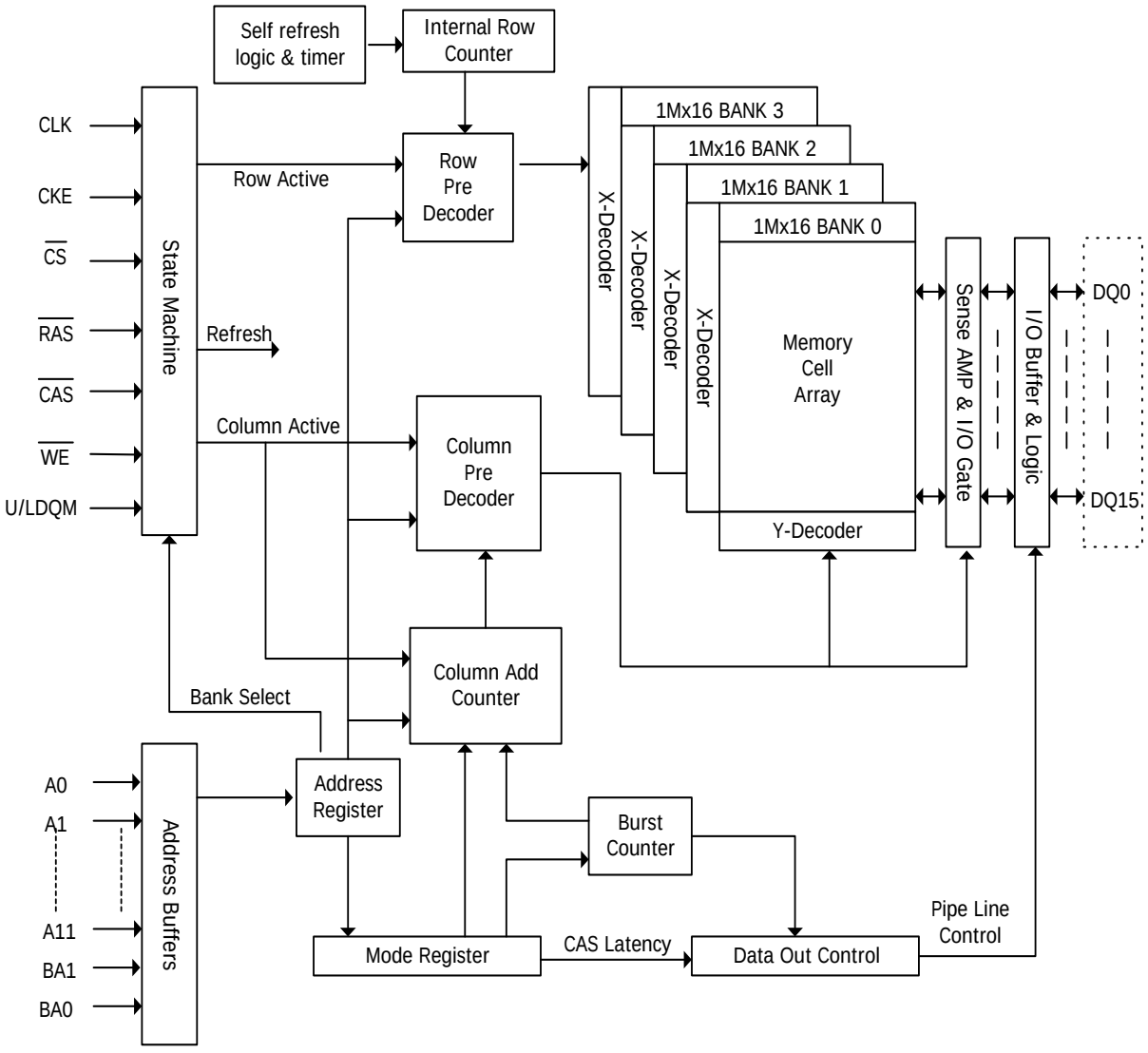


PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE, UDQM and LDQM
BA0, BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address: RA0 ~ RA11, Column Address: CA0 ~ CA7 Auto-precharge flag: A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
UDQM, LDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input / Output	Multiplexed data input / output pin
VDD / VSS	Power Supply / Ground	Power supply for internal circuits and input buffers
VDDQ / VSSQ	Data Output Power / Ground	Power supply for output buffers
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

1Mbit x 4banks x 16 I/O Synchronous DRAM



BASIC FUNCTIONAL DESCRIPTION

Mode Register

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	OP Code	0	0	CAS Latency			BT	Burst Length		

OP Code

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature / Time	TSOLDER	260 / 10	°C / Sec

DC OPERATING CONDITION (TA= 0 to 70°C)

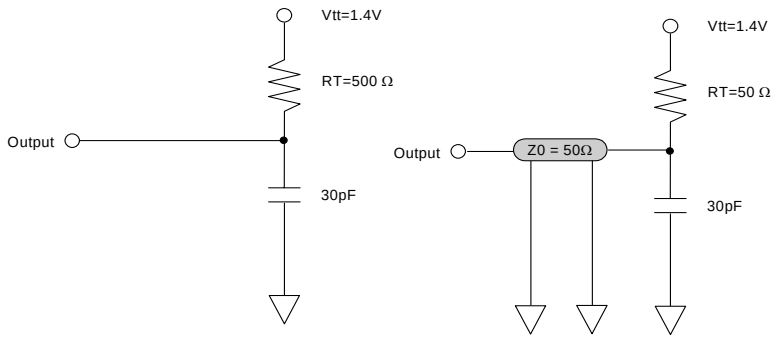
Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High Voltage	VIH	2.0	3.0	VDDQ + 0.3	V	1, 2
Input Low Voltage	VIL	-0.3	-	0.8	V	1, 3

Note: 1. All voltages are referenced to VSS = 0V
2. VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
3. VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration.

AC OPERATING TEST CONDITION (TA= 0 to 70 °C, VDD=3.3±0.3V, VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	VIH / VIL	2.4 / 0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	30	pF	1

Note: 1.



DC Output Load Circuit AC Output Load Circuit

CAPACITANCE (T_A= 0 to 70 °C, f=1MHz, V_{DD}=3.3V)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	CI1	2.0	4.0	pF
	A0 ~ A11, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, LDQM, UDQM	CI2	2.5	5.0	pF
Data input / output capacitance	DQ0 ~ DQ15	CI/O	3.0	5.5	pF

DC CHARACTERRISTICS I (T_A= 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	IOH = -4mA
Output Low Voltage	VOL	-	0.4	V	IOL = +4mA

Note: 1. V_{IN} = 0 to 3.3V, All other balls are not tested under V_{IN} =0V
2. D_{OUT} is disabled, V_{OUT}=0 to 3.6

DC CHARACTERISTICS II (TA= 0 to 70°C)

Parameter	Symbol	Test Condition		Speed				Unit	Note
				5	6	7	H		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA		120	110	100	100	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns		2				mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		2				mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		18				mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		15					
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns		3				mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		3					
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		40				mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		35					
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active		120	110	100	100	mA	1
Auto Refresh Current	IDD5	tRC ≥ tRC(min), All banks active		170	160	150	150	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V	Normal	1				mA	3
			Low power	400				uA	
			Super Low power	300				uA	3, 4

Note: 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRRC (Refresh $\overline{RAS}$ cycle time) is shown at AC CHARACTERISTICS II
3. HY57V641620ET(P) Series: Normal Power
HY57V641620ELT(P) Series: Low Power
HY57V641620EST(P) Series: Super Low Power

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	5		6		7		H		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CL = 3	tCK3	5.0	1000	6.0	1000	7.0	1000	7.5	1000	ns	
	CL = 2	tCK2	10		10		10		10		ns	
Clock High Pulse Width		tCHW	1.75	-	2.0	-	2.0	-	2.5	-	ns	1
Clock Low Pulse Width		tCLW	1.75	-	2.0	-	2.0	-	2.5	-	ns	1
Access Time From Clock	CL = 3	tAC3	-	4.5	-	5.4	-	5.4	-	5.4	ns	2
	CL = 2	tAC2	-	6.0	-	6.0	-	6.0	-	6.0	ns	
Data-out Hold Time		tOH	2.0	-	2.0	-	2.5	-	2.5	-	ns	
Data-Input Setup Time		tDS	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
Data-Input Hold Time		tDH	0.8	-	0.8	-	0.8	-	0.8	-	ns	1
Address Setup Time		tAS	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
Address Hold Time		tAH	0.8	-	0.8	-	0.8	-	0.8	-	ns	1
CKE Setup Time		tCKS	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
CKE Hold Time		tCKH	0.8	-	0.8	-	0.8	-	0.8	-	ns	1
Command Setup Time		tCS	1.5	-	1.5	-	1.5	-	1.5	-	ns	1
Command Hold Time		tCH	0.8	-	0.8	-	0.8	-	0.8	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1.0	-	1.0	-	1.5	-	1.5	-	ns	
CLK to Data Output in High-Z Time	CL = 3	tOHZ3	-	4.5	-	5.4	-	5.4	-	5.4	ns	
	CL = 2	tOHZ2	-	6.0	-	6.0	-	6.0	-	6.0	ns	

Note: 1. Assume t_R / t_F (input rise and fall time) is 1ns. If t_R & t_F > 1ns, then [(t_R+t_F)/2-1]ns should be added to the parameter.
2. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 0.2V. If t_R > 1ns, then (t_R/2-0.5)ns should be added to the parameter.

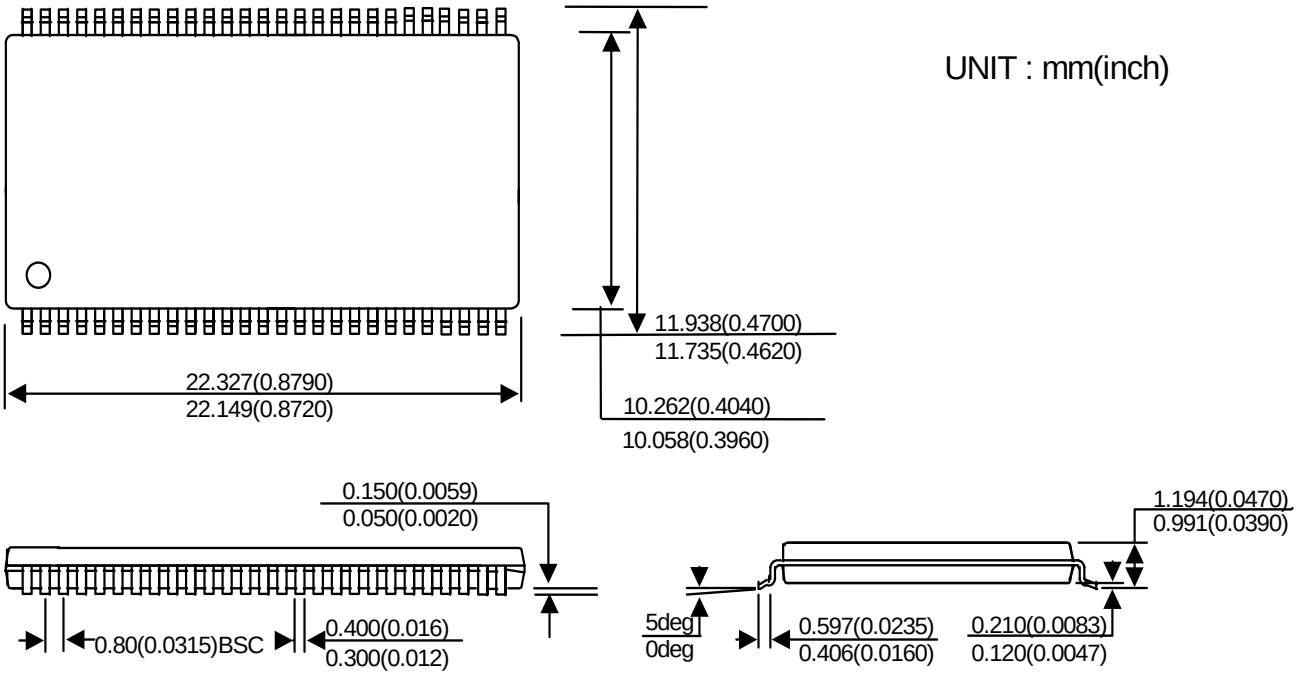
AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Symbol	5		6		7		H		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	55	-	60	-	63	-	63	-	ns	
$\overline{RAS}$ Cycle Time	Auto Refresh	tRRC	55	-	60	-	63	-	63	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	15	-	18	-	20	-	20	-	ns	
$\overline{RAS}$ Active Time		tRAS	38.7	100K	42	100K	42	100K	42	120K	ns	
$\overline{RAS}$ Precharge Time		tRP	15	-	18	-	20	-	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	10	-	12	-	14	-	15	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	0	-	CLK	
Data-in to Precharge Command		tDPL	2	-	2	-	2	-	2	-	CLK	
Data-In to Active Command		tDAL	tDPL + tRP									
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	2	-	CLK	
Precharge to Data Output High-Z	CL = 3	tPROZ3	3	-	3	-	3	-	3	-	CLK	
	CL = 2	tPROZ2	2	-	2	-	2	-	2	-	CLK	
Power Down Exit Time		tDPE	1	-	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	-	64	ms	

Note: 1. A new command can be given tRRC after self refresh exit.

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autopre-charge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autopre-charge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Burst-Read-Single-WRITE		H	X	L	L	L	L	X	A9 ball High (Other balls OP code)			MRS Mode
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

PACKAGE INFORMATION

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