PLL frequency synthesizer TDA8735

FEATURES

- Complete 30 MHz single-chip tuning system
- Loop amplifier included
- 2-level current amplifier (charge pump) for adjusting the loop gain
- A powerful digital memory phase detector
- Programmable reference frequencies of 1 kHz, 10 kHz or 25 kHz
- I²C-bus interface
- Programmable address select input
- Software controlled switch output.

APPLICATIONS

- Satellite sound receiver
- Radio receiver: LW, MW and SW.

GENERAL DESCRIPTION

The TDA8735 is a single-chip PLL synthesizer designed for satellite receivers. The device can be set to two different addresses which can be used in applications where independently tuned VCOs are required.

To adapt to different frequency accuracy, 3 reference frequencies are selectable via the I²C-bus. The charge pump current can be set to 2 values with a ratio of 1 : 100 via the I²C-bus.

A programmable switch (open collector) is integrated to enable mode or normal switching, or other types of application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (pin 3)		4.5	5.0	5.5	V
V_{CC2}	supply voltage (pin 16)		V_{CC1}	8.5	12	V
I_{CC1}	supply current (pin 3)	outputs unloaded	12	20	28	mA
I_{CC2}	supply current (pin 16)	outputs unloaded	0.2	0.5	1	mA
$f_{i(max)}$	maximum input frequency		30	–	–	MHz
$f_{i(min)}$	minimum input frequency		–	–	512	kHz
$V_{i(rms)}$	input voltage (RMS value)		30	–	500	mV
P_{tot}	total power dissipation		–	0.14	–	W
T_{amb}	operating ambient temperature		−30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8735	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TDA8735T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

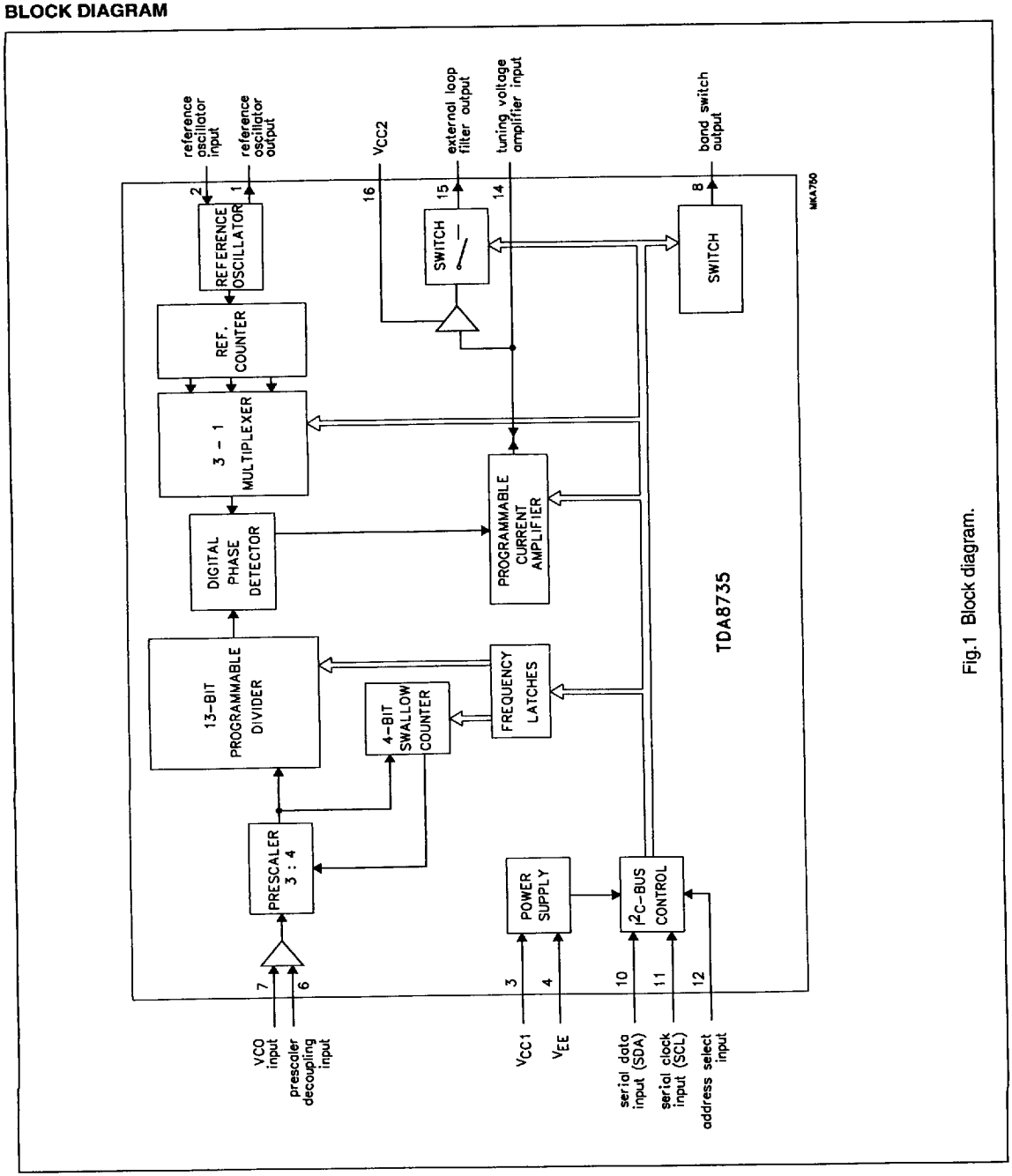


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XTAL1	1	reference oscillator output
XTAL2	2	reference oscillator input
V_{CC1}	3	supply voltage 1
V_{EE}	4	ground
n.c.	5	not connected
DEC	6	prescaler decoupling
VCOFI	7	VCO input frequency
BS	8	band switch output
n.c.	9	not connected
SDA	10	serial data input (I^2C-bus)
SCL	11	serial clock input (I^2C-bus)
AS	12	address select input (I^2C-bus)
n.c.	13	not connected
$LOOP_I$	14	tuning voltage amplifier input
$LOOP_O$	15	external loop filter output
V_{CC2}	16	supply voltage 2

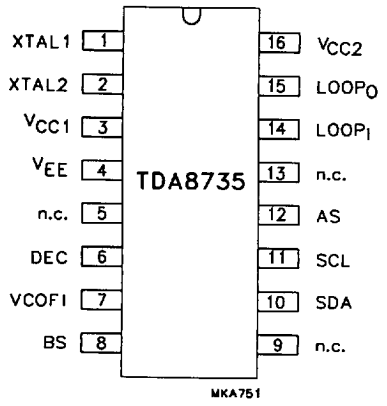


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8735 contains the following parts and facilities:

- Input amplifier VCO-signal.
- A prescaler with the divisors 3 : 4 and a 2-bit programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter; the reference frequency can be 1 kHz, 10 kHz or 25 kHz and is applied to the digital memory phase detector.
- An I^2C-bus interface with data latches and control logic; the I^2C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I^2C-bus specification is available on request.
- A software-controlled switch output.
- A programmable current amplifier (charge pump) which consists of a 5 μA and a 500 μA current source, this allows adjustment of loop gain, thus providing high-current high-speed tuning and low current-stable tuning. The output at the loop amplifier can deliver a tuning voltage of up to 10.5 V (V_{CC2} – 1.5 V).

Controls

The TDA8735 is controlled via the 2-wire I^2C-bus. As slave receiver for programming there is one module address, a logic 0 ($R/\overline{W}$ bit), a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address select input AS (pin 12) makes it possible to operate two TDA8735 in one system.

The auto increment facility of the I^2C-bus allows programming of the TDA8735 within one transmission (address + subaddress + 4 data bytes).

The TDA8735 can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is illustrated in Fig.3 and is described below.

The divider number is defined by 15-bit words, bits S0 to S14. To calculate the lock frequency, the divider number has to be multiplied by the selected reference frequency.

Table 1 Divider number setting.

$\overline{ON}$	DIVIDER NUMBER SETTING	INPUT
0	$(S0 + S1) \times 2^1 .... + S13 \times 2^{13} + S14 \times 2^{14}$	ON

Where the minimum divider ratio is: $2^6 = 64$ to $2^{15} - 1 = 32761$.

Table 2 Bit CP (used to control the charge pump; DB0: D0).

CP	CURRENT
0	LOW
1	HIGH

Table 3 Bits REF1 and REF2 (used to set the reference frequency applied to the phase detector; DB2: D7 and D6).

REF1	REF2	FREQUENCY (kHz)
0	0	1
0	1	10
1	0	25
1	1	0

Table 4 Bit OPAMP (used to control the switch in the tuning voltage amplifier output circuitry; DB2: D4).

OPAMP	SWITCH
1	on
0	off

Table 5 Bit BS (used to control the open-collector switch output; DB2: D2).

BS	SWITCH OUTPUT
1	sink current
0	floating

The data byte DB3 must be set to 0....0. It is also used for test purposes (see Fig.3).

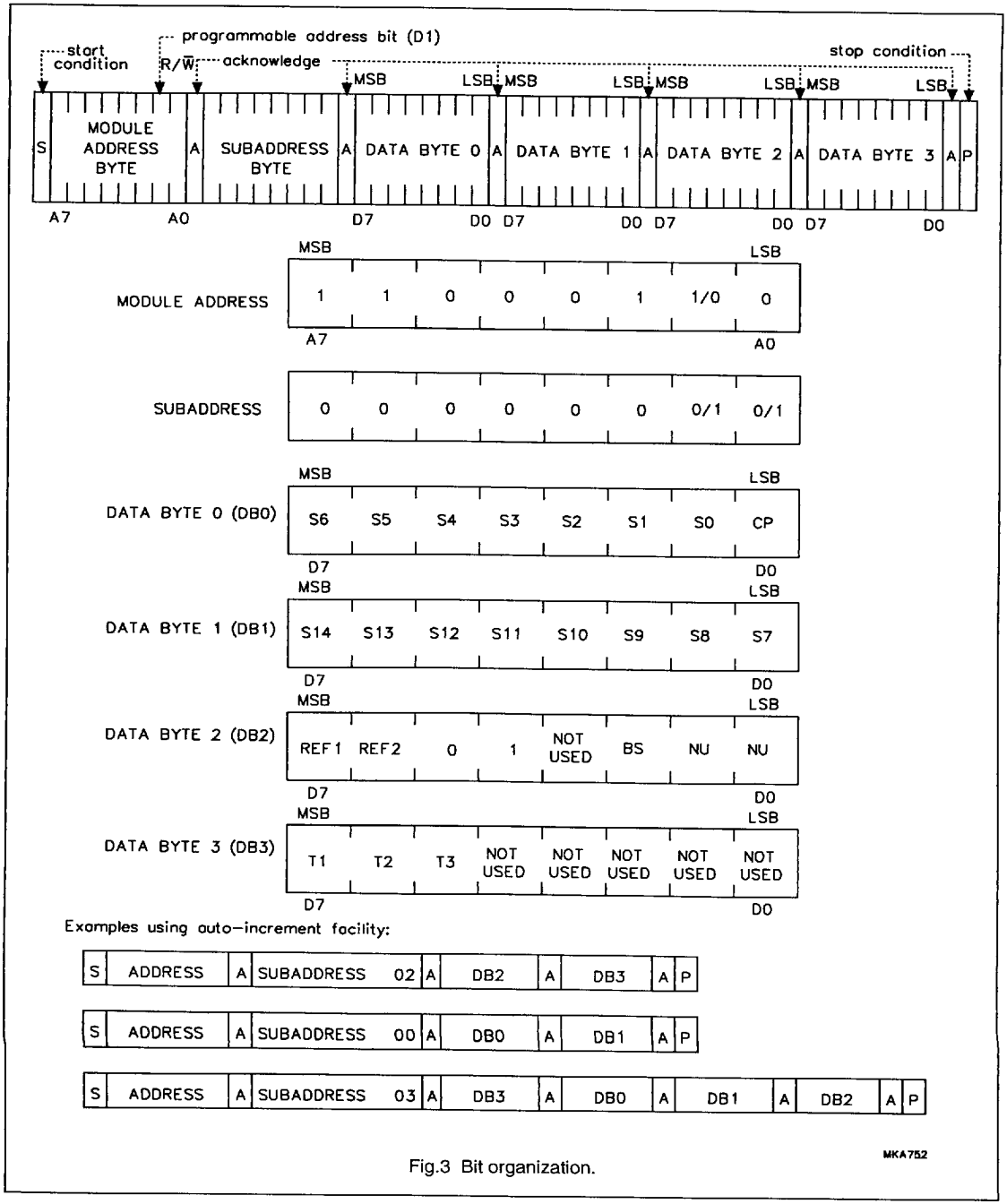


Fig.3 Bit organization.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC1}	supply voltage (pin 3)	−0.3	+5.5	V
V_{CC2}	supply voltage (pin 16)	V_{CC1}	12.5	V
P_{tot}	total power dissipation	–	0.85	W
T_{amb}	operating ambient temperature	−30	+85	°C
T_{stg}	storage temperature	−65	+150	°C

HANDLING

Every pin withstands the ESD test in accordance with *"MIL-STD-883C category B"* (2000 V).

CHARACTERISTICS

V_{CC1} = 5 V; V_{CC2} = 8.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC1}	supply voltage (pin 3)		4.5	5.0	5.5	V
V_{CC2}	supply voltage (pin 16)		V_{CC1}	8.5	12	V
I_{CC1}	supply current (pin 3)	no outputs loaded	12	20	28	mA
I_{CC2}	supply current (pin 16)	no outputs loaded	0.2	0.5	1	mA
		TDA8735T only	0.7	1	1.5	mA
I²C-bus inputs (SDA and SCL)						
V_{IH}	HIGH level input voltage		3.0	–	5.0	V
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
I_{IH}	HIGH level input current		–	–	10	µA
I_{IL}	LOW level input current		–	–	10	µA
SDA output						
V_{OL}	LOW level output voltage	open collector; I_{OL} = 3.0 mA	–	–	0.4	V
AS input						
V_{IH}	HIGH level input voltage	AS = C6	3.0	–	5.0	V
V_{IL}	LOW level input voltage	AS = C4	−0.3	–	+1.0	V
I_{IH}	HIGH level input current		–	–	10	µA
I_{IL}	LOW level input current		–	–	10	µA
RF input						
$f_{i(max)}$	maximum input frequency		30	–	–	MHz
$f_{i(min)}$	minimum input frequency		–	–	512	kHz
$V_{i(rms)}$	input voltage (RMS value)	measured in Fig.4	30	–	500	mV
R_i	input resistance		–	5.9	–	kΩ
C_i	input capacitance		–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator (XTAL1 and XTAL2)						
R_{xtal}	crystal resonance resistance (4 MHz)	see Fig.5	–	–	150	Ω
Programmable charge pump						
I_{CHP}	output current to loop filter	bit CP = logic 0	3	5	7	µA
		bit CP = logic 1	400	500	600	µA
		bit CP = logic 0; TDA8735T only	3	5	9	µA
Ripple rejection						
RR	$20 \log \frac{\Delta V_{CC1}}{\Delta V_O}$	f_{ripple} = 100 Hz	40	50	–	dB
	$20 \log \frac{\Delta V_{CC2}}{\Delta V_O}$	f_{ripple} = 100 Hz	40	50	–	dB
Band switch output (pin 8)						
V_{OH}	HIGH level output voltage		–	–	12	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.8	V
$\|I_{LO}\|$	output leakage current	V_{OH} = 12 V	–	–	10	µA
Tuning voltage amplifier output (pin 15)						
$V_{O(max)}$	maximum output voltage	I_{source} = 0.5 mA	V_{CC2} – 1.5	–	–	V
$V_{O(min)}$	minimum output voltage	I_{sink} = 1 mA	–	–	0.8	V
I_{source}	maximum output source current		0.5	–	–	mA
I_{sink}	maximum output sink current		1.0	–	–	mA
$Z_{o(off)}$	impedance of switched-off output		5	–	–	MΩ
$\|I_{bias}\|$	input bias current (absolute value)		–	1	5	nA

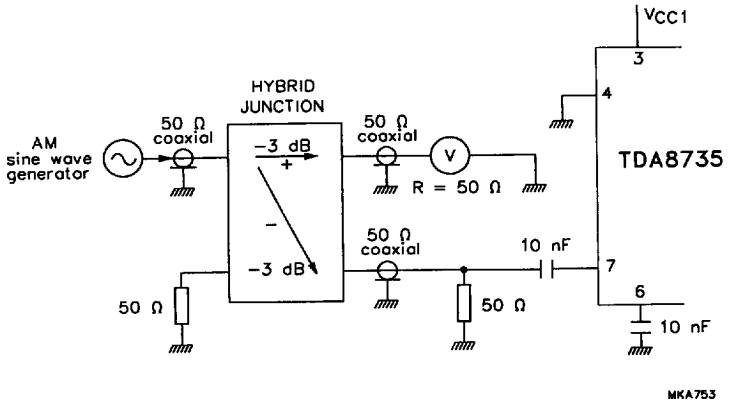


Fig.4 Prescaler input sensitivity (set-up measurement).

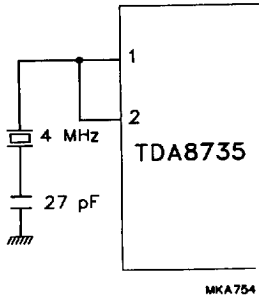
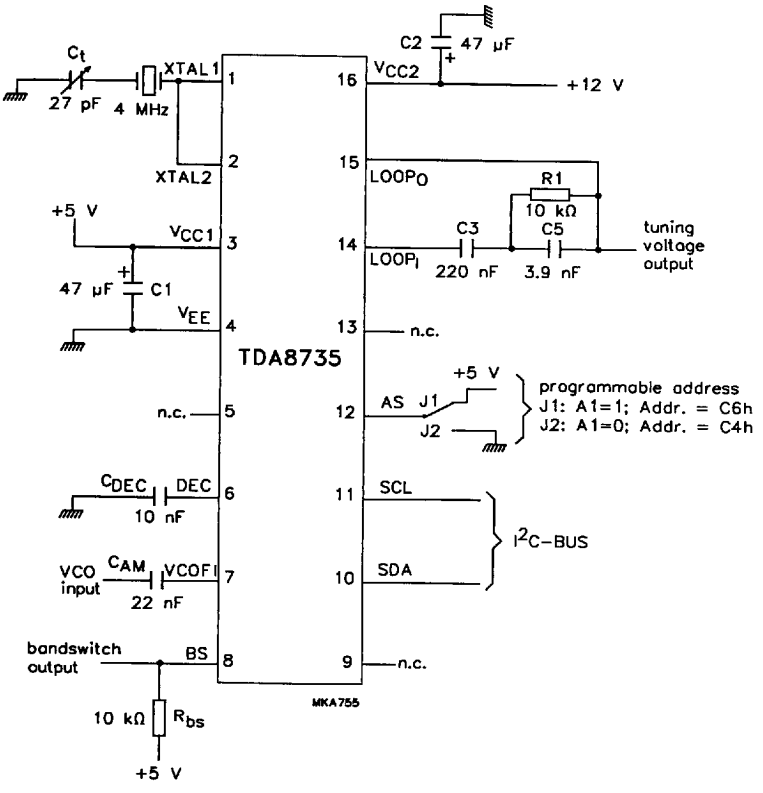


Fig.5 Crystal connection (4 MHz).

APPLICATION INFORMATION



Loop filter depends on VCO parameters.

Fig.6 Application example.