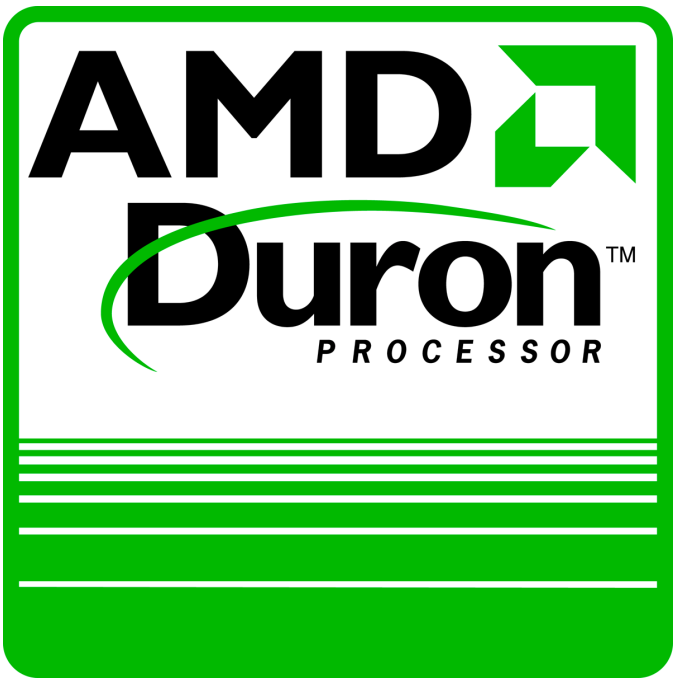
Preliminary Information

AMD Duron™

Processor Model 3
Data Sheet



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Revision History

Date	Rev	Description
June 2001	I	This revision includes added information about the 950 MHz AMD Duron™ Processor Model 3 and the following changes: ■ In Chapter 4, included APIC information in "Halt State" on page 10 and "Stop Grant States" on page 10 ■ In Chapter 5, updated Table 1, "Thermal Design Power," on page 19 ■ In Chapter 7, updated Table 8, "VCC_CORE Voltage and Current," on page 27 ■ In Chapter 10, revised description of "FERR Pin" on page 63 and Table 17 on page 54
April 2001	H	This revision includes added information about the 900 MHz AMD Duron™ Processor Model 3 and changes since January 2001 as follows: ■ In Chapter 4, revised Figure 3, "AMD Duron™ Processor Model 3 Power Management States" on page 9 ■ In Chapter 5, updated Table 1, "Thermal Design Power," on page 19 ■ In Chapter 7, revised Table 3, "VID[4:0] DC Characteristics," on page 24, Table 4, "FID[3:0] DC Characteristics," on page 24, Table 11, "AMD Duron™ System Bus DC Characteristics," on page 30, Table 14, "APIC Pins AC and DC Characteristics," on page 34, and updated Table 8, "VCC_CORE Voltage and Current," on page 27 ■ In Chapter 8, revised description of "Serial Initialization Packet (SIP) Protocol" on page 38 ■ In Chapter 9, added Table 15, "CPGA Mechanical Loading," on page 39 ■ In Chapter 10, revised description of "VID[4:0] Pins" on page 67, revised Table 16, "Pin Name Abbreviations," on page 48 , revised description of "AMD Pin" on page 62, and added description of "APIC Pins, PICCLK, PICD[1:0]#" on page 62
January 2001	G	Added information about the 850 MHz AMD Duron™ Processor Model 3 as follows: ■ Table 1, "Thermal Design Power," on page 19 ■ Table 6, "Operating Ranges," on page 25 ■ Table 8, "VCC_CORE Voltage and Current," on page 27 ■ Table 10, "SYSCLK and SYSCLK# AC Characteristics," on page 29 Added Chapter 6, "CPUID Support" on page 21 Revised Figure 16, "OPN Example for the AMD Duron™ Processor Model 3" on page 69
October 2000	F	Revised VID[4:0] information in Table 3 on page 24 and "VID[4:0] Pins" on page 67

Date	Rev	Description
October 2000	E	Added information about the 800 MHz AMD Duron™ Processor Model 3 as follows: ■ Table 1, "Thermal Design Power," on page 19 ■ Table 6, "Operating Ranges," on page 25 ■ Table 8, "VCC_CORE Voltage and Current," on page 27 ■ Added AMD Athlon to the trademark list ■ Updated "Motherboard PGA Design Guide, order# 90009" with new document name of "Socket A Motherboard Design Guide, order# 24363" throughout book ■ Added SAI#[0] pin in location AJ29 to Figure 14, "AMD Duron™ Processor Model 3 Pin Diagram—Topside View" on page 46 ■ Added the AMD Pin (AH6) to Table 17, "Cross-Reference by Pin Location," on page 54 and to the pin descriptions Section 10.3 on page 62 ■ Revised all no connect (NC) pins on the pin grid array (PGA) as follows: ● Figure 14, "AMD Duron™ Processor Model 3 Pin Diagram—Topside View" on page 46 ● Table 16, "Pin Name Abbreviations," on page 48 ● Table 17, "Cross-Reference by Pin Location," on page 54 ■ Revised "K7CLKOUT and K7CLKOUT# Pins" description on page 65 ■ Updated the ordering information on page 69
September 2000	D	Added information about the 750 MHz AMD Duron™ Processor Model 3 processor as follows: ■ Table 1, "Thermal Design Power," on page 19 ■ Table 6, "Operating Ranges," on page 25 ■ Table 8, "VCC_CORE Voltage and Current," on page 27
August 2000	C	■ Added Table 1, "Thermal Design Power," on page 19 ■ Revised VCC_CORE to 1.6 in Table 7, "Operating Ranges," on page 24 ■ Revised and reorganized the AC and DC characteristics for SYSCLK and SYSCLK#. See Table 11, "SYSCLK and SYSCLK# AC Characteristics," on page 27, and Table 10, "SYSCLK and SYSCLK# DC Characteristics," on page 26 ■ Added Table 15, "Miscellaneous Pins AC and DC Characteristics" on page 30 ■ Revised mechanical drawings in Chapter 8, pages 38 - 40 ■ Made corrections and updates to Chapter 9, "Pin Descriptions", in particular Table 19, "Socket A Pin Cross-Reference by Pin Location," on page 51 ■ Revised OPN from 4 digits to 3 (i.e. *from* 0550=0550 MHz *to* 550 MHz) in Chapter 11, "Ordering Information" on page 69
June 2000	B	Initial public release

1 Overview

The AMD Duron™ Processor Model 3 enables an optimized PC solution for value-conscious business and home users by providing the capability and flexibility to meet their computing needs for both today and tomorrow.

The AMD Duron™ Processor Model 3 is the latest offering from AMD designed for the value segment of the market. The innovative design was developed to accommodate new and more advanced applications, meeting the requirements of today's most demanding value-conscious buyers without compromising their budget.

Delivered in a PGA package, the AMD Duron Processor Model 3 is the new AMD workhorse processor for value desktop systems, delivering the highest integer, floating-point and 3D multimedia performance for applications running on x86 system platforms. The AMD Duron Processor Model 3 provides value-conscious customers with access to advanced technology that allows their system investment to last for years to come. The AMD Duron Processor Model 3 is designed as a solid platform for surfing the Internet, digital entertainment, and personal creativity. In addition, it is engineered to enable superior business productivity by delivering an optimized combination of computing performance and value.

The AMD Duron Processor Model 3 features the seventh-generation microarchitecture with an integrated L2 cache, which supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The AMD Duron Processor Model 3 high-speed execution core includes multiple x86 instruction decoders, a dual-ported 128-Kbyte split level-one (L1) cache, a 64-Kbyte on-chip L2 cache, three independent integer pipelines, three address calculation pipelines, and a superscalar, fully pipelined, out-of-order, three-way floating-point engine. The floating-point engine is capable of delivering superior performance on numerically complex applications.

The AMD Duron Processor Model 3 microarchitecture incorporates enhanced 3DNow!™ technology, a high-performance cache architecture, and a 200-MHz, 1.6-Gigabyte per second system bus. The AMD Duron system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling, to provide the most powerful, scalable bus available for any x86 processor.

The AMD Duron Processor Model 3 is binary-compatible with existing x86 software and backwards compatible with applications optimized for MMX™ and 3DNow! instructions. Using a data format and single-instruction multiple-data (SIMD) operations based on the MMX instruction model, the AMD Duron Processor Model 3 can produce as many as four, 32-bit, single-precision floating-point results per clock cycle. The enhanced 3DNow! technology implemented in the AMD Duron Processor Model 3 includes new integer multimedia instructions and software-directed data movement instructions to deliver a superior performance to Celeron in multimedia and number-intensive applications.

1.1 AMD Duron™ Processor Model 3 Microarchitecture Summary

The following features summarize the AMD Duron Processor Model 3 microarchitecture:

- The industry's first nine-issue, superpipelined, superscalar x86 processor microarchitecture designed for high clock frequencies
- Multiple x86 instruction decoders
- Three out-of-order, superscalar, fully pipelined floating-point execution units, which execute all x87 (floating-point), MMX and 3DNow! instructions
- Three out-of-order, superscalar, pipelined integer units
- Three out-of-order, superscalar, pipelined address calculation units
- 72-entry instruction control unit
- Advanced dynamic branch prediction
- Enhanced 3DNow! technology with new instructions to enable improved integer math calculations for speech or video encoding and improved data movement for internet plug-ins and other streaming applications

- 200-MHz AMD Duron system bus (scalable beyond 400 MHz) enabling leading-edge system bandwidth for data movement-intensive applications
- High-performance cache architecture featuring an integrated 128-Kbyte L1 cache and a 16-way, on-chip 64-Kbyte L2 cache

The AMD Duron Processor Model 3 delivers superior system performance in a cost-effective, industry-standard form factor. The AMD Duron Processor Model 3 is compatible with motherboards based on AMD's Socket A. Figure 1 shows a typical AMD Duron Processor Model 3 system block diagram.

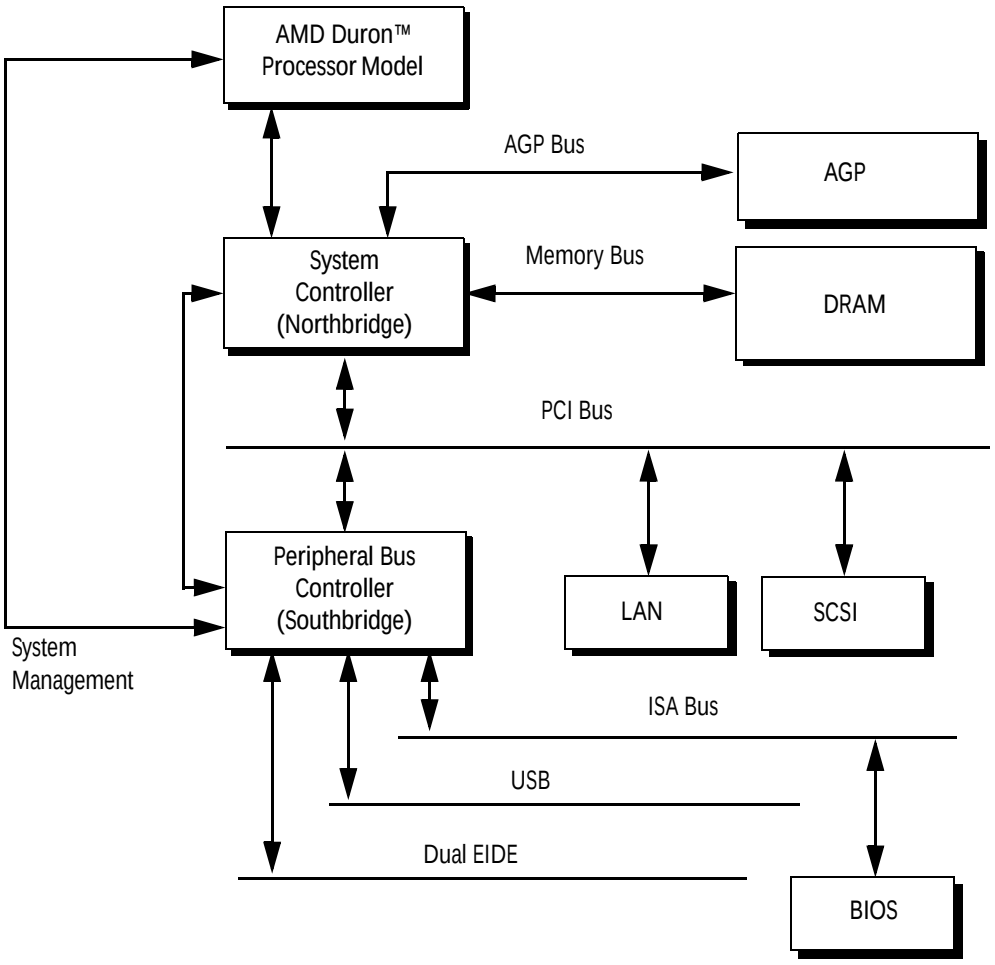


Figure 1. Typical AMD Duron™ Processor Model 3 System Block Diagram

2 Interface Signals

2.1 Overview

The AMD Duron system bus architecture is designed to deliver superior data movement bandwidth for value x86 platforms. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional probe channel, and a 72-bit bidirectional data channel, including 8-bit error code correction [ECC] protection), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use an impedance controlled push-pull low-voltage swing signaling technology contained within the Socket A socket. For more information, see "AMD Duron™ System Bus Signals" on page 6, Chapter 10, "Pin Descriptions" on page 45, and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

2.2 Signaling Technology

The AMD Duron system bus uses a low-voltage, swing signaling technology, which has been enhanced to provide larger noise margins, reduced ringing, and variable voltage levels. The signals are push-pull and impedance compensated. The signal inputs use differential receivers, which require a reference voltage (V_{REF}). The reference signal is used by the receivers to determine if a signal is asserted or deasserted by the source. Termination resistors are not needed because the driver is impedance matched to the motherboard and a high impedance reflection is used at the receiver to bring the signal past the input threshold.

For more information about pins and signals, see Chapter 10, "Pin Descriptions" on page 45.

2.3 Push-Pull (PP) Drivers

The Socket A AMD Duron™ Processor Model 3 supports Push-Pull (PP) drivers. The system logic configures the AMD Duron Processor Model 3 with the configuration parameter called SysPushPull (1=PP). The impedance of the PP drivers is set to match the impedance of the motherboard by two external resistors connected to the ZN and ZP pins. See "ZN, VCC_Z, ZP, and VSS_Z Pins" on page 68 for more information.

2.4 AMD Duron™ System Bus Signals

The AMD Duron system bus is a clock-forwarded, point-to-point interface with the following three point-to-point channels:

- A 13-bit unidirectional output address/command channel
- A 13-bit unidirectional input address/command channel
- 72-bit bidirectional data channel

For more information, see Chapter 7, "Electrical Data" on page 23 and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

3 Logic Symbol Diagram

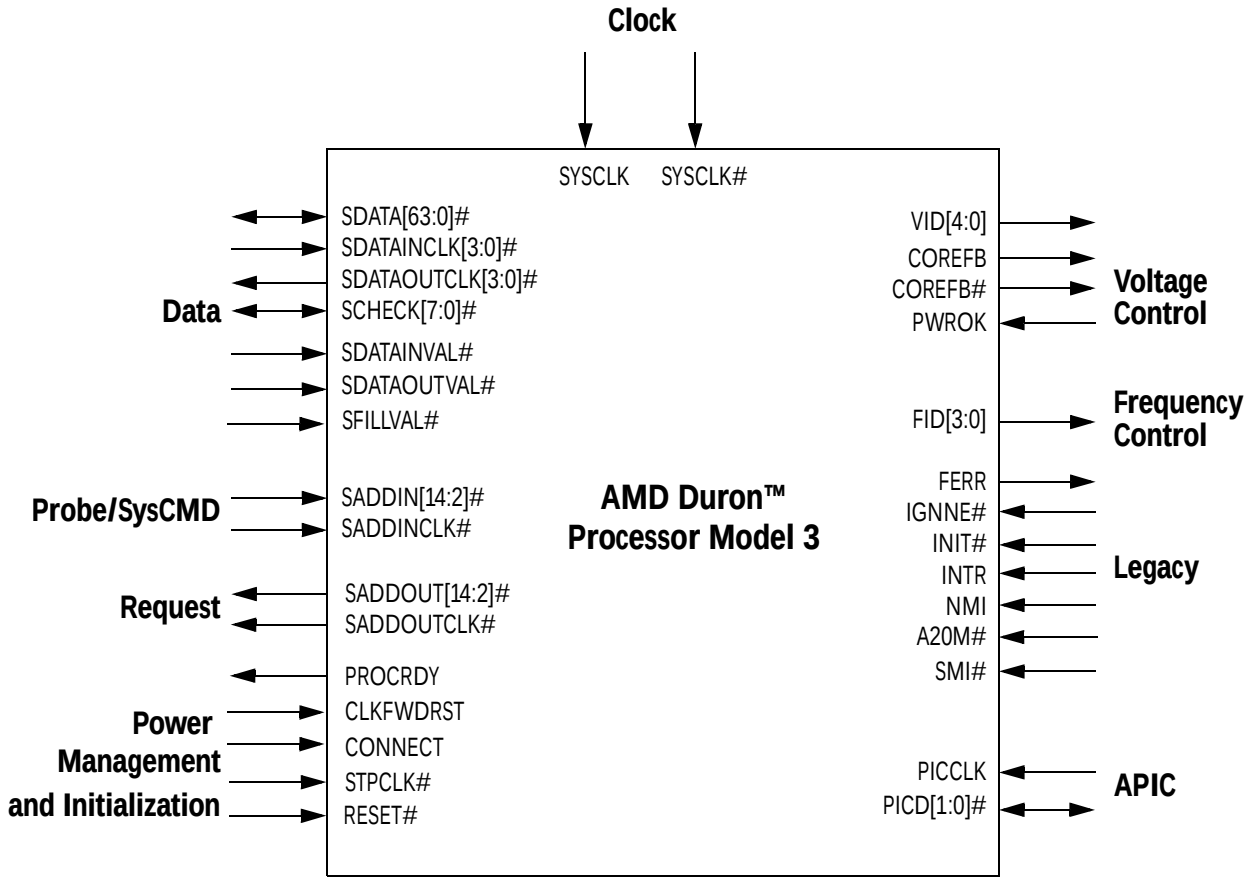
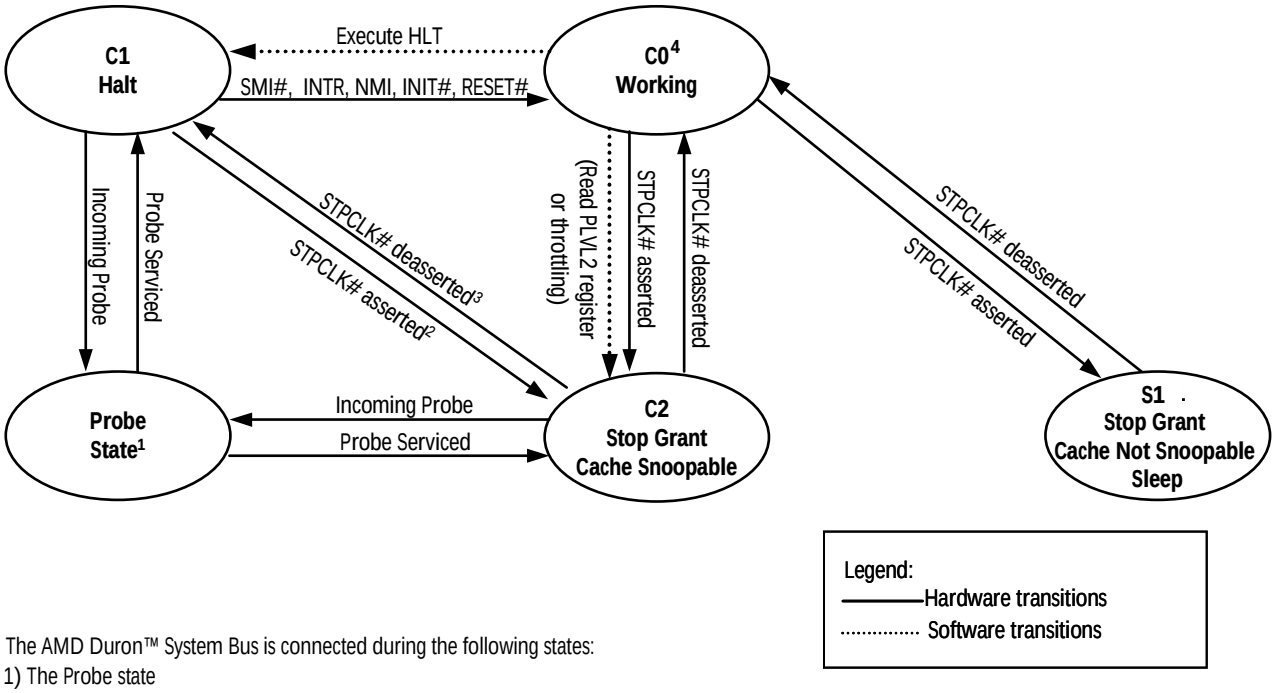


Figure 2. Logic Symbol Diagram

4 Power Management

4.1 Power Management States

The AMD Duron™ Processor Model 3 supports low-power Halt and Stop Grant states. These states are used by Advanced Configuration and Power Interface (ACPI) enabled operating systems for processor power management. Figure 3 shows the power management states of the AMD Duron Processor Model 3. The figure includes the ACPI "Cx" naming convention for these states.



The AMD Duron™ System Bus is connected during the following states:
1) The Probe state
2) During transitions from Halt state to Stop Grant state
3) Stop Grant state to the Halt state
4) C0 Working State

Figure 3. AMD Duron™ Processor Model 3 Power Management States

The following paragraphs describe each of the power management states.

Note: *In all power management states, the system must not disable the system clock (SYSCLK/SYSCLK#) to the processor.*

Working State

The Working state refers to the state in which the processor is executing instructions.

Halt State

When the AMD Duron Processor Model 3 executes the HLT instruction, the processor issues a Halt special cycle to the system bus. The phase-lock loop (PLL) continues to run, enabling the processor to monitor bus activity and provide a quick resume from the Halt state. The processor enters a lower power state if the system logic (Northbridge) disconnects the AMD Duron system bus in response to the Halt special cycle.

The Halt state is exited when the processor detects the assertion of INIT#, RESET#, SMI#, or an interrupt via the INTR or NMI pins, or via a local APIC interrupt message.

Stop Grant States

The AMD Duron Processor Model 3 enters the Stop Grant state upon recognition of assertion of STPCLK# input. There are two mechanisms for asserting STPCLK#—hardware and software. The Southbridge can force a STPCLK# assertion for throttling to protect the processor from exceeding its maximum case temperature. This task is accomplished by asserting the THERM# input to the Southbridge. Throttling asserts STPCLK# for a percentage of a predefined throttling period: STPCLK# is repetitively asserted and deasserted until the THERM# pin is deasserted.

Software can force the processor into the Stop Grant state by accessing ACPI-defined registers typically located in the Southbridge. Software places the processor in C2 by reading the PLVL_2 register in the Southbridge. In C2, probes are allowed, as shown in Figure 3 on page 9.

If an ACPI Thermal Zone is defined for the processor, the OS can initiate throttling with STPCLK# using the ACPI defined P_CNT register in the Southbridge. The processor enters the Probe state to service cache snoops initiated by the Northbridge during Stop Grant for C2 or throttling.

The Stop Grant state is also entered for the S1 system sleep state based on a write to the SLP_TYP field in the ACPI-defined power management 1 control register. During the S1 sleep state, system software ensures no bus master or probe activity occurs.

After recognizing the assertion of STPCLK#, the AMD Duron Processor Model 3 completes all pending and in-progress bus cycles and acknowledges the STPCLK# assertion by issuing a Stop Grant special bus cycle to the AMD Duron system bus. After the Northbridge disconnects the AMD Duron system bus in response to the Stop Grant special bus cycle, the processor enters a low-power state dictated by the CLK_Ctl register. During the Stop Grant states, the processor latches INIT#, INTR, NMI, and SMI#, or a local APIC interrupt message if they are asserted.

The Stop Grant state is exited upon the deassertion of STPCLK# or the assertion of RESET#. When STPCLK# is deasserted, the processor initiates a connection of the AMD Duron system bus if it is disconnected. After the processor enters the Working state, any pending interrupts are recognized and serviced and the processor resumes execution at the instruction boundary where STPCLK# was initially recognized.

If RESET# is sampled asserted during the Stop Grant state, the processor returns to the Working state and the reset process begins.

Probe State

The Probe state is entered when the Northbridge initiates an AMD Duron system bus connect as required to probe the processor. If the processor has been disconnected from the system bus, the Northbridge must initiate a system bus connection prior to probing the processor to snoop the processor's caches for example. When in the Probe state, the processor responds to a probe cycle in the same manner as when it is in the Working state.

When the probe has been serviced, the processor returns to the same state as when it entered the Probe state (Halt or Stop Grant state). Once in the Halt or Stop Grant state, a low-power state is only achieved if the Northbridge initiates a disconnection from the system bus.

4.2 Connect and Disconnect Protocol

Significant power savings of the AMD Duron Processor Model 3 only occurs if the processor is disconnected from the system bus by the Northbridge while in the Halt or Stop Grant state. The Northbridge can optionally initiate a bus disconnect upon the receipt of a Halt or Stop Grant special cycle. The option of disconnecting is controlled by an enable bit in the Northbridge. If the Northbridge requires the processor to service a probe after the system bus has been disconnected, it must first initiate a system bus connect.

Connect Protocol

In addition to the legacy STPCLK# signal and the Halt and Stop Grant special cycles, the AMD Duron system bus connect protocol includes the CONNECT, PROCRDY, and CLKFWDRST signals and a *Connect* special cycle.

AMD Duron system bus disconnects are initiated by the Northbridge in response to the receipt of a Halt or Stop Grant special cycle. Reconnect is initiated by the processor in response to an interrupt for Halt, STPCLK# deassertion, or by the Northbridge to service a probe.

The Northbridge contains BIOS programmable registers to enable the system bus disconnect in response to Halt and Stop Grant special cycles. When the Northbridge receives the Halt or Stop Grant special cycle from the processor and, if there are no outstanding probes or data movements, the Northbridge deasserts CONNECT a minimum of eight SYSCLK periods after the last command sent to the processor. The processor detects the deassertion of CONNECT on a rising edge of SYSCLK, and deasserts PROCRDY to the Northbridge. In return, the Northbridge asserts CLKFWDRST in anticipation of reestablishing a connection at some later point.

Note: *The Northbridge must disconnect the processor from the AMD Duron system bus before issuing the Stop Grant special cycle to the PCI bus, or passing the Stop Grant special cycle to the Southbridge for systems that connect to the Southbridge with HyperTransport™ technology.*

This note applies to current chipset implementation: alternate chipset implementations that do not require this state are possible.

Note: *In response to Halt special cycles, the Northbridge passes the Halt special cycle to the PCI bus or Southbridge immediately.*

The processor can receive an interrupt after it sends a Halt special cycle, or STPCLK# deassertion after it sends a Stop Grant special cycle to the Northbridge but before the disconnect actually occurs. In this case, the processor sends the Connect special cycle to the Northbridge, rather than continuing with the disconnect sequence. In response to the Connect special cycle, the Northbridge cancels the disconnect request.

The system is required to assert the CONNECT signal before returning the C-bit for the connect special cycle (assuming CONNECT has been deasserted). For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for the definition of the C-bit and the Connect special cycle.

Figure 4 shows the sequence of events from a Northbridge perspective, which leads to disconnecting the processor from the AMD Duron system bus and placing the processor in the Stop Grant state.

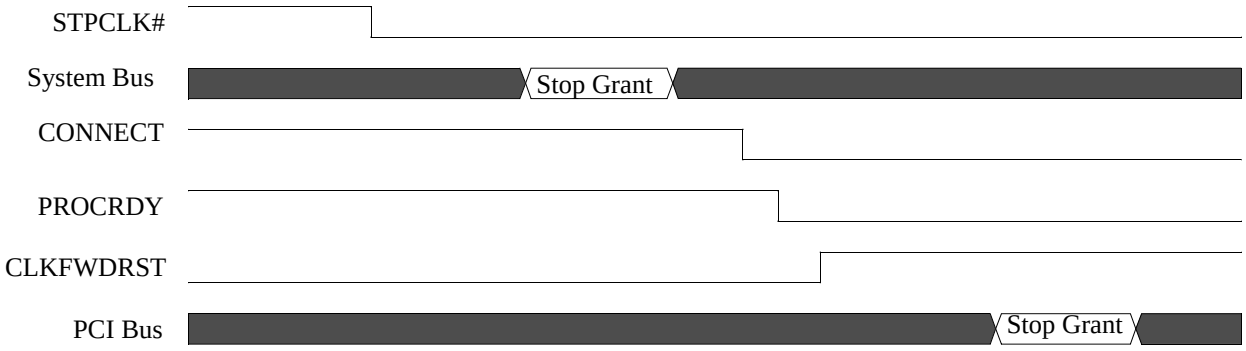


Figure 4. Example of an AMD Duron™ System Bus Disconnect Sequence

The following sequence of events describes how the processor is placed in the Stop Grant state when bus disconnect is enabled within the Northbridge:

1. The Southbridge asserts STPCLK# to place the processor in the Stop Grant state.

2. When the processor recognizes STPCLK# asserted, the processor enters the Stop Grant State, then issues a Stop Grant special cycle on the AMD Duron system bus.
3. When the Stop Grant special cycle is received by the Northbridge and no probe traffic is pending, the Northbridge deasserts CONNECT, initiating a bus disconnect to the processor.
4. The processor responds to the Northbridge by deasserting PROCRDY, acknowledging the bus disconnect request.
5. The Northbridge asserts CLKFWDRST to complete the bus disconnect sequence.
6. After the processor is disconnected from the bus, the Northbridge passes the Stop Grant special cycle to the Southbridge.

Figure 5 shows the signal sequence of events that take the processor out of the Stop Grant state, reconnect the processor to the AMD Duron system bus, and put the processor into the Working state.

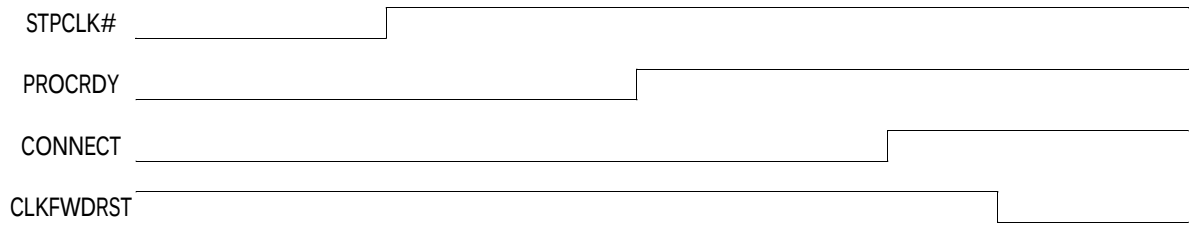


Figure 5. Exiting Stop Grant State/Bus Reconnect Sequence

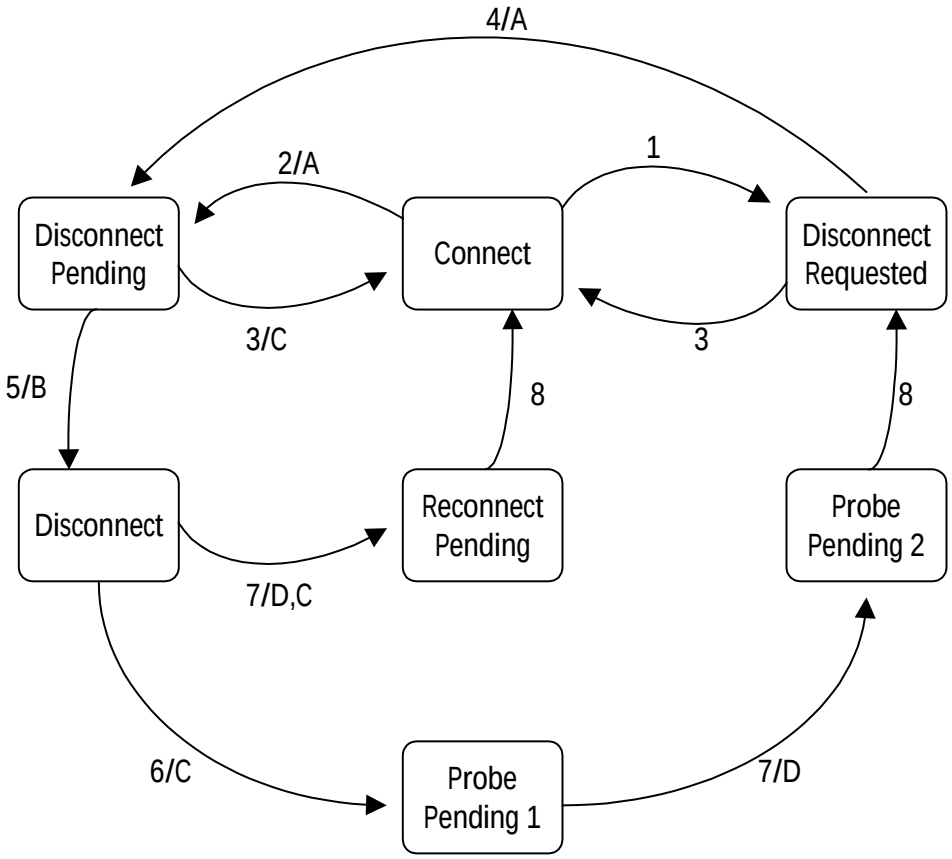
The following sequence of events removes the processor from the Stop Grant state and reconnects it to the AMD Duron system bus:

1. The Southbridge deasserts STPCLK# in response to a resume event.
2. When the processor recognizes STPCLK# deassertion, it asserts PROCRDY, notifying the Northbridge to reconnect to the bus.
3. The Northbridge asserts CONNECT.

4. The Northbridge finally deasserts CLKFWDRST, which synchronizes the forwarded clocks between the processor and the Northbridge.

Connect State Diagram

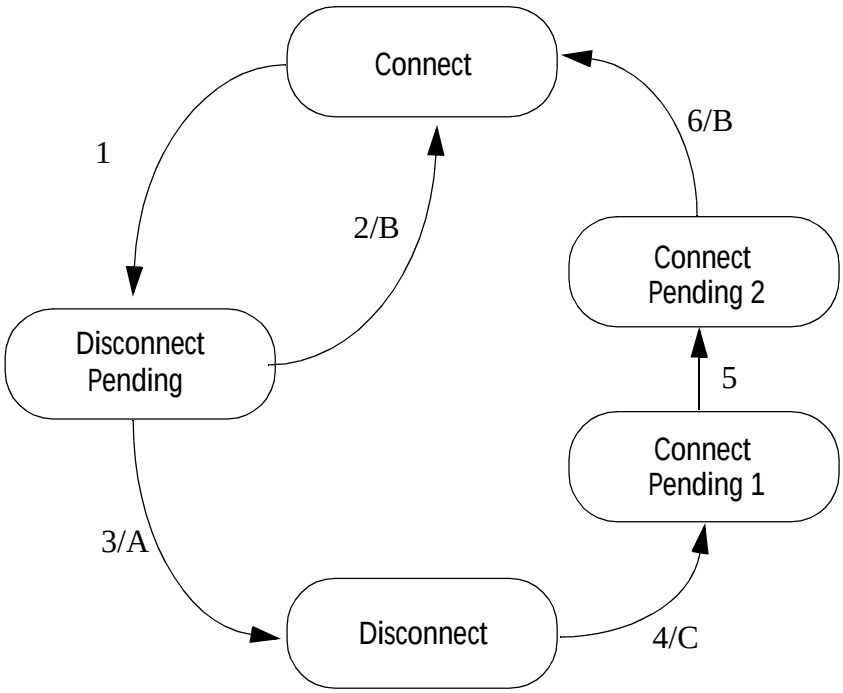
Figure 6 and Figure 7 describe the Northbridge and processor connect state diagrams, respectively.



	Condition
1	A disconnect is requested and probes are still pending
2	A disconnect is requested and no probes are pending
3	A CONNECT special cycle from the processor
4	No probes are pending
5	PROCRDY is deasserted
6	A probe needs service
7	PROCRDY is asserted
8	3 SYSCLK periods after CLKFWDRST is deasserted. *Although reconnected to the system interface, the Northbridge must not issue any non-NOP SysDC commands for a minimum of four SYSCLK periods after deasserting CLKFWDRST.*

	Action
A	Deassert CONNECT 8 SYSCLK periods after last SysDC sent
B	Assert CLKFWDRST
C	Assert CONNECT
D	Deassert CLKFWDRST

Figure 6. Northbridge Connect State Diagram



	Condition
1	CONNECT is deasserted by the Northbridge (for a previously sent Halt or Stop Grant special cycle).
2	Processor receives a wake-up event and must cancel the disconnect request.
3	Deassert PROCRDY and slow down internal clocks.
4	Processor wake-up event or CONNECT asserted by Northbridge.
5	CLKFWDRST is deasserted by the Northbridge.
6	Forward clocks start 3 SYSCLK periods after CLKFWDRST is deasserted.

	Action
A	CLKFWDRST is asserted by the Northbridge.
B	Issue a CONNECT special cycle.*
C	Return internal clocks to full speed and assert PROCRDY

***** *The Connect special cycle is only issued after a processor wake-up event (interrupt or STPCLK# deassertion) occurs. If the AMD Duron system bus is connected so the Northbridge can probe the processor a Connect special cycle is not issued at that time (it is only issued after a subsequent processor wake-up event).*

Figure 7. Processor Connect State Diagram

4.3 Clock Control

The processor implements a Clock Control (CLK_Ctl) MSR (address C001_001Bh) that determines the internal clock divisor when the AMD Duron system bus is disconnected.

Refer to the *AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656, for more details on the CLK_Ctl register.

5 Thermal Design

For information about thermal design, including layout and airflow considerations, see the *AMD Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794 and the cooling guidelines on www.amd.com.

Table 1 shows the thermal design power. The thermal design power represents the maximum sustained power dissipated while executing publicly available software or instruction sequences under normal system operation at nominal VCC_CORE. Thermal solutions must monitor the processor temperature to prevent the processor from exceeding its maximum die temperature.

The maximum die temperature is specified through characterization at 90°C.

Table 1. Thermal Design Power

Frequency (MHz)	Nominal Voltage	Maximum Thermal Power	Typical Thermal Power	Max Die Temperature
600	1.6 V	27.4 W	24.5 W	90° C
650		29.4 W	26.4 W	
700		31.4 W	28.2 W	
750		33.4 W	30.0 W	
800		35.4 W	31.8 W	
850		37.4 W	33.6 W	
900		39.5 W	35.4 W	
950		41.5 W	37.2 W	

6 CPUID Support

AMD Duron™ Processor Model 3 version and feature set recognition can be performed through the use of the CPUID instruction, that provides complete information about the processor—vendor, type, name, etc., and its capabilities. Software can make use of this information to accurately tune the system for maximum performance and benefit to users.

For information on the use of the CPUID instruction, see the *AMD Processor Recognition Application Note* , order# 20734.

7 Electrical Data

7.1 Conventions

The conventions used in this chapter are as follows:

- Current specified as being sourced by the processor is *negative*.
- Current specified as being sunk by the processor is *positive*.

7.2 Interface Signal Groupings

The electrical data in this chapter is presented separately for each signal group. Table 2 defines each group and the signals contained in each group.

Table 2. Interface Signal Groupings

Signal Group	Signals	Notes
Power	VID[4:0], VCC_CORE, VCCA, COREFB, COREFB#	See "Voltage Identification (VID[4:0])" on page 24, "VID[4:0] Pins" on page 67, and "VCCA AC and DC Characteristics" on page 25.
Frequency	FID[3:0]	See "Frequency Identification (FID[3:0])" on page 24 and "FID[3:0] Pins" on page 63.
System Clocks	SYSCLK, SYSCLK# (Tied to CLKIN/CLKIN# and RSTCLK/RSTCLK#), PLLBYPASSCLK#, PLLBYPASSCLK	See "SYSCLK and SYSCLK# DC Characteristics" on page 28.
AMD Duron™ System Bus	SADDIN[14:2]#, SADDOUT[14:2]#, SADDINCLK#, SADDOUTCLK#, SFILLVAL#, SDATAINVAL#, SDATAOUTVAL#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAOUTCLK[3:0]#, SCHECK[7:0]#, CLKFWDRST, PROCRDY, CONNECT	See "AMD Duron™ System Bus AC and DC Characteristics" on page 30.
Southbridge	RESET#, INTR, NMI, SMI#, INIT#, A20M#, FERR, IGNNE#, STPCLK#, FLUSH#	See "General AC and DC Characteristics" on page 32.
JTAG	TMS, TCK, TRST#, TDI, TDO	See "General AC and DC Characteristics" on page 32.
APIC	PICD[1:0]#, PICCLK	See "APIC Pins AC and DC Characteristics" on page 34 and "APIC Pins, PICCLK, PICD[1:0]#" on page 62.

Table 2. Interface Signal Groupings (continued)

Signal Group	Signals	Notes
Test	PLLTEST#, PLLMON1, PLLMON2, SCANCLK1, SCANCLK2, SCANSHIFTEN, SCANINTEVAL, ANALOG	See "General AC and DC Characteristics" on page 32.
Miscellaneous	DBREQ#, DBRDY, PWROK, PLLBYPASS#	See "General AC and DC Characteristics" on page 32.

7.3 Voltage Identification (VID[4:0])

Table 3 shows the VID[4:0] DC characteristics. For more information, see "VID[4:0] Pins" on page 65.

Table 3. VID[4:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low	16 mA	
V_{OH}	Output High Voltage		2.625 V *

Note:
* *The VID pins must not be pulled above this voltage by an external pullup resistor.*

7.4 Frequency Identification (FID[3:0])

Table 4 shows the FID[3:0] DC characteristics. For more information, see "VID[4:0] Pins" on page 67.

Table 4. FID[3:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low	16 mA	
V_{OH}	Output High Voltage		2.625 V *

Note:
* *The FID pins must not be pulled above this voltage by an external pullup resistor.*

7.5 VCCA AC and DC Characteristics

Table 5 shows the AC and DC characteristics for VCCA. For more information, see “VCCA Pin” on page 67.

Table 5. VCCA AC and DC Characteristics

Symbol	Parameter	Min	Nominal	Max	Units	Notes
I_{VCCA}	VCCA Pin Current	0		50	mA/GHz	1
V_{VCCA}	VCCA Pin Voltage (AC & DC)	2.25	2.5	2.75	V	2

Notes:
1. *Measured at 2.5 V*
2. *Minimum and maximum voltages are absolute. No transients below minimum nor above maximum voltages are permitted.*

7.6 Decoupling

AMD Athlon™ Processor-Based Motherboard Design Guide, order# 24363, or contact your local AMD office for information about the decoupling required on the motherboard for use with the AMD Duron™ Processor Model 3.

7.7 Operating Ranges

The AMD Duron Processor Model 3 is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in Table 6.

Table 6. Operating Ranges

Parameter	Description		Min	Nominal	Max	Notes
VCC_CORE	Processor core supply	600-950 MHz	1.5 V	1.6 V	1.7 V	1
VCC_CORE_{SLEEP}	Processor core supply in Sleep state		1.2 V	1.3 V	1.4 V	2
T_{DIE}	Temperature of processor die				90º C	

Notes:
1. *For normal operating conditions (nominal VCC_CORE is 1.6 V)*
2. *Sleep Voltage can be used for the S1 sleep state..*

7.8 Absolute Ratings

The AMD Duron Processor Model 3 should not be subjected to conditions exceeding the absolute ratings listed in Table 7, as such conditions can adversely affect long-term reliability or result in functional damage.

Table 7. Absolute Ratings

Parameter	Description	Min	Max
VCC_CORE	AMD Duron™ Processor Model 3 core supply	–0.5 V	VCC_CORE Max + 0.5 V
VCCA	AMD Duron Processor Model 3 PLL Supply	–0.5 V	VCCA Max + 0.5 V
V_{PIN}	Voltage on any signal pin	–0.5 V	VCC_CORE Max + 0.5 V
$T_{STORAGE}$	Storage temperature of processor	–40º C	100º C

7.9 VCC_CORE Voltage and Current

Table 8 shows the power and current of the processor during normal and reduced power states.

Table 8. VCC_CORE Voltage and Current

Frequency (MHz)	Nominal Voltage	Maximum Voltage	Stop Grant (Maximum)[1]	Maximum I_{CC} (Power Supply Current)[2]	Die Temperature
600	1.6 V	1.7 V	5 W	17.1 A	90° C
650				18.4 A	
700				19.6 A	
750				20.9 A	
800				22.1 A	
850				23.4 A	
900				24.7 A	
950				25.9 A	

Notes:

1. *Measured at 1.3V for Sleep state operating conditions. The BIOS must program the CLK_Ctrl MSR to fff0_d22fh for the AMD Duron™ Processor Model 3.*
2. *Measured at Nominal voltage of 1.6 V.*

7.10 SYSCLK and SYSCLK# AC and DC Characteristics

Table 9 shows the DC characteristics of the SYSCLK and SYSCLK# differential clocks. The SYSCLK signal represents CLKIN and RSTCLK tied together while the SYSCLK# signal represents CLKIN# and RSTCLK# tied together. Figure 8 shows this condition.

Table 9. SYSCLK and SYSCLK# DC Characteristics

Symbol	Description	Min	Max	Units
$V_{Threshold-DC}$	Crossing before transition is detected (DC)	400		mV
$V_{Threshold-AC}$	Crossing before transition is detected (AC)	450		mV
I_{LEAK_P}	Leakage current through P-channel pullup to VCC_CORE	–1		mA
I_{LEAK_N}	Leakage current through N-channel pulldown to VSS (Ground)		1	mA
V_{CROSS}	Differential signal crossover		VCC_CORE/2 +/– 100	mV
C_{PIN}	Capacitance	4	12	pF

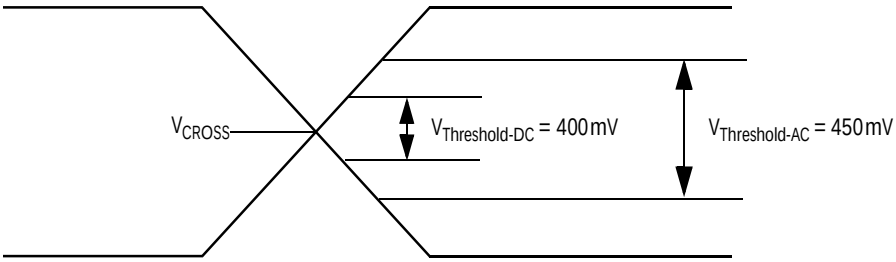


Figure 8. SYSCLK and SYSCLK# Differential Clock Signals

Table 10 shows the SYSCLK/SYSCLK# differential clock AC characteristics of the AMD Duron Processor Model 3. Figure 9 shows a sample waveform.

Table 10. SYSCLK and SYSCLK# AC Characteristics

Symbol	Parameter Description	Min	Max	Units	Notes
	Clock Frequency	50	100	MHz	
	Duty Cycle	30%	70%		
t_1	Period	10		ns	1, 2
t_2	High Time	1.8		ns	
t_3	Low Time	1.8		ns	
t_4	Fall Time		2	ns	
t_5	Rise Time		2	ns	
	Period Stability		± 300	ps	

Notes:

1. *Circuitry driving the SYSCLK & SYSCLK# inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The –20 dB attenuation point, as measured into a 10-pF or 20-pF load must be less than 500 kHz.*
2. *Circuitry driving the SYSCLK & SYSCLK# inputs can purposely alter the SYSCLK & SYSCLK# period (spread spectrum clock generators). In no cases can the SYSCLK & SYSCLK# period violate the minimum specification above. SYSCLK & SYSCLK# inputs can vary from 100% of the specified period to 99% of the specified period at a maximum rate of 100 kHz.*

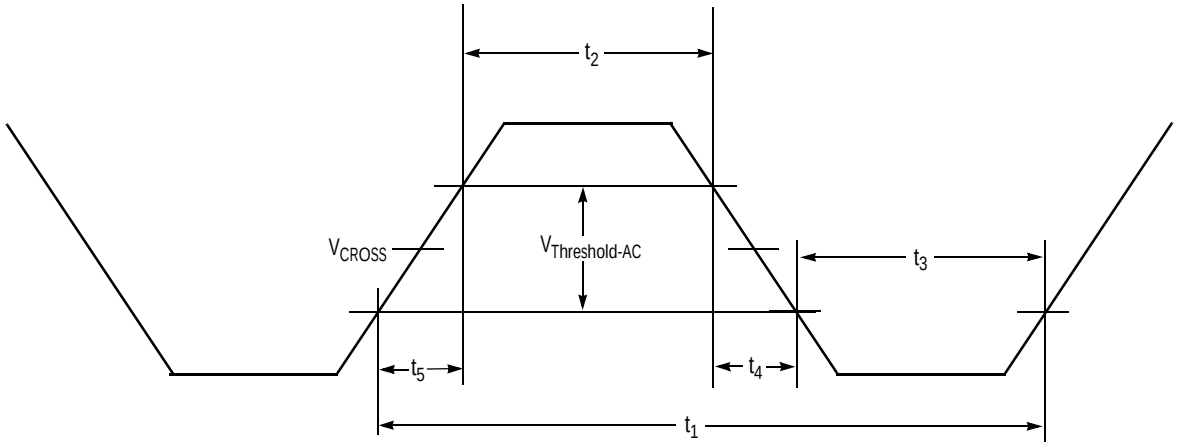


Figure 9. SYSCLK Waveform

7.11 AMD Duron™ System Bus AC and DC Characteristics

Table 11 shows the DC characteristics of the AMD System Bus used by the AMD Duron Processor Model 3.

Table 11. AMD Duron™ System Bus DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{REF}	DC Input Reference Voltage		(0.5*VCC_CORE) –50	(0.5*VCC_CORE) +50	mV	1
$I_{VREF\_LEAK\_P}$	V_{REF} Tristate Leakage Pullup	V_{IN} = V_{REF} Nominal	–100		µA	
$I_{VREF\_LEAK\_N}$	V_{REF} Tristate Leakage Pulldown	V_{IN} = V_{REF} Nominal		+100	µA	
V_{IH}	Input High Voltage		V_{REF} + 200	VCC_CORE + 500	mV	
V_{IL}	Input Low Voltage		–500	V_{REF} – 200	mV	
V_{OH}	Output High Voltage	I_{OUT} = –200 µA	0.85*VCC_CORE	VCC_CORE+500	mV	2
V_{OL}	Output Low Voltage	I_{OUT} = 1 mA	–500	400	mV	2
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN} = VCC_CORE Nominal		+1	mA	
C_{IN}	Input Pin Capacitance		4	12	pF	3

Notes:

1. *V_{REF} is nominally set to 50% of VCC_CORE with actual values that are specific to motherboard design implementation. V_{REF} must be created with a sufficiently accurate DC source and a sufficiently quiet AC response to adhere to the ± 50 mV specification listed above.*
2. *Specified at T = 90°C and VCC_CORE*
3. *The following processor inputs have twice the listed capacitance because they connect to two input pads— SYSCLK, and SYSCLK#. SYSCLK connects to CLKIN/RSTCLK. SYSCLK# connects to CLKIN#/RSTCLK#. For more information, see Table 16 on page 48 .*

The AC characteristics of the AMD Duron system bus are shown in Table 12. The parameters are grouped based on the source or destination of the signals involved.

Table 12. AMD Duron™ System Bus AC Characteristics

Group	Symbol	Parameter	Min	Max	Units	Notes
All Signals	T_{RISE}	Output Rise Slew Rate	1	3	V/ns	1
	T_{FALL}	Output Fall Slew Rate	1	3	V/ns	1
Forward Clocks	$T_{SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge		385	ps	2
	$T_{SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge		770	ps	2
	T_{SU}	Input Data Setup Time	300		ps	3
	T_{HD}	Input Data Hold Time	300		ps	3
	C_{IN}	Capacitance on input Clocks	4	12	pF	
	C_{OUT}	Capacitance on output Clocks	4	12	pF	
Sync[4]	T_{VAL}	RSTCLK to Output Valid	250	2000	ps	5
	T_{SU}	Setup to RSTCLK	500		ps	6
	T_{HD}	Hold from RSTCLK	1000		ps	6

Notes:

1. *Rise and fall time ranges are guidelines over which the I/O has been characterized.*
2. *$T_{SKEW-SAMEEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.*
   $T_{SKEW-DIFFEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
3. *Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.*
4. *The synchronous signals include PROCRDY, CONNECT, CLKFWDRST.*
5. *T_{VAL} is RSTCLK rising edge to output valid for PROCRDY. Test Load is 25pF.*
6. *T_{SU} is setup of CONNECT/CLKFWDRST to rising edge of RSTCLK. T_{HD} is hold of CONNECT/CLKFWDRST from rising edge of RSTCLK.*

7.12 General AC and DC Characteristics

Table 13 shows the AMD Duron Processor Model 3 AC and DC characteristics of the Southbridge, JTAG, test, and miscellaneous pins.

Table 13. General AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		(VCC_CORE/2) + 200mV	VCC_CORE max	V	1,2
V_{IL}	Input Low Voltage		–300	350	mV	1,2
V_{OH}	Output High Voltage		VCC_CORE – 400	VCC_CORE + 300	mV	
V_{OL}	Output Low Voltage		–300	400	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN} = VCC_CORE Nominal		600	µA	
I_{OH}	Output High Current			–16	mA	3
I_{OL}	Output Low Current		16		mA	3
T_{SU}	Sync Input Setup Time		2.0		ns	4, 5
T_{HD}	Sync Input Hold Time		0.0		ps	4, 5
T_{DELAY}	Output Delay with respect to RSTCLK		0.0	6.1	ns	5
T_{BIT}	Input Time to Acquire		20.0		ns	7,8
T_{RPT}	Input Time to Reacquire		40.0		ns	9-13

Notes:

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal VCC_CORE. Scale parameters between VCC_CORE Min and VCC_CORE Max.*
3. *I_{OL} and I_{OH} are measured at V_{OL} max and V_{OH} min, respectively.*
4. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
5. *These are aggregate numbers.*
6. *Edge rates indicate the range over which inputs were characterized.*
7. *In asynchronous operation, the signal must persist for this time to guarantee capture.*
8. *This value assumes RSTCLK frequency is 10 ns ==> TBIT = 2*fRST.*
9. *The approximate value for standard case in normal mode operation.*
10. *This value is dependent on RSTCLK frequency, divisors, LowPower mode, and core frequency.*
11. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
12. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
13. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*

Table 13. General AC and DC Characteristics (continued)

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
T_{RISE}	Signal Rise Time		1.0	3.0	V/ns	6
T_{FALL}	Signal Fall Time		1.0	3.0	V/ns	6
C_{PIN}	Pin Capacitance		4	12	pF	

Notes:

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal VCC_CORE. Scale parameters between VCC_CORE Min and VCC_CORE Max.*
3. *I_{OL} and I_{OH} are measured at V_{OL} max and V_{OH} min, respectively.*
4. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
5. *These are aggregate numbers.*
6. *Edge rates indicate the range over which inputs were characterized.*
7. *In asynchronous operation, the signal must persist for this time to guarantee capture.*
8. *This value assumes RSTCLK frequency is 10 ns ==> TBIT = 2*fRST.*
9. *The approximate value for standard case in normal mode operation.*
10. *This value is dependent on RSTCLK frequency, divisors, LowPower mode, and core frequency.*
11. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
12. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
13. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*

7.13 APIC Pins AC and DC Characteristics

Table 14 shows the AMD Duron Processor Model 3 AC and DC characteristics of the APIC pins.

Table 14. APIC Pins AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		1.7	2.625	V	1, 3
V_{IL}	Input Low Voltage		–300	700	mV	1, 2
V_{OH}	Output High Voltage			2.625	V	3
V_{OL}	Output Low Voltage		–300	400	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN} = 2.5 V		1	mA	
I_{OL}	Output Low Current	V_{OL} Max	12		mA	
T_{RISE}	Signal Rise Time		1.0	3.0	V/ns	4
T_{FALL}	Signal Fall Time		1.0	3.0	V/ns	4
C_{PIN}	Pin Capacitance		4	12	pF	

Notes:

1. *Characterized across DC supply voltage range*
2. *Values specified at nominal VDD (1.5 V). Scale parameters with VDD*
3. *2.625 V = 2.5 V + 5% maximum*
4. *Edge rates indicate the range over which inputs were characterized*

8 Signal and Power-Up Requirements

This chapter describes the AMD Duron™ Processor Model 3 power-up requirements during system power-up and warm resets.

8.1 Power-Up Requirements

Signal Sequence and Timing Description

Figure 10 shows the relationship between key signals in the system during a power-up sequence. This figure details the requirements of the processor.

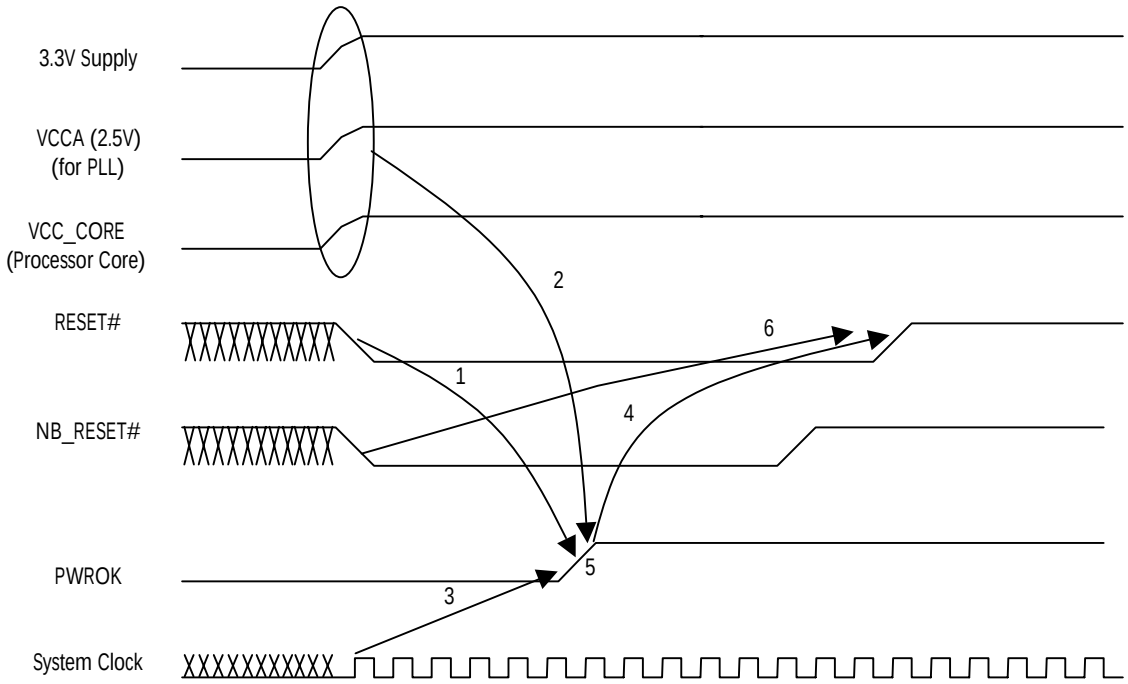


Figure 10. Signal Relationship Requirements During Power-Up Sequence

Notes: *1) Figure 10 represents several signals generically by using names not necessarily consistent with any pin lists or schematics.*

2) Requirements 1-6 in Figure 10 are described in the following section.

Power-Up Timing Requirements. The signal timing requirements are as follows:

1. RESET# must be asserted before PWROK is asserted.

   The AMD Duron Processor Model 3 does not set the correct clock multiplier if PWROK is asserted prior to a RESET# assertion. It is recommended that RESET# be asserted at least **10ns** prior to the assertion of PWROK.

   In practice, Southbridges assert RESET# milliseconds before PWROK is deasserted.

2. All motherboard voltage planes must be within specification before PWROK is asserted.

   PWROK is an output of the voltage regulation circuit on the motherboard. PWROK indicates that VCC_CORE and all other voltage planes in the system are within specification.

   The motherboard is required to delay PWROK assertion for a minimum of 3 milliseconds from the 3.3V supply being within specification. This delay ensures that the system clock (SYSCLK/SYSCLK#) is operating within specification when PWROK is asserted.

   The processor core voltage, VCC_CORE, must be within specification as dictated by the VID[4:0] pins driven by the processor before PWROK is asserted. Before PWROK assertion, the processor is clocked by a ring oscillator.

   The processor PLL is powered by VCCA. The processor PLL does not lock if VCCA is not high enough for the processor logic to switch for some period before PWROK is asserted. VCCA must be within spec at least 5 microseconds before PWROK is asserted.

   In practice VCCA, VCC_CORE, and all other voltage planes must be within specification be for several milliseconds before PWROK is asserted.

   After PWROK is asserted, the processor PLL locks to its operational frequency.

3. The system clock (SYSCLK/SYSCLK#) must be running within specification before PWROK is asserted.

   When PWROK is asserted, the processor switches from driving the internal processor clock grid from the ring oscillator to driving from the PLL. The reference system clock should be valid at this time. The system clocks are guaranteed to be running after 3.3V has been within specification for 3 milliseconds.

4. PWROK assertion to deassertion of RESET#.

   The duration of RESET# assertion during cold boots is intended to satisfy the time it takes for the PLL to lock with a less than 1-ns phase error. The processor PLL begins to run after PWROK is asserted and the internal clock grid is switched from the ring oscillator to the PLL. The PLL lock time can take from hundreds of nanoseconds to tens of microseconds. It is recommended that the minimum time between PWROK assertion to the deassertion of RESET# be at least **1.0ms**. AMD Southbridges enforce a delay of 1.5 to 2.0 milliseconds between PWRGD (Southbridge version of PWROK) assertion and NB_RESET# deassertion.

5. PWROK must be monotonic.

   The processor should not switch between the ring oscillator and the PLL after the initial assertion of PWROK.

6. NB_RESET# must be asserted (causing CONNECT to also assert) before RESET# is deasserted. In practice all Southbridges enforce this requirement.

   If NB_RESET# does not assert until after RESET# has deasserted, the processor misinterprets the CONNECT assertion (due to NB_RESET# being asserted) as the beginning of the SIP transfer (See "Serial Initialization Packet (SIP) Protocol" on page 38). There must be sufficient overlap in the resets to ensure that CONNECT is sampled asserted by the processor before RESET# is deasserted.

Clock Multiplier Selection (FID[3:0])

When RESET# is de-asserted, the Northbridge samples the FID[3:0] Frequency ID from the processor in a chipset specific manner. For more information, see "FID[3:0] Clock Multiplier Encodings" on page 64.

The Northbridge uses this FID information and other information sampled at the deassertion of RESET# to determine the correct Serial Initialization Packet (SIP) to send to the processor for configuration of the AMD Duron system bus for the clock multiplier (processor frequency) indicated by the FID[3:0] code. The SIP is sent to the processor using the SIP protocol. This protocol uses the PROCRDY, CONNECT, and CLKFWDRST signals, which are synchronous to SYSCLK.

Serial Initialization Packet (SIP) Protocol

Refer to the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for details of the SIP protocol. Packet (SIP) Protocol

8.2 Processor Warm Reset Requirements

The AMD Duron™ Processor Model 3 and Northbridge Reset Pins

RESET cannot be asserted to the processor without also being asserted to the Northbridge. RESET# to the Northbridge is the same in as PCI RESET#. The minimum assertion for PCI RESET# is 1 millisecond. AMD Southbridges enforce a minimum assertion of RESET# (processor, Northbridge, PCI) of 1.5 to 2.0 milliseconds.

9 Mechanical Data

9.1 Introduction

The AMD Duron™ Processor Model 3 connects to the motherboard through a PGA socket named Socket A. For more information, see the *AMD Athlon Processor Socket 462 Application Note*, order# 90020.

9.2 Die Loading

The processor die on the CPGA package is exposed at the top of the package. This is done to facilitate heat transfer from the die to an approved heat sink. It is critical that the mechanical loading of the heat sink does not exceed the limits shown in Table 15. Any heat sink design should avoid loads on corners and edges of die. The CPGA package has compliant pads that serve to bring surfaces in planar contact.

Table 15. CPGA Mechanical Loading

Location	Dynamic (MAX)	Static (MAX)	Units	Note
Die Surface	100	30	lbf	2
Die Edge	10	10	lbf	3

Notes:

1. *Tool–assisted zero insertion force sockets should be designed such that no load is placed on the ceramic substrate of the package.*
2. *Load specified for coplanar contact to die surface.*
3. *Load defined for a surface at no more than a 2 degree angle of inclination to die surface.*

9.3 Pinout Diagram

The pin location designations for the Socket A connector are shown in Figure 11 on page 41. Voided (plugged) pin locations should have a base that accepts a contact, but the top plate of Socket A should *not* have pin openings. The *exceptions* are the two plugs on the outside corners, which should be permanently closed and not accommodate a contact. It is permissible, if necessary for manufacturing reasons, to place a contact in the base at plug sites (*except* for the two plugs on the outside corners). Socket A has 462 pin sites, with 11 plugs total. For more information, see Chapter 10, "Pin Descriptions" on page 45.

In addition, Figure 11 on page 41 shows the Socket A package side view and top view.

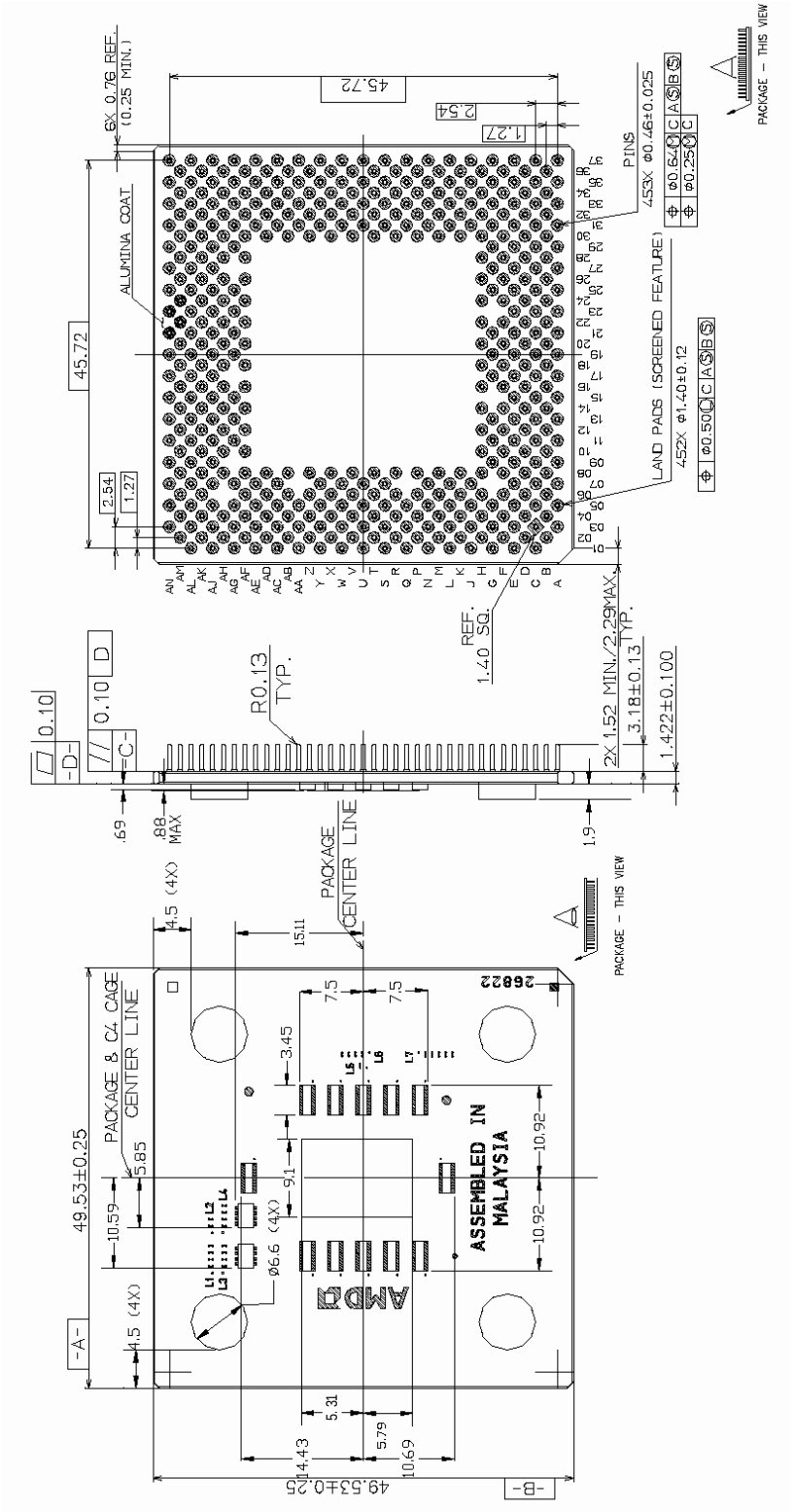
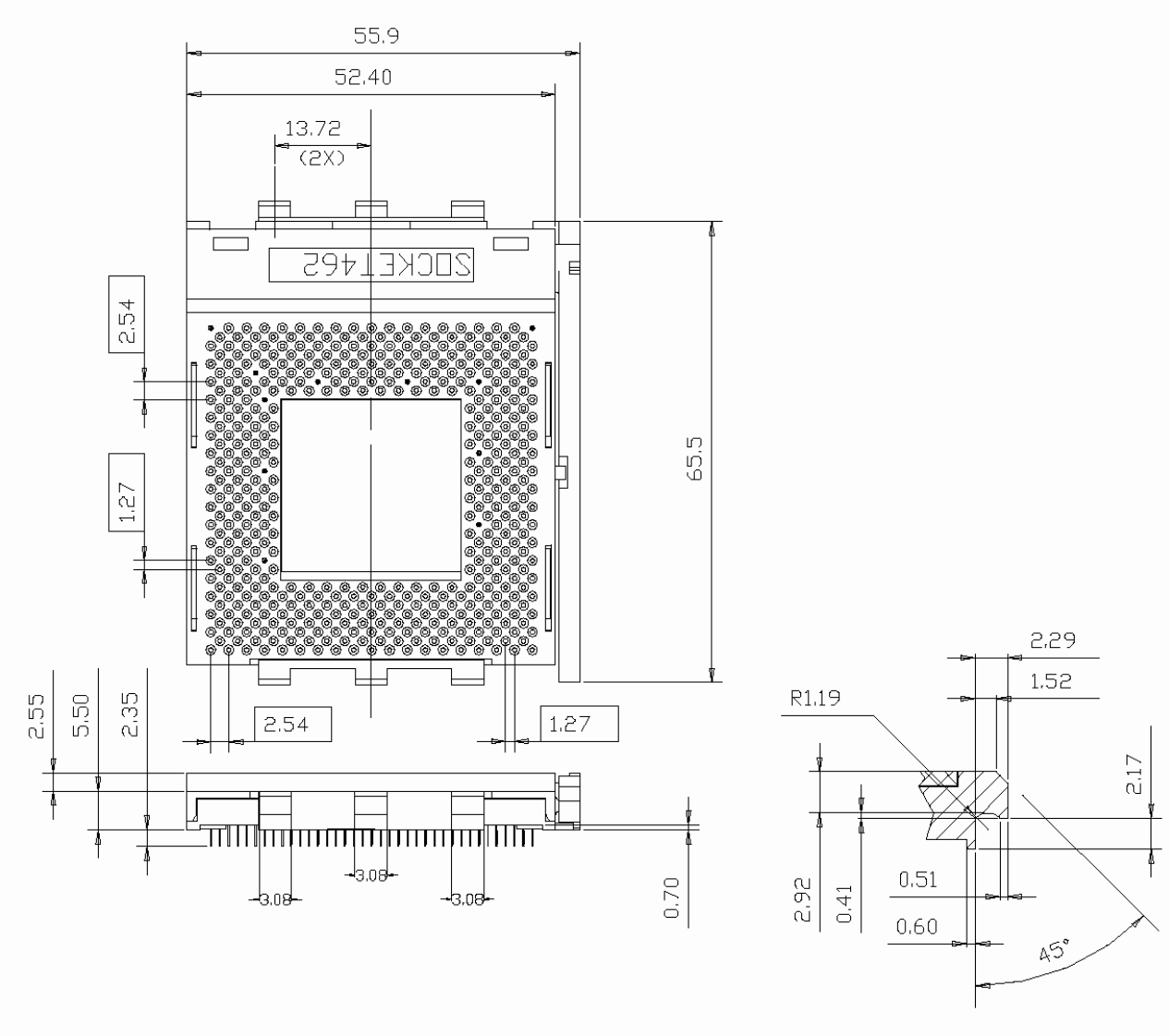


Figure 11. PGA Package, Top, Side, and Bottom Views

9.4 Socket Tabs for Heatsink Clips

Figure 12 shows the socket tab required on Socket A. These features are required to support a 300g heatsink. Figure 13 on page 43 shows the socket tab side view.



Note: *Measurements are in mm*

Figure 12. Socket A with Outline of Socket and Heatsink Tab

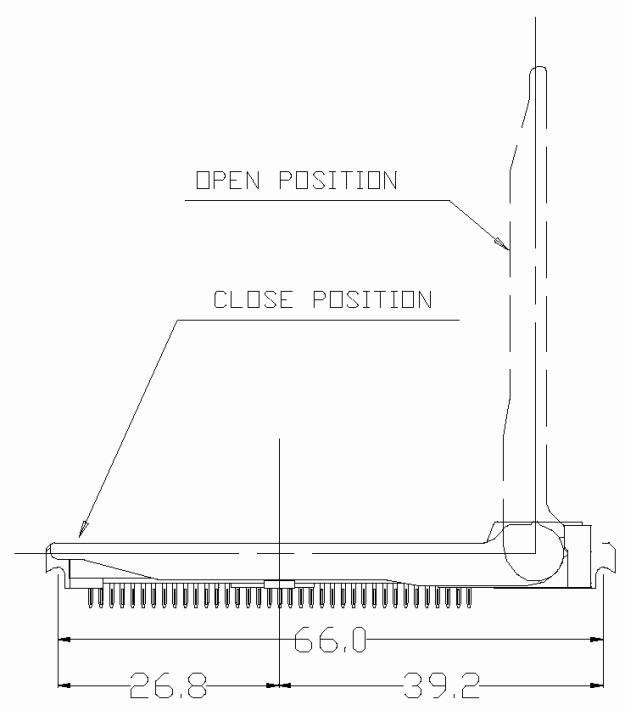


Figure 13. Socket A Heatsink Tab Side View

10 Pin Descriptions

10.1 Pin Diagram and Pin Name Abbreviations

Figure 14 on page 46 shows the staggered Pin Grid Array (PGA) for the AMD Duron™ Processor Model 3. Because some of the pin names are too long to fit in the grid, they are abbreviated. Figure 15 on page 47 shows the bottomside view of the array. Table 16 on page 48 lists all the pins in alphabetical order by pin name, along with the abbreviation where necessary.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	
A			SAO#12		SAO#5		SAO#3		SD#55		SD#61		SD#53		SD#63		SD#62		SCK#7		SD#57		SD#39		SD#35		SD#34		SD#44		SCK#5		SDOC#2		SD#40		SD#30	**A**
B		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		**B**
C	SAO#7		SAO#9		SAO#8		SAO#2		SD#54		SDOC#3		SCK#6		SD#51		SD#60		SD#59		SD#56		SD#37		SD#47		SD#38		SD#45		SD#43		SD#42		SD#41		SDOC#1	**C**
D		VCC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VSS		**D**
E	SAO#11		SAOC#		SAO#4		SAO#6		SD#52		SD#50		SD#49		SDIC#3		SD#48		SD#58		SD#36		SD#46		SCK#4		SDIC#2		SD#33		SD#32		SCK#3		SD#31		SD#22	**E**
F		VSS		VSS		VSS		NC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		NC		VCC		VCC		VCC		**F**
G	SAO#10		SAO#14		SAO#13				KEY		NC		NC				KEY		NC		NC				KEY		NC		NC		NC		SD#20		SD#23		SD#21	**G**
H		VCC		VCC		NC		NC		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		NC		NC		NC		VSS		VSS		**H**
J	SAO#0		SAO#1		NC		VID[4]																							NC		SD#19		SDIC#1		SD#29	**J**
K		VSS		VSS		VSS		NC																						NC		VCC		VCC		VCC		**K**
L	VID[0]		VID[1]		VID[2]		VID[3]																								NC		SD#26		SCK#2		SD#28	**L**
M		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		**M**
N	PICCLK		PICD#0		PICD#1		KEY																								NC		SD#25		SD#27		SD#18	**N**
P		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		**P**
Q	TCK		TMS		SCNSN																										NC		SD#24		SD#17		SD#16	**Q**
R		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		**R**
S	SCNCK1		SCNINV		SCNCK2		NC																								NC		SD#7		SD#15		SD#6	**S**
T		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		**T**
U	TDI		TRST#		TDO		NC																								NC		SD#5		SD#4		SCK#0	**U**
V		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		**V**
W	FID[0]		FID[1]		VREF_S		NC																								NC		SDIC#0		SD#2		SD#1	**W**
X		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		**X**
Y	FID[2]		FID[3]		NC		KEY																								NC		SCK#1		SD#3		SD#12	**Y**
Z		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		**Z**
AA	DBRDY		DBREQ#		SVRFM																										NC		SD#8		SD#0		SD#13	**AA**
AB		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		**AB**
AC	STPC#		PLTST#		ZN		VCC_Z																								NC		SD#10		SD#14		SD#11	**AC**
AD		VCC		VCC		VCC		NC																						NC		VSS		VSS		VSS		**AD**
AE	A20M#		PWROK		ZP		VSS_Z																								NC		SAI#5		SDOC#0		SD#9	**AE**
AF		VSS		VSS		NC		NC		NC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		NC		NC		VCC		VCC		**AF**
AG	FERR		RESET#		NC		KEY				COREFB		COREFB#		KEY				NC		NC		NC		NC				KEY		NC		SAI#2		SAI#11		SAI#7	**AG**
AH		VCC		VCC		AMD		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		NC		VSS		VSS		VSS		**AH**
AJ	IGNNE#		INIT#		VCC		NC		NC		NC		ANLOG		NC		NC		NC		CLKFR		VCCA		PLBYP#		NC		SAI#0		SFILLV#		SAIC#		SAI#6		SAI#3	**AJ**
AK		VSS		VSS		CPR#		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VCC		**AK**
AL	INTR		FLUSH#		VCC		NC		NC		NC		PLMN2		PLBYC#		CLKIN#		RCLK#		K7CO		CNNCT		NC		NC		SAI#1		SDOV#		SAI#8		SAI#4		SAI#10	**AL**
AM		VCC		VSS		VSS		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		**AM**
AN			NMI		SMI#		NC		NC		NC		PLMN1		PLBYC		CLKIN		RCLK		K7CO#		PRCRDY		NC		NC		SAI#12		SAI#14		SDINV#		SAI#13		SAI#9	**AN**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	

AMD Duron™ Processor
Model 3
Topside View

Figure 14. AMD Duron™ Processor Model 3 Pin Diagram—Topside View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	
1			SAO#7		SAO#11		SAO#10		SAO#0		VID[0]		PICCLK		TCK		SCNCK1		TDI		FID[0]		FID[2]		DBRDY		STPC#		A20M#		FERR		IGNNE#		INTR			1
2		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		2
3	SAO#12		SAO#9		SAOC#		SAO#14		SAO#1		VID[1]		PICD#0		TMS		SCNINV		TRST#		FID[1]		FID[3]		DBREQ#		PLTST#		PWROK		RESET#		INIT#		FLUSH#		NMI	3
4		VCC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VSS		4
5	SAO#5		SAO#8		SAO#4		SAO#13		NC		VID[2]		PICD#1		SCNSN		SCNCK2		TDO		VREF_S		NC		SVRFM		ZN		ZP		NC		VCC		VCC		SMI#	5
6		VSS		VSS		VSS		NC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		NC		AMD		CPR#		VSS		6
7	SAO#3		SAO#2		SAO#6				VID[4]		VID[3]		KEY				NC		NC		NC		KEY				VCC_Z		VSS_Z		KEY		NC		NC		NC	7
8		VCC		VCC		NC		NC		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		NC		NC		NC		NC		NC		8
9	SD#55		SD#54		SD#52		KEY																										NC		NC		NC	9
10		VSS		VSS		VSS		NC																							NC		VCC		VCC		VCC		10
11	SD#61		SDOC#3		SD#50		NC																								COREFB		NC		NC		NC	11
12		VCC		VCC		VCC		VCC																							VSS		VSS		VSS		VSS		12
13	SD#53		SCK#6		SD#49		NC																								COREFB#		ANLOG		PLMN2		PLMN1	13
14		VSS		VSS		VSS		VSS																							VCC		VCC		VCC		VCC		14
15	SD#63		SD#51		SDIC#3																										KEY		NC		PLBYC#		PLBYC	15
16		VCC		VCC		VCC		VCC																							VSS		VSS		VSS		VSS		16
17	SD#62		SD#60		SD#48		KEY																										NC		CLKIN#		CLKIN	17
18		VSS		VSS		VSS		VSS																							VCC		VCC		VCC		VCC		18
19	SCK#7		SD#59		SD#58		NC																								NC		NC		RCLK#		RCLK	19
20		VCC		VCC		VCC		VCC																							VSS		VSS		VSS		VSS		20
21	SD#57		SD#56		SD#36		NC																								NC		CLKFR		K7CO		K7CO#	21
22		VSS		VSS		VSS		VSS																							VCC		VCC		VCC		VCC		22
23	SD#39		SD#37		SD#46																										NC		VCCA		CNNCT		PRCRDY	23
24		VCC		VCC		VCC		VCC																							VSS		VSS		VSS		VSS		24
25	SD#35		SD#47		SCK#4		KEY																								NC		PLBYP#		NC		NC	25
26		VSS		VSS		VSS		VSS																							VCC		VCC		VCC		VCC		26
27	SD#34		SD#38		SDIC#2		NC																										NC		NC		NC	27
28		VCC		VCC		VCC		NC																							NC		VSS		VSS		VSS		28
29	SD#44		SD#45		SD#33		NC																										KEY		SAI#0		SAI#1		SAI#12	29
30		VSS		VSS		NC		NC		NC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		NC		NC		NC		VCC		VCC		30
31	SCK#5		SD#43		SD#32		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		SFILLV#		SDOV#		SAI#14	31
32		VCC		VCC		VCC		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		NC		VSS		VSS		VSS		32
33	SDOC#2		SD#42		SCK#3		SD#20		SD#19		SD#26		SD#25		SD#24		SD#7		SD#5		SDIC#0		SCK#1		SD#8		SD#10		SAI#5		SAI#2		SAIC#		SAI#8		SDINV#	33
34		VSS		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VCC		34
35	SD#40		SD#41		SD#31		SD#23		SDIC#1		SCK#2		SD#27		SD#17		SD#15		SD#4		SD#2		SD#3		SD#0		SD#14		SDOC#0		SAI#11		SAI#6		SAI#4		SAI#13	35
36		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		36
37	SD#30		SDOC#1		SD#22		SD#21		SD#29		SD#28		SD#18		SD#16		SD#6		SCK#0		SD#1		SD#12		SD#13		SD#11		SD#9		SAI#7		SAI#3		SAI#10		SAI#9	37
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	

AMD Duron™ Processor Model 3 Bottomside View

Figure 15. AMD Duron™ Processor Model 3 Pin Diagram—Bottomside View

Table 16. Pin Name Abbreviations

Abbreviation	Full Name	Pin
	A20M#	AE1
	AMD	AH6
ANLOG	ANALOG	AJ13
CLKFR	CLKFWDRST	AJ21
	CLKIN	AN17
	CLKIN#	AL17
CNNCT	CONNECT	AL23
	COREFB	AG11
	COREFB#	AG13
CPR#	CPU_PRESENCE#	AK6
	DBRDY	AA1
	DBREQ#	AA3
	FERR	AG1
	FID[0]	W1
	FID[1]	W3
	FID[2]	Y1
	FID[3]	Y3
	FLUSH#	AL3
	IGNNE#	AJ1
	INIT#	AJ3
	INTR	AL1
K7CO	K7CLKOUT	AL21
K7CO#	K7CLKOUT#	AN21
	KEY	G7
	KEY	G9
	KEY	G15
	KEY	G17
	KEY	G23
	KEY	G25
	KEY	N7
	KEY	Q7
	KEY	Y7
	KEY	AA7
	KEY	AG7
	KEY	AG9
	KEY	AG15
	KEY	AG17
	KEY	AG27
	KEY	AG29

Abbreviation	Full Name	Pin
	NC	F8
	NC	F30
	NC	G11
	NC	G13
	NC	G19
	NC	G21
	NC	G27
	NC	G29
	NC	G31
	NC	H6
	NC	H8
	NC	H10
	NC	H28
	NC	H30
	NC	H32
	NC	J5
	NC	J31
	NC	K8
	NC	K30
	NC	L31
	NC	N31
	NC	Q31
	NC	S7
	NC	S31
	NC	U7
	NC	U31
	NC	W7
	NC	W31
	NC	Y5
	NC	Y31
	NC	AA31
	NC	AC31
	NC	AD8
	NC	AD30
	NC	AE31
	NC	AF6
	NC	AF8
	NC	AF10
	NC	AF28

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	NC	AF30	PRCRDY	PROCREADY	AN23
	NC	AF32		PWROK	AE3
	NC	AG5		RESET#	AG3
	NC	AG19	RCLK	RSTCLK	AN19
	NC	AG21	RCLK#	RSTCLK#	AL19
	NC	AG23	SAI#0	SADDIN[0]#	AJ29
	NC	AG25	SAI#1	SADDIN[1]#	AL29
	NC	AG31	SAI#2	SADDIN[2]#	AG33
	NC	AH8	SAI#3	SADDIN[3]#	AJ37
	NC	AH30	SAI#4	SADDIN[4]#	AL35
	NC	AJ7	SAI#5	SADDIN[5]#	AE33
	NC	AJ9	SAI#6	SADDIN[6]#	AJ35
	NC	AJ11	SAI#7	SADDIN[7]#	AG37
	NC	AJ15	SAI#8	SADDIN[8]#	AL33
	NC	AJ17	SAI#9	SADDIN[9]#	AN37
	NC	AJ19	SAI#10	SADDIN[10]#	AL37
	NC	AJ27	SAI#11	SADDIN[11]#	AG35
	NC	AK8	SAI#12	SADDIN[12]#	AN29
	NC	AL7	SAI#13	SADDIN[13]#	AN35
	NC	AL9	SAI#14	SADDIN[14]#	AN31
	NC	AL11	SAIC#	SADDINCLK#	AJ33
	NC	AL25	SAO#0	SADDOUT[0]#	J1
	NC	AL27	SAO#1	SADDOUT[1]#	J3
	NC	AM8	SAO#2	SADDOUT[2]#	C7
	NC	AN7	SAO#3	SADDOUT[3]#	A7
	NC	AN9	SAO#4	SADDOUT[4]#	E5
	NC	AN11	SAO#5	SADDOUT[5]#	A5
	NC	AN25	SAO#6	SADDOUT[6]#	E7
	NC	AN27	SAO#7	SADDOUT[7]#	C1
	NMI	AN3	SAO#8	SADDOUT[8]#	C5
	PICCLK	N1	SAO#9	SADDOUT[9]#	C3
PICD#0	PICD[0]#	N3	SAO#10	SADDOUT[10]#	G1
PICD#1	PICD[1]#	N5	SAO#11	SADDOUT[11]#	E1
PLBYP#	PLLBYPASS#	AJ25	SAO#12	SADDOUT[12]#	A3
PLBYC	PLLBYPASSCLK	AN15	SAO#13	SADDOUT[13]#	G5
PLBYC#	PLLBYPASSCLK#	AL15	SAO#14	SADDOUT[14]#	G3
PLMN1	PLLMON1	AN13	SAOC#	SADDOUTCLK#	E3
PLMN2	PLLMON2	AL13	SCNCK1	SCANCLK1	S1
PLTST#	PLLTEST#	AC3	SCNCK2	SCANCLK2	S5

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin
SCNINV	SCANINTEVAL	S3
SCNSN	SCANSHIFTEN	Q5
SCK#0	SCHECK[0]#	U37
SCK#1	SCHECK[1]#	Y33
SCK#2	SCHECK[2]#	L35
SCK#3	SCHECK[3]#	E33
SCK#4	SCHECK[4]#	E25
SCK#5	SCHECK[5]#	A31
SCK#6	SCHECK[6]#	C13
SCK#7	SCHECK[7]#	A19
SD#0	SDATA[0]#	AA35
SD#1	SDATA[1]#	W37
SD#2	SDATA[2]#	W35
SD#3	SDATA[3]#	Y35
SD#4	SDATA[4]#	U35
SD#5	SDATA[5]#	U33
SD#6	SDATA[6]#	S37
SD#7	SDATA[7]#	S33
SD#8	SDATA[8]#	AA33
SD#9	SDATA[9]#	AE37
SD#10	SDATA[10]#	AC33
SD#11	SDATA[11]#	AC37
SD#12	SDATA[12]#	Y37
SD#13	SDATA[13]#	AA37
SD#14	SDATA[14]#	AC35
SD#15	SDATA[15]#	S35
SD#16	SDATA[16]#	Q37
SD#17	SDATA[17]#	Q35
SD#18	SDATA[18]#	N37
SD#19	SDATA[19]#	J33
SD#20	SDATA[20]#	G33
SD#21	SDATA[21]#	G37
SD#22	SDATA[22]#	E37
SD#23	SDATA[23]#	G35
SD#24	SDATA[24]#	Q33
SD#25	SDATA[25]#	N33
SD#26	SDATA[26]#	L33
SD#27	SDATA[27]#	N35
SD#28	SDATA[28]#	L37
SD#29	SDATA[29]#	J37
SD#30	SDATA[30]#	A37
SD#31	SDATA[31]#	E35
SD#32	SDATA[32]#	E31
SD#33	SDATA[33]#	E29
SD#34	SDATA[34]#	A27
SD#35	SDATA[35]#	A25
SD#36	SDATA[36]#	E21
SD#37	SDATA[37]#	C23
SD#38	SDATA[38]#	C27
SD#39	SDATA[39]#	A23
SD#40	SDATA[40]#	A35
SD#41	SDATA[41]#	C35
SD#42	SDATA[42]#	C33
SD#43	SDATA[43]#	C31
SD#44	SDATA[44]#	A29
SD#45	SDATA[45]#	C29
SD#46	SDATA[46]#	E23
SD#47	SDATA[47]#	C25
SD#48	SDATA[48]#	E17
SD#49	SDATA[49]#	E13
SD#50	SDATA[50]#	E11
SD#51	SDATA[51]#	C15
SD#52	SDATA[52]#	E9
SD#53	SDATA[53]#	A13
SD#54	SDATA[54]#	C9
SD#55	SDATA[55]#	A9
SD#56	SDATA[56]#	C21
SD#57	SDATA[57]#	A21
SD#58	SDATA[58]#	E19
SD#59	SDATA[59]#	C19
SD#60	SDATA[60]#	C17
SD#61	SDATA[61]#	A11
SD#62	SDATA[62]#	A17
SD#63	SDATA[63]#	A15
SDIC#0	SDATAINCLK[0]#	W33
SDIC#1	SDATAINCLK[1]#	J35
SDIC#2	SDATAINCLK[2]#	E27
SDIC#3	SDATAINCLK[3]#	E15

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SDINV#	SDATAINVALID#	AN33	VCC	VCC_CORE	F34
SDOC#0	SDATAOUTCLK[0]#	AE35	VCC	VCC_CORE	F36
SDOC#1	SDATAOUTCLK[1]#	C37	VCC	VCC_CORE	H2
SDOC#2	SDATAOUTCLK[2]#	A33	VCC	VCC_CORE	H4
SDOC#3	SDATAOUTCLK[3]#	C11	VCC	VCC_CORE	H12
SDOV#	SDATAOUTVALID#	AL31	VCC	VCC_CORE	H16
SFILLV#	SFILLVALID#	AJ31	VCC	VCC_CORE	H20
	SMI#	AN5	VCC	VCC_CORE	H24
STPC#	STPCLK#	AC1	VCC	VCC_CORE	K32
SVRFM	SYSVREFMODE	AA5	VCC	VCC_CORE	K34
	TCK	Q1	VCC	VCC_CORE	K36
	TDI	U1	VCC	VCC_CORE	M2
	TDO	U5	VCC	VCC_CORE	M4
	TMS	Q3	VCC	VCC_CORE	M6
	TRST#	U3	VCC	VCC_CORE	M8
VCC	VCC_CORE	B4	VCC	VCC_CORE	P30
VCC	VCC_CORE	B8	VCC	VCC_CORE	P32
VCC	VCC_CORE	B12	VCC	VCC_CORE	P34
VCC	VCC_CORE	B16	VCC	VCC_CORE	P36
VCC	VCC_CORE	B20	VCC	VCC_CORE	R2
VCC	VCC_CORE	B24	VCC	VCC_CORE	R4
VCC	VCC_CORE	B28	VCC	VCC_CORE	R6
VCC	VCC_CORE	B32	VCC	VCC_CORE	R8
VCC	VCC_CORE	B36	VCC	VCC_CORE	T30
VCC	VCC_CORE	D2	VCC	VCC_CORE	T32
VCC	VCC_CORE	D4	VCC	VCC_CORE	T34
VCC	VCC_CORE	D8	VCC	VCC_CORE	T36
VCC	VCC_CORE	D12	VCC	VCC_CORE	V2
VCC	VCC_CORE	D16	VCC	VCC_CORE	V4
VCC	VCC_CORE	D20	VCC	VCC_CORE	V6
VCC	VCC_CORE	D24	VCC	VCC_CORE	V8
VCC	VCC_CORE	D28	VCC	VCC_CORE	X30
VCC	VCC_CORE	D32	VCC	VCC_CORE	X32
VCC	VCC_CORE	F12	VCC	VCC_CORE	X34
VCC	VCC_CORE	F16	VCC	VCC_CORE	X36
VCC	VCC_CORE	F20	VCC	VCC_CORE	Z2
VCC	VCC_CORE	F24	VCC	VCC_CORE	Z4
VCC	VCC_CORE	F28	VCC	VCC_CORE	Z6
VCC	VCC_CORE	F32	VCC	VCC_CORE	Z8

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin
VCC	VCC_CORE	AB30
VCC	VCC_CORE	AB32
VCC	VCC_CORE	AB34
VCC	VCC_CORE	AB36
VCC	VCC_CORE	AD2
VCC	VCC_CORE	AD4
VCC	VCC_CORE	AD6
VCC	VCC_CORE	AF14
VCC	VCC_CORE	AF18
VCC	VCC_CORE	AF22
VCC	VCC_CORE	AF26
VCC	VCC_CORE	AF34
VCC	VCC_CORE	AF36
VCC	VCC_CORE	AH2
VCC	VCC_CORE	AH4
VCC	VCC_CORE	AH10
VCC	VCC_CORE	AH14
VCC	VCC_CORE	AH18
VCC	VCC_CORE	AH22
VCC	VCC_CORE	AH26
VCC	VCC_CORE	AK10
VCC	VCC_CORE	AK14
VCC	VCC_CORE	AK18
VCC	VCC_CORE	AK22
VCC	VCC_CORE	AK26
VCC	VCC_CORE	AK30
VCC	VCC_CORE	AK34
VCC	VCC_CORE	AK36
VCC	VCC_CORE	AJ5
VCC	VCC_CORE	AL5
VCC	VCC_CORE	AM2
VCC	VCC_CORE	AM10
VCC	VCC_CORE	AM14
VCC	VCC_CORE	AM18
VCC	VCC_CORE	AM22
VCC	VCC_CORE	AM26
VCC	VCC_CORE	AM22
VCC	VCC_CORE	AM26
VCC	VCC_CORE	AM30

Abbreviation	Full Name	Pin
VCC	VCC_CORE	AM34
	VCCA	AJ23
	VCC_Z	AC7
	VID[0]	L1
	VID[1]	L3
	VID[2]	L5
	VID[3]	L7
	VID[4]	J7
VREF_S	VREF_SYS	W5
	VSS	B2
	VSS	B6
	VSS	B10
	VSS	B14
	VSS	B18
	VSS	B22
	VSS	B26
	VSS	B30
	VSS	B34
	VSS	D6
	VSS	D10
	VSS	D14
	VSS	D18
	VSS	D22
	VSS	D26
	VSS	D30
	VSS	D34
	VSS	D36
	VSS	F2
	VSS	F4
	VSS	F6
	VSS	F10
	VSS	F14
	VSS	F18
	VSS	F22
	VSS	F26
	VSS	H14
	VSS	H18
	VSS	H22
	VSS	H26

Table 16. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin
	VSS	H34
	VSS	H36
	VSS	K2
	VSS	K4
	VSS	K6
	VSS	M30
	VSS	M32
	VSS	M34
	VSS	M36
	VSS	P2
	VSS	P4
	VSS	P6
	VSS	P8
	VSS	R30
	VSS	R32
	VSS	R34
	VSS	R36
	VSS	T2
	VSS	T4
	VSS	T6
	VSS	T8
	VSS	V30
	VSS	V32
	VSS	V34
	VSS	V36
	VSS	X2
	VSS	X4
	VSS	X6
	VSS	X8
	VSS	Z30
	VSS	Z32
	VSS	Z34
	VSS	Z36
	VSS	AB2
	VSS	AB8
	VSS	AB4
	VSS	AB6
	VSS	AD32
	VSS	AD34
	VSS	AD36
	VSS	AF2
	VSS	AF4
	VSS	AF12
	VSS	AF16
	VSS	AH12
	VSS	AH16
	VSS	AH20
	VSS	AH24
	VSS	AH28
	VSS	AH32
	VSS	AH34
	VSS	AH36
	VSS	AK2
	VSS	AK4
	VSS	AK12
	VSS	AK16
	VSS	AK20
	VSS	AK24
	VSS	AK28
	VSS	AK32
	VSS	AM4
	VSS	AM6
	VSS	AM12
	VSS	AM16
	VSS	AM20
	VSS	AM24
	VSS	AM28
	VSS	AM32
	VSS	AM36
	VSS_Z	AE7
	ZN	AC5
	ZP	AE5

10.2 Pin List

Table 17 cross-references Socket A pin location to signal name.

The "L" (Level) column shows the electrical specification for this pin. "P" indicates a push-pull mode driven by a single source. "O" indicates open-drain mode that allows devices to share the pin.

Note: *The Socket A AMD Duron Processor supports push-pull drivers. For more information, see "Push-Pull (PP) Drivers" on page 6.*

The "P" (Port) column indicates if this signal is an input (I), output (O), or bidirectional (B) signal. The "R" (Reference) column indicates if this signal should be referenced to VSS (G) or VCC_CORE (P) planes for the purpose of signal routing with respect to the current return paths.

Table 17. Cross-Reference by Pin Location

Pin	Name	Description	L	P	R
A1	No Pin	page 65	-	-	-
A3	SADDOUT[12]#		P	O	G
A5	SADDOUT[5]#		P	O	G
A7	SADDOUT[3]#		P	O	G
A9	SDATA[55]#		P	B	P
A11	SDATA[61]#		P	B	P
A13	SDATA[53]#		P	B	G
A15	SDATA[63]#		P	B	G
A17	SDATA[62]#		P	B	G
A19	SCHECK[7]#	page 66	P	B	G
A21	SDATA[57]#		P	B	G
A23	SDATA[39]#		P	B	G
A25	SDATA[35]#		P	B	P
A27	SDATA[34]#		P	B	P
A29	SDATA[44]#		P	B	G
A31	SCHECK[5]#	page 66	P	B	G
A33	SDATAOUTCLK[2]#		P	O	P
A35	SDATA[40]#		P	B	G
A37	SDATA[30]#		P	B	P
B2	VSS		-	-	-
B4	VCC_CORE		-	-	-
B6	VSS		-	-	-
B8	VCC_CORE		-	-	-
B10	VSS		-	-	-
B12	VCC_CORE		-	-	-
B14	VSS		-	-	-
B16	VCC_CORE		-	-	-
B18	VSS		-	-	-
B20	VCC_CORE		-	-	-
B22	VSS		-	-	-
B24	VCC_CORE		-	-	-
B26	VSS		-	-	-
B28	VCC_CORE		-	-	-
B30	VSS		-	-	-
B32	VCC_CORE		-	-	-
B34	VSS		-	-	-

Table 17. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
B36	VCC_CORE		-	-	-
C1	SADDOUT[7]#		P	O	G
C3	SADDOUT[9]#		P	O	G
C5	SADDOUT[8]#		P	O	G
C7	SADDOUT[2]#		P	O	G
C9	SDATA[54]#		P	B	P
C11	SDATAOUTCLK[3]#		P	O	G
C13	SCHECK[6]#	page 66	P	B	G
C15	SDATA[51]#		P	B	P
C17	SDATA[60]#		P	B	G
C19	SDATA[59]#		P	B	G
C21	SDATA[56]#		P	B	G
C23	SDATA[37]#		P	B	P
C25	SDATA[47]#		P	B	G
C27	SDATA[38]#		P	B	G
C29	SDATA[45]#		P	B	G
C31	SDATA[43]#		P	B	G
C33	SDATA[42]#		P	B	G
C35	SDATA[41]#		P	B	G
C37	SDATAOUTCLK[1]#		P	O	G
D2	VCC_CORE		-	-	-
D4	VCC_CORE		-	-	-
D6	VSS		-	-	-
D8	VCC_CORE		-	-	-
D10	VSS		-	-	-
D12	VCC_CORE		-	-	-
D14	VSS		-	-	-
D16	VCC_CORE		-	-	-
D18	VSS		-	-	-
D20	VCC_CORE		-	-	-
D22	VSS		-	-	-
D24	VCC_CORE		-	-	-
D26	VSS		-	-	-
D28	VCC_CORE		-	-	-
D30	VSS		-	-	-
D32	VCC_CORE		-	-	-
D34	VSS		-	-	-
D36	VSS		-	-	-
E1	SADDOUT[11]#		P	O	P
E3	SADDOUTCLK#		P	O	G
E5	SADDOUT[4]#		P	O	P
E7	SADDOUT[6]#		P	O	G
E9	SDATA[52]#		P	B	P
E11	SDATA[50]#		P	B	P
E13	SDATA[49]#		P	B	G
E15	SDATAINCLK[3]#		P	I	G
E17	SDATA[48]#		P	B	P
E19	SDATA[58]#		P	B	G
E21	SDATA[36]#		P	B	P
E23	SDATA[46]#		P	B	P
E25	SCHECK[4]#	page 66	P	B	P
E27	SDATAINCLK[2]#		P	I	G
E29	SDATA[33]#		P	B	P
E31	SDATA[32]#		P	B	P
E33	SCHECK[3]#	page 66	P	B	P
E35	SDATA[31]#		P	B	P
E37	SDATA[22]#		P	B	G
F2	VSS		-	-	-
F4	VSS		-	-	-
F6	VSS		-	-	-
F8	NC Pin	page 65	-	-	-
F10	VSS		-	-	-
F12	VCC_CORE		-	-	-
F14	VSS		-	-	-
F16	VCC_CORE		-	-	-
F18	VSS		-	-	-
F20	VCC_CORE		-	-	-
F22	VSS		-	-	-

Table 17. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
F24	VCC_CORE		-	-	-
F26	VSS		-	-	-
F28	VCC_CORE		-	-	-
F30	NC Pin	page 65	-	-	-
F32	VCC_CORE		-	-	-
F34	VCC_CORE		-	-	-
F36	VCC_CORE		-	-	-
G1	SADDOUT[10]#		P	O	P
G3	SADDOUT[14]#		P	O	G
G5	SADDOUT[13]#		P	O	G
G7	Key Pin	page 65	-	-	-
G9	Key Pin	page 65	-	-	-
G11	NC Pin	page 65	-	-	-
G13	NC Pin	page 65	-	-	-
G15	Key Pin	page 65	-	-	-
G17	Key Pin	page 65	-	-	-
G19	NC Pin	page 65	-	-	-
G21	NC Pin	page 65	-	-	-
G23	Key Pin	page 65	-	-	-
G25	Key Pin	page 65	-	-	-
G27	NC Pin	page 65	-	-	-
G29	NC Pin	page 65	-	-	-
G31	NC Pin	page 65	-	-	-
G33	SDATA[20]#		P	B	G
G35	SDATA[23]#		P	B	G
G37	SDATA[21]#		P	B	G
H2	VCC_CORE		-	-	-
H4	VCC_CORE		-	-	-
H6	NC Pin	page 65	-	-	-
H8	NC Pin	page 65	-	-	-
H10	NC Pin	page 65	-	-	-
H12	VCC_CORE		-	-	-
H14	VSS		-	-	-
H16	VCC_CORE		-	-	-
H18	VSS		-	-	-
H20	VCC_CORE		-	-	-
H22	VSS		-	-	-
H24	VCC_CORE		-	-	-
H26	VSS		-	-	-
H28	NC Pin	page 65	-	-	-
H30	NC Pin	page 65	-	-	-
H32	NC Pin	page 65	-	-	-
H34	VSS		-	-	-
H36	VSS		-	-	-
J1	SADDOUT[0]#	page 66	P	O	-
J3	SADDOUT[1]#	page 66	P	O	-
J5	NC Pin	page 65	-	-	-
J7	VID[4]	page 67	O	O	-
J31	NC Pin	page 65	-	-	-
J33	SDATA[19]#		P	B	G
J35	SDATAINCLK[1]#		P	I	P
J37	SDATA[29]#		P	B	P
K2	VSS		-	-	-
K4	VSS		-	-	-
K6	VSS		-	-	-
K8	NC Pin	page 65	-	-	-
K30	NC Pin	page 65	-	-	-
K32	VCC_CORE		-	-	-
K34	VCC_CORE		-	-	-
K36	VCC_CORE		-	-	-
L1	VID[0]	page 67	O	O	-
L3	VID[1]	page 67	O	O	-
L5	VID[2]	page 67	O	O	-
L7	VID[3]	page 67	O	O	-
L31	NC Pin	page 65	-	-	-
L33	SDATA[26]#		P	B	P
L35	SCHECK[2]#	page 66	P	B	G
L37	SDATA[28]#		P	B	P

Table 17. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
M2	VCC_CORE		-	-	-
M4	VCC_CORE		-	-	-
M6	VCC_CORE		-	-	-
M8	VCC_CORE		-	-	-
M30	VSS		-	-	-
M32	VSS		-	-	-
M34	VSS		-	-	-
M36	VSS		-	-	-
N1	PICCLK	page 62	O	I	-
N3	PICD#[0]	page 62	O	B	-
N5	PICD#[1]	page 62	O	B	-
N7	Key Pin	page 65	-	-	-
N31	NC Pin	page 65	-	-	-
N33	SDATA[25]#		P	B	P
N35	SDATA[27]#		P	B	P
N37	SDATA[18]#		P	B	G
P2	VSS		-	-	-
P4	VSS		-	-	-
P6	VSS		-	-	-
P8	VSS		-	-	-
P30	VCC_CORE		-	-	-
P32	VCC_CORE		-	-	-
P34	VCC_CORE		-	-	-
P36	VCC_CORE		-	-	-
Q1	TCK	page 65	P	I	-
Q3	TMS	page 65	P	I	-
Q5	SCANSHIFTEN	page 66	P	I	-
Q7	Key Pin	page 65	-	-	-
Q31	NC Pin	page 65	-	-	-
Q33	SDATA[24]#		P	B	P
Q35	SDATA[17]#		P	B	G
Q37	SDATA[16]#		P	B	G
R2	VCC_CORE		-	-	-
R4	VCC_CORE		-	-	-
R6	VCC_CORE		-	-	-
R8	VCC_CORE		-	-	-
R30	VSS		-	-	-
R32	VSS		-	-	-
R34	VSS		-	-	-
R36	VSS		-	-	-
S1	SCANCLK1	page 66	P	I	-
S3	SCANINTEVAL	page 66	P	I	-
S5	SCANCLK2	page 66	P	I	-
S7	NC Pin	page 65	-	-	-
S31	NC Pin	page 65	-	-	-
S33	SDATA[7]#		P	B	G
S35	SDATA[15]#		P	B	P
S37	SDATA[6]#		P	B	G
T2	VSS		-	-	-
T4	VSS		-	-	-
T6	VSS		-	-	-
T8	VSS		-	-	-
T30	VCC_CORE		-	-	-
T32	VCC_CORE		-	-	-
T34	VCC_CORE		-	-	-
T36	VCC_CORE		-	-	-
U1	TDI	page 65	P	I	-
U3	TRST#	page 65	P	I	-
U5	TDO	page 65	P	O	-
U7	NC Pin	page 65	-	-	-
U31	NC Pin	page 65	-	-	-
U33	SDATA[5]#		P	B	G
U35	SDATA[4]#		P	B	G
U37	SCHECK[0]#	page 66	P	B	G
V2	VCC_CORE		-	-	-
V4	VCC_CORE		-	-	-
V6	VCC_CORE		-	-	-
V8	VCC_CORE		-	-	-

Table 17. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
V30	VSS		-	-	-
V32	VSS		-	-	-
V34	VSS		-	-	-
V36	VSS		-	-	-
W1	FID[0]	page 64	O	O	-
W3	FID[1]	page 64	O	O	-
W5	VREFSYS	page 68	P	-	-
W7	NC Pin	page 65	-	-	-
W31	NC Pin	page 65	-	-	-
W33	SDATAINCLK[0]#		P	I	G
W35	SDATA[2]#		P	B	G
W37	SDATA[1]#		P	B	P
X2	VSS		-	-	-
X4	VSS		-	-	-
X6	VSS		-	-	-
X8	VSS		-	-	-
X30	VCC_CORE		-	-	-
X32	VCC_CORE		-	-	-
X34	VCC_CORE		-	-	-
X36	VCC_CORE		-	-	-
Y1	FID[2]	page 64	O	O	-
Y3	FID[3]	page 64	O	O	-
Y5	NC Pin	page 65	-	-	-
Y7	Key Pin	page 65	-	-	-
Y31	NC Pin	page 65	-	-	-
Y33	SCHECK[1]#	page 66	P	B	P
Y35	SDATA[3]#		P	B	G
Y37	SDATA[12]#		P	B	P
Z2	VCC_CORE		-	-	-
Z4	VCC_CORE		-	-	-
Z6	VCC_CORE		-	-	-
Z8	VCC_CORE		-	-	-
Z30	VSS		-	-	-
Z32	VSS		-	-	-
Z34	VSS		-	-	-
Z36	VSS		-	-	-
AA1	DBRDY	page 63	P	O	-
AA3	DBREQ#	page 63	P	I	-
AA5	SYSVREFMODE	page 67	P	I	-
AA7	Key Pin	page 65	-	-	-
AA31	NC Pin	page 65	-	-	-
AA33	SDATA[8]#		P	B	P
AA35	SDATA[0]#		P	B	G
AA37	SDATA[13]#		P	B	G
AB2	VSS		-	-	-
AB4	VSS		-	-	-
AB6	VSS		-	-	-
AB8	VSS		-	-	-
AB30	VCC_CORE		-	-	-
AB32	VCC_CORE		-	-	-
AB34	VCC_CORE		-	-	-
AB36	VCC_CORE		-	-	-
AC1	STPCLK#	page 66	P	I	-
AC3	PLLTEST#	page 66	P	I	-
AC5	ZN	page 68	P	-	-
AC7	VCC_Z	page 68	-	-	-
AC31	NC Pin	page 65	-	-	-
AC33	SDATA[10]#		P	B	P
AC35	SDATA[14]#		P	B	G
AC37	SDATA[11]#		P	B	G
AD2	VCC_CORE		-	-	-
AD4	VCC_CORE		-	-	-
AD6	VCC_CORE		-	-	-
AD8	NC Pin	page 65	-	-	-
AD30	NC Pin	page 65	-	-	-
AD32	VSS		-	-	-
AD34	VSS		-	-	-
AD36	VSS		-	-	-

Table 17. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
AE1	A20M#		P	I	-
AE3	PWROK		P	I	-
AE5	ZP	page 68	P	-	-
AE7	VSS_Z	page 68	-	-	-
AE31	NC Pin	page 65	-	-	-
AE33	SADDIN[5]#		P	I	G
AE35	SDATAOUTCLK[0]#		P	O	P
AE37	SDATA[9]#		P	B	G
AF2	VSS		-	-	-
AF4	VSS		-	-	-
AF6	NC Pin	page 65	-	-	-
AF8	NC Pin	page 65	-	-	-
AF10	NC Pin	page 65	-	-	-
AF12	VSS		-	-	-
AF14	VCC_CORE		-	-	-
AF16	VSS		-	-	-
AF18	VCC_CORE		-	-	-
AF20	VSS		-	-	-
AF22	VCC_CORE		-	-	-
AF24	VSS		-	-	-
AF26	VCC_CORE		-	-	-
AF28	NC Pin	page 65	-	-	-
AF30	NC Pin	page 65	-	-	-
AF32	NC Pin	page 65	-	-	-
AF34	VCC_CORE		-	-	-
AF36	VCC_CORE		-	-	-
AG1	FERR	page 63	P	O	-
AG3	RESET#		-	I	-
AG5	NC Pin	page 65	-	-	-
AG7	Key Pin	page 65	-	-	-
AG9	Key Pin	page 65	-	-	-
AG11	COREFB	page 63	-	-	-
AG13	COREFB#	page 63	-	-	-
AG15	Key Pin	page 65	-	-	-
AG17	Key Pin	page 65	-	-	-
AG19	NC Pin	page 65	-	-	-
AG21	NC Pin	page 65	-	-	-
AG23	NC Pin	page 65	-	-	-
AG25	NC Pin	page 65	-	-	-
AG27	Key Pin	page 65	-	-	-
AG29	Key Pin	page 65	-	-	-
AG31	NC Pin	page 65	-	-	-
AG33	SADDIN[2]#		P	I	G
AG35	SADDIN[11]#		P	I	G
AG37	SADDIN[7]#		P	I	P
AH2	VCC_CORE		-	-	-
AH4	VCC_CORE		-	-	-
AH6	AMD Pin	page 62	-	-	-
AH8	NC Pin	page 65	-	-	-
AH10	VCC_CORE		-	-	-
AH12	VSS		-	-	-
AH14	VCC_CORE		-	-	-
AH16	VSS		-	-	-
AH18	VCC_CORE		-	-	-
AH20	VSS		-	-	-
AH22	VCC_CORE		-	-	-
AH24	VSS		-	-	-
AH26	VCC_CORE		-	-	-
AH28	VSS		-	-	-
AH30	NC Pin	page 65	-	-	-
AH32	VSS		-	-	-
AH34	VSS		-	-	-
AH36	VSS		-	-	-
AJ1	IGNNE#	page 65	P	I	-
AJ3	INIT#	page 65	P	I	-
AJ5	VCC_CORE		-	-	-
AJ7	NC Pin	page 65	-	-	-
AJ9	NC Pin	page 65	-	-	-

Table 17. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
AJ11	NC Pin	page 65	-	-	-
AJ13	Analog	page 62	-	-	-
AJ15	NC Pin	page 65	-	-	-
AJ17	NC Pin	page 65	-	-	-
AJ19	NC Pin	page 65	-	-	-
AJ21	CLKFWDRST	page 62	P	I	P
AJ23	VCCA	page 67	-	-	-
AJ25	PLLBYPASS#	page 66	P	I	-
AJ27	NC Pin	page 65	-	-	-
AJ29	SADDIN[0]#	page 66	P	I	-
AJ31	SFILLVALID#		P	I	G
AJ33	SADDINCLK#		P	I	G
AJ35	SADDIN[6]#		P	I	P
AJ37	SADDIN[3]#		P	I	G
AK2	VSS		-	-	-
AK4	VSS		-	-	-
AK6	CPU_PRESENCE#	page 63	-	-	-
AK8	NC Pin	page 65	-	-	-
AK10	VCC_CORE		-	-	-
AK12	VSS		-	-	-
AK14	VCC_CORE		-	-	-
AK16	VSS		-	-	-
AK18	VCC_CORE		-	-	-
AK20	VSS		-	-	-
AK22	VCC_CORE		-	-	-
AK24	VSS		-	-	-
AK26	VCC_CORE		-	-	-
AK28	VSS		-	-	-
AK30	VCC_CORE		-	-	-
AK32	VSS		-	-	-
AK34	VCC_CORE		-	-	-
AK36	VCC_CORE		-	-	-
AL1	INTR	page 65	P	I	-
AL3	FLUSH#	page 65	P	I	-
AL5	VCC_CORE		-	-	-
AL7	NC Pin	page 65	-	-	-
AL9	NC Pin	page 65	-	-	-
AL11	NC Pin	page 65	-	-	-
AL13	PLLMON2	page 66	O	O	-
AL15	PLLBYPASSCLK#	page 66	P	I	-
AL17	CLKIN#	page 62	P	I	P
AL19	RSTCLK#	page 62	P	I	P
AL21	K7CLKOUT	page 65	P	O	-
AL23	CONNECT	page 63	P	I	P
AL25	NC Pin	page 65	-	-	-
AL27	NC Pin	page 65	-	-	-
AL29	SADDIN[1]#	page 66	P	I	-
AL31	SDATAOUTVALID#		P	O	P
AL33	SADDIN[8]#		P	I	P
AL35	SADDIN[4]#		P	I	G
AL37	SADDIN[10]#		P	I	G
AM2	VCC_CORE		-	-	-
AM4	VSS		-	-	-
AM6	VSS		-	-	-
AM8	NC Pin	page 65	-	-	-
AM10	VCC_CORE		-	-	-
AM12	VSS		-	-	-
AM14	VCC_CORE		-	-	-
AM16	VSS		-	-	-
AM18	VCC_CORE		-	-	-
AM20	VSS		-	-	-
AM22	VCC_CORE		-	-	-
AM24	VSS		-	-	-
AM26	VCC_CORE		-	-	-
AM28	VSS		-	-	-
AM30	VCC_CORE		-	-	-
AM32	VSS		-	-	-
AM34	VCC_CORE		-	-	-

Table 17. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
AM36	VSS		-	-	-
AN1	No Pin	page 65	-	-	-
AN3	NMI		P	I	-
AN5	SMI#		P	I	-
AN7	NC Pin	page 65	-	-	-
AN9	NC Pin	page 65	-	-	-
AN11	NC Pin	page 65	-	-	-
AN13	PLLMON1	page 66	O	B	-
AN15	PLLBYPASSCLK	page 66	P	I	-
AN17	CLKIN	page 62	P	I	P
AN19	RSTCLK	page 62	P	I	P
AN21	K7CLKOUT#	page 65	P	O	-
AN23	PROCRDY		P	O	P
AN25	NC Pin	page 65	-	-	-
AN27	NC Pin	page 65	-	-	-
AN29	SADDIN[12]#		P	I	G
AN31	SADDIN[14]#		P	I	G
AN33	SDATAINVALID#		P	I	P
AN35	SADDIN[13]#		P	I	G
AN37	SADDIN[9]#		P	I	G

10.3 Detailed Pin Descriptions

The information in this section pertains to Table 17 on page 54.

A20M# Pin

A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.

AMD Pin

AMD Socket A processors do not implement a pin at location AH6. All Socket A designs must have a top plate or cover that blocks this pin location. When the cover plate blocks this location, a non-AMD part (e.g., PGA370) does not fit into the socket. However, socket manufacturers are allowed to have a contact loaded in the AH6 position. Therefore, motherboard socket design should account for the possibility that a contact could be loaded in this position.

AMD Duron™ System Bus Pins

See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for information about the system bus pins—PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SCHECK[7:0]#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVALID#, SDATAOUTCLK[3:0]#, SDATAOUTVALID#, SFILLVALID#.

Analog Pin

Treat this pin as a NC.

APIC Pins, PICCLK, PICD[1:0]#

The Advanced Programmable Interrupt Controller (APIC) is a feature that provides a flexible and expandable means of delivering interrupts in a system using an AMD processor. The pins, PICD[1:0], are the bi-directional message-passing signals used for the APIC and are driven to the Southbridge or a dedicated I/O APIC. The pin, PICCLK, must be driven with a valid clock input. For more information, see Table 14, “APIC Pins AC and DC Characteristics,” on page 34.

CLKFWDRST Pin

CLKFWDRST resets clock-forward circuitry for both the system and processor.

CLKIN, RSTCLK (SYSCLK) Pins

Connect CLKIN (AN17) with RSTCLK (AN19) and name it SYSCLK. Connect CLKIN# (AL17) with RSTCLK# (AL19) and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor. See “SYSCLK and SYSCLK#” on page 66 for more information.

CONNECT Pin

CONNECT is an input from the system used for power management and clock-forward initialization at reset.

COREFB and COREFB# Pins

COREFB and COREFB# are outputs to the system that provide processor core voltage feedback to the system.

CPU_PRESENCE# Pin

CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# can be used to detect the presence or absence of a processor in the Socket A–style socket.

DBRDY and DBREQ# Pins

DBRDY (AA1) and DBREQ# (AA3) are routed to the debug connector. DBREQ# is tied to VCC_CORE with a pullup resistor.

FERR Pin

FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is an push-pull active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the "Required Circuits" chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

FID[3:0] Pins

See "Frequency Identification (FID[3:0])" on page 24 for the AC and DC characteristics for FID[3:0].

FID[3] (Y3), FID[2] (Y1), FID[1] (W3), and FID[0] (W1) are the 4-bit processor clock-to-SYSCLK ratio. Table 18 on page 64 describes the encodings of the clock multipliers on FID[3:0]

.

Table 18. FID[3:0] Clock Multiplier Encodings

FID[3]	FID[2]	FID[1]	FID[0]	Processor Clock to SYSCLK Frequency Ratio
0	0	0	0	11
0	0	0	1	11.5
0	0	1	0	12
0	0	1	1	≥ 12.5*
0	1	0	0	5
0	1	0	1	5.5
0	1	1	0	6
0	1	1	1	6.5
1	0	0	0	7
1	0	0	1	7.5
1	0	1	0	8
1	0	1	1	8.5
1	1	0	0	9
1	1	0	1	9.5
1	1	1	0	10
1	1	1	1	10.5

Note:
**All ratios greater than or equal to 12.5x have the same FID[3:0] code of 0011, which causes the SIP configuration for all ratios of 12.5x or greater to be the same.*

The FID[3:0] signals are open drain processor outputs that are pulled High on the motherboard and sampled by the Northbridge at the deassertion of RESET# to determine the SIP (serialization initialization packet) that gets sent to the processor. See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order#21902 for more information about the SIP and SIP protocol.

The processor FID[3:0] outputs are open drain and 2.5V tolerant. **To prevent damage to the processor, if these signals are pulled High to above 2.5 V, they must be electrically isolated from the processor.** For information about the FID[3:0] isolation circuit, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

FLUSH# Pin FLUSH# must be tied to VCC_CORE with a pullup resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.

IGNNE# Pin IGNNE# is an input from the system that tells the processor to ignore numeric errors.

INIT# Pin INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0FFFF FFF0h.

INTR Pin INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.

JTAG Pins TCK (Q1), TMS (Q3), TDI (U1), TRST# (U3), and TDO (U5) are the JTAG interface. Connect these pins directly to the motherboard debug connector. Pullup TDI, TCK, TMS, and TRST# to VCC_CORE with pullup resistors.

K7CLKOUT and K7CLKOUT# Pins K7CLKOUT (AL21) and K7CLKOUT# (AN21) are each run for 2 to 3 inches and then terminated with a resistor pair, 100 ohms to VCC_CORE and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and VCC_CORE/2.

Key Pins These 16 locations are for processor type keying for forwards and backwards compatibility (G7, G9, G15, G17, G23, G25, N7, Q7, Y7, AA7, AG7, AG9, AG15, AG17, AG27, and AG29). Motherboard designers should treat key pins like NC (no connect) pins. See “NC Pins” on page 65 for more information. A socket designer has the option of creating a top mold piece that allows PGA key pins only where designated. However, sockets that populate all 16 key pins must be allowed, so the motherboard must always provide for pins at all key pin locations.

NC Pins The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.

NMI Pin NMI is an input from the system that causes a non-maskable interrupt.

PGA Orientation Pins No pin is present at pin locations A1 and AN1. Motherboard designers should not allow for a PGA socket pin at these locations.

For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

PLL Bypass and Test Pins

PLLTEST# (AC3), PLLBYPASS# (AJ25), PLLMON1 (AN13), PLLMON2 (AL13), PLLBYPASSCLK (AN15), and PLLBYPASSCLK# (AL15) are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to VCC_CORE with pullup resistors.

PWROK Pin

The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification.

For more information, See "Signal and Power-Up Requirements" on page 35.

SADDIN[1:0]# and SADDOUT[1:0]# Pins

The AMD Duron Processor Model 3 does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to VCC with pullup resistors, if this bit is not supported by the Northbridge (future models can support SADDIN[1]#). SADDOUT[1:0]# are tied to VCC with pullup resistors if these pins are supported by the Northbridge. For more information, see the *AMD Athlon™ System Bus Specification*, order# 21902.

Scan Pins

SCANSHIFTEN (Q5), SCANCLK1 (S1), SCANINTEVAL (S3), and SCANCLK2 (S5) are the scan interface. This interface is AMD internal and is tied disabled with pulldown resistors to ground on the motherboard.

SCHECK[7:0]# Pin

For systems that do not support ECC, SCHECK[7:0]# should be treated as NC pins.

SMI# Pin

SMI# is an input that causes the processor to enter the system management mode.

STPCLK# Pin

STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.

SYSCLK and SYSCLK#

SYSCLK and SYSCLK# are differential input clock signals provided to the processor's PLL from a system-clock generator. See "CLKIN, RSTCLK (SYSCLK) Pins" on page 62 for more information.

SYSVREFMODE Pin

SYSVREFMODE (AA5) is Low to ensure that the external VREFSYS voltage is the actual voltage used by the input buffers and that no scaling occurs internally between the VREFSYS voltage and the input threshold. This pin is tied Low with a pulldown resistor.

VCCA Pin

VCCA is the processor PLL supply. For information about the VCCA pin, see Table 5, “VCCA AC and DC Characteristics,” on page 25 and the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

VID[4:0] Pins

The VID[4:0] (Voltage Identification) outputs are used to dictate the VCC_CORE voltage level. The VID[4:0] pins are strapped to ground or left unconnected on the processor’s package. The VID[4:0] pins are pulled-up on the motherboard and used by the VCC_CORE DC/DC converter.

These voltage ID values are defined inTable 19 on page 68.

Table 19. VID[4:0] Code to Voltage Definition

VID[4:0]	VCC_CORE (V)	VID[4:0]	VCC_CORE (V)
00000	1.850	10000	1.450
00001	1.825	10001	1.425
00010	1.800	10010	1.400
00011	1.775	10011	1.375
00100	1.750	10100	1.350
00101	1.725	10101	1.325
00110	1.700	10110	1.300
00111	1.675	10111	1.275
01000	1.650	11000	1.250
01001	1.625	11001	1.225
01010	1.600	11010	1.200
01011	1.575	11011	1.175
01100	1.550	11100	1.150
01101	1.525	11101	1.125
01110	1.500	11110	1.100
01111	1.475	11111	No CPU

For more information, see the "Required Circuits" chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

VREFSYS Pin

VREFSYS (W5) drives the threshold voltage for the system bus input receivers. The value of VREFSYS is system specific. In addition, to minimize VCC_CORE noise rejection from VREFSYS, include decoupling capacitors. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

ZN, VCC_Z, ZP, and VSS_Z Pins

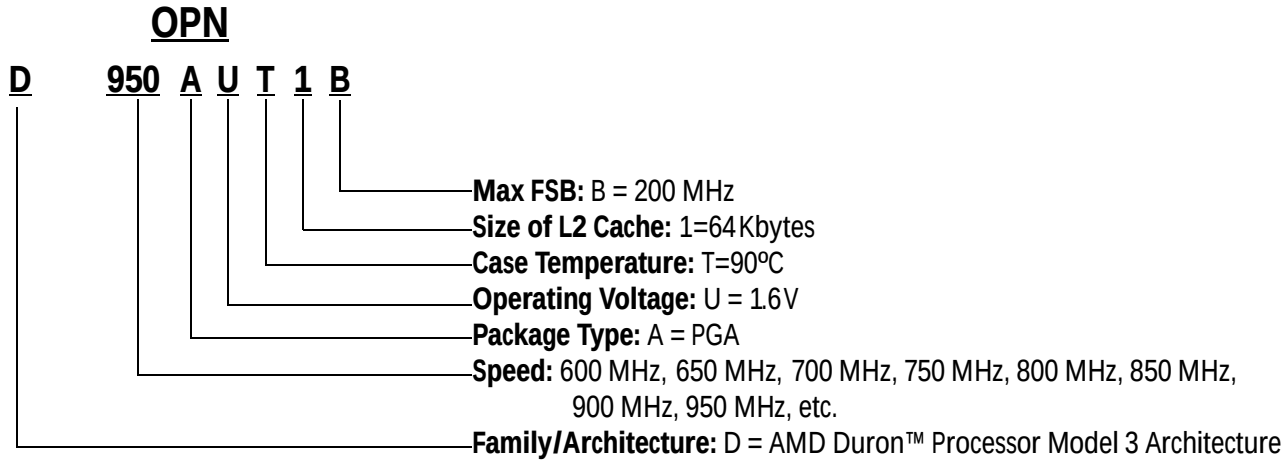
ZN (AC5), VCC_Z (AC7), ZP (AE5), and VSS_Z(AE7) are the push-pull compensation circuit pins. VCC_Z is tied to VCC_CORE. VSS_Z is tied to VSS.

In Push-Pull mode (selected by the SIP parameter SysPushPull asserted), ZN is tied to VCC_CORE with a resistor that has a resistance matching the impedance Z_0 of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance Z_0 of the transmission line.

11 Ordering Information

Standard AMD Duron™ Processor Model 3 Products

AMD standard products are available in several operating ranges. The ordering part numbers (OPN) are formed by a combination of the elements shown in Figure 16. ***These OPNs are examples only.***



Note: Spaces are added to the number shown above for viewing clarity only.

Figure 16. OPN Example for the AMD Duron™ Processor Model 3

Appendix A

Conventions, Abbreviations, and References

This section contains information about the conventions and abbreviations used in this document.

Signals and Bits

- Active-Low Signals—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- Three-State—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.

- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

  See Table 21 for more abbreviations.
- Little-Endian Convention—The byte with the address xx...xx00 is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

Abbreviations and Acronyms

Table 21 contains the definitions of abbreviations used in this document.

Table 20. Abbreviations

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga-
Gbit	Gigabit
Gbyte	Gigabyte
H	Henry
h	Hexadecimal
K	Kilo-
Kbyte	Kilobyte
M	Mega-
Mbit	Megabit
Mbyte	Megabyte
MHz	Megahertz
m	Milli-
ms	Millisecond
mW	Milliwatt
µ	Micro-
µA	Microampere
µF	Microfarad
µH	Microhenry
µs	Microsecond
µV	Microvolt
n	nano-
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond
ohm	Ohm
p	pico-
pA	picoampere

Table 20. Abbreviations (continued)

Abbreviation	Meaning
pF	picofarad
pH	picohenry
ps	picosecond
s	Second
V	Volt
W	Watt

Table 21 contains the definitions of acronyms used in this document.

Table 21. Acronyms

Abbreviation	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
ECC	Error Correcting Code
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
EV6	Digital™ Alpha™ Bus
FIFO	First In, First Out
GART	Graphics Address Remapping Table
HSTL	High-Speed Transistor Logic
IDE	Integrated Device Electronics
ISA	Industry Standard Architecture

Table 21. Acronyms (continued)

Abbreviation	Meaning
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LAN	Large Area Network
LRU	Least-Recently Used
LVTTL	Low Voltage Transistor Transistor Logic
MSB	Most Significant Bit
MTRR	Memory Type and Range Registers
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OD	Open-Drain
PBGA	Plastic Ball Grid Array
PA	Physical Address
PCI	Peripheral Component Interconnect
PDE	Page Directory Entry
PDT	Page Directory Table
PLL	Phase Locked Loop
PMSM	Power Management State Machine
POS	Power-On Suspend
POST	Power-On Self-Test
RAM	Random Access Memory
ROM	Read Only Memory
RXA	Read Acknowledge Queue
SDI	System DRAM Interface
SDRAM	Synchronous Direct Random Access Memory
SIP	Serial Initialization Packet
SMbus	System Management Bus
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory
SROM	Serial Read Only Memory
TLB	Translation Lookaside Buffer
TOM	Top of Memory
TTL	Transistor Transistor Logic
VAS	Virtual Address Space
VPA	Virtual Page Address

Table 21. Acronyms (continued)

Abbreviation	Meaning
VGA	Video Graphics Adapter
USB	Universal Serial Bus
ZDB	Zero Delay Buffer