SLUS555 – FEBRUARY 2003

9 LINE MULTIMODE SCSI PLUG AND CABLE TERMINATOR FOR SCSI–2, SPI–2 THROUGH SPI–4

FEATURES

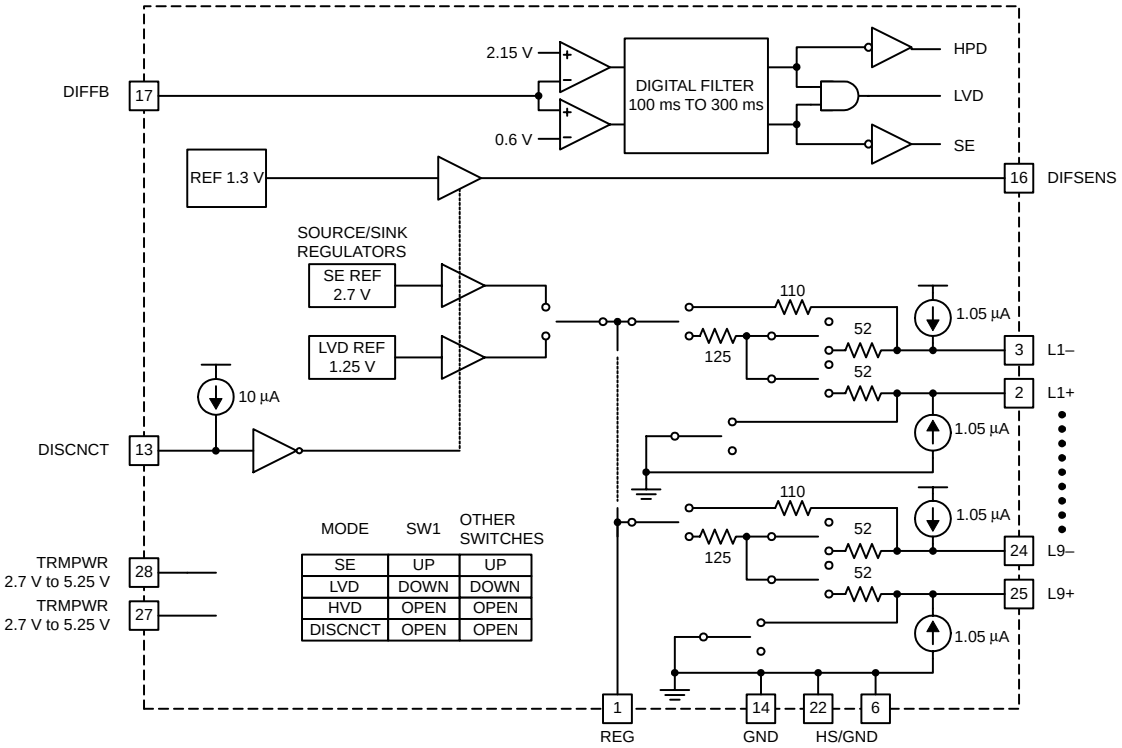
- **Meets SCSI–2, Ultra2 (SPI–2), Ultra3/Ultra160 (SPI–3), and Ultra320 (SPI–4) Standards**
- **2.7-V to 5.25-V Termpwr Operation**
- **Built in SPI–3 Delay**
- **3-pF Channel Capacitance**
- **Pin Compatible with SS–AR7519**
- **225-mA MIN Source Regulator, Supports SE With all 9 Lines Low**
- **Available in a 28-Pin (PWP) TSSOP Package**

DESCRIPTION

The UCC5519 is a multimode small computer system interface (SCSI) terminator that integrates the mode change delay function required by the SPI–3 specification. The device senses what types of SCSI drivers are present on the bus via the voltage on the DIFFSENS SCSI control line. High-voltage differential (HVD) SCSI drivers (EIA485) are not supported. If the chip detects the presence of a HVD SCSI device, it disconnects itself by switching all terminating resistors off the bus and enters a high-impedance state. The terminator can also be commanded to disconnect the terminating resistors with the DISCNCT input. Impedance is trimmed for accuracy and maximum effectiveness.

Bus lines are biased to a fail-safe state to ensure signal integrity.

BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UCC5519	UNIT
TERMPWR voltage	6	V
Signal line voltage	0 to 6	
Package power dissipation	0.5	W
Operating junction temperature, T_J	–55 to 150	°C
Storage temperature, T_{stg}	–65 to 150	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

RECOMMENDED OPERATING CONDITIONS

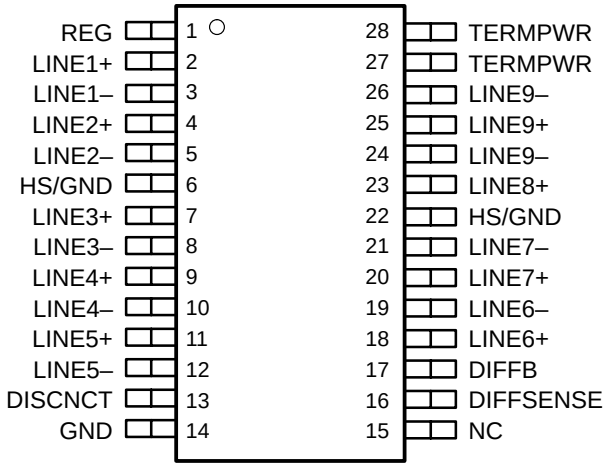
	MIN	NOM	MAX	UNIT
TERMPWR voltage	2.7		5.25	V

ORDERING INFORMATION

T_A	DISCONNECT STATUS	PACKAGED DEVICE
		TSSOP–28 (PWP)
0°C to 70°C	Regular	UCC5519PWP

† The PWP packages are available taped and reeled. Add R suffix to device type (e.g. UCC5519PWPR) to order quantities of 2,500 devices per reel.

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, TERMPWR = 2.7 V to 5.25 V, (unless otherwise specified the measurements).

TERMPWR supply current

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
TERMPWR supply current	LVD (No load)		25		mA
	SE (No Load)		15		
	Disabled terminator			2.5	
TERMPWR voltage		2.7		5.25	V

regulator

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
1.25-V regulator	LVD mode, 0.5 V _ V_{CM} _ 2.0 V, all lines loaded	1.15	1.25	1.35	V
2.7-V regulator	SE mode	2.5	2.7	3.0	
1.3-V regulator	Differential sense, —5 mA _ $I_{DIFSENSE}$ _ 50 µA	1.2	1.3	1.4	
1.25-V/2.7-V regulator source current	LVD mode, VREG = 0	–225	–420	–800	mA
1.25-V/2.7-V regulator sink current	LVD mode, VREG = 3. 3	100	180	420	
1.3-V regulator source current	Differential sense, V_{DIF} = 0 V	–5		–15	
1.3-V regulator sink current	Differential sense, V_{DIF} = 2.75 V	50		200	µA

differential termination

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Differential impedance		100	105	110	Ω
Common mode impedance	(3)	100		200	
Differential bias current		100		125	mV
Output leakage	Disabled, TERMPWR 0 < 5.25 V			400	nA
Output capacitance	Single ended measurement to ground,(1)			3	pF

NOTES: 1. Ensured by design and engineering test, but not production tested.
2. Current is the absolute value of current, as some addresses are pulled high, while others are pulled low.
3. ZCM = 1.2 V/ 1(V_{CM} +0.6) – I(V_{CM} –0.6V); Where VCM = Voltage measured with L+ tied to L– and zero current applied;
4. VLX= Output voltage for each terminator minus output pin (L1– through L9–) with each pin unloaded. ILX = Output current for each terminator minus output pin (L1– through L9–) with the minus output pin forced to 0.2V.
5. Noise on DIFFB will not cause a false mode change. The time delay is that same for a change from any mode to anyother mode. Within 300 ms after power is applied the mode is defined by the voltage of DIFFB.

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, TERMPWR = 2.7 V to 5.25 V, (unless otherwise specified the measurements).

single ended termination section

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Impedance	Z = (VLx –0.2 V)/IIx, (4)	100	108	116	Ω
Termination current	Signal level 0.2 V, all lines low	–20	–23	–25.4	mA
	Signal level 0.5 V	–17		–22.4	
Output leakage				400	nA
Output capacitance	Single ended measurement to ground(1)			3	pF
SE GND driver impedance	I = 10 mA		20	60	Ω

Disconnect (DISCNCT) and Diff Buffer (DIFFB) input section

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
DISCNT threshold		0.8		2.0	V
Input current DIFF B	0 V _ V_{DIFFB} _ 2.75 V	–1		1	µA
Input current disconnect		10		30	

time delay/filter

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Mode change delay	A new mode can start any time after a previous mode change has been detected.(5)	100	190	300	ms

status line output characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Source current	V_{LOAD} = 2.4 V		–6	–4	mA
Sink current	V_{LOAD} = 0.4 V	2	5		

NOTES: 1. Ensured by design and engineering test, but not production tested.
2. Current is the absolute value of current, as some addresses are pulled high, while others are pulled low.
3. ZCM = 1.2 V/ 1(V_{CM} +0.6) – I(V_{CM} –0.6V); Where VCM = Voltage measured with L+ tied to L– and zero current applied;
4. VLX= Output voltage for each terminator minus output pin (L1– through L9–) with each pin unloaded. ILX = Output current for each terminator minus output pin (L1– through L9–) with the minus output pin forced to 0.2V.
5. Noise on DIFFB will not cause a false mode change. The time delay is that same for a change from any mode to anyother mode. Within 300 ms after power is applied the mode is defined by the voltage of DIFFB.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DIFF SENSE	16	O	The SCSI bus DIFF SENSE line to detect what types of devices is connected to the SCSI bus.
DISCNT	13	I	Disconnect pin shuts down the terminator when it is not at the end of the bus. The disconnect pin low enables the terminator.
DIFF B	17	I	Senses the bus mode, a 50-Hz filter is required, 0.1 μF to ground and 20 kΩ to the SCSI bus DIFF SENSE line with internal SPI–3 100-ms to 300-ms delay.
HVD			High-voltage differential has been detected on the DIFF B pin; the terminator is in high impedance. (Not brought out)
Line n–		O	Negative line in differential applications for the SCSI bus.
Line n+		O	Positive line for differential applications for the SCSI bus.
LVD			Low-voltage differential level is on the DIFF B pin; the terminator is in LVD mode. (Not brought out)
REG	1	O	REG pin should be bypassed to ground with a 4.7-μF capacitor.
SE			Single ended device has been detected on the DIFF B Pin; the terminator is in high impedance. (Not brought out)
TERMPWR	27, 28		VIN 2.7-V to 5.25-V supply. TERMPWR should be bypassed to ground with a 4.7-μF capacitor.
GND	14		Signal ground
HS/GND	6, 22		This are for power dissipation and must be tied to ground and a large area of copper on 2 sided boards or to the Ground plane on multilayer boards with at least one feed through per pin with 10 mil etch going to the pins.
NC	15		No connect, other parts use this to disable the 1.3-V Diff sense drive. The circuit is wired with only one diff sense driver connected at each end. This function is not needed.

APPLICATION INFORMATION

The diff sense line is driven by the terminator and monitored by the terminator DIFF B input pin. DIFF B has a digital filter and a 100-ms to 300-ms delay before the mode of the terminator is changed to reflect the new DIFF B input level. A set of comparators that allow for ground shifts determine the bus status as any DIFF SENSE signal below 0.5 V is single ended, between 0.7 V and 1.9 V is LVD SCSI, and above 2.2 V is HVD SCSI.

The UCC5519 is high-impedance in HVD SCSI bus mode.

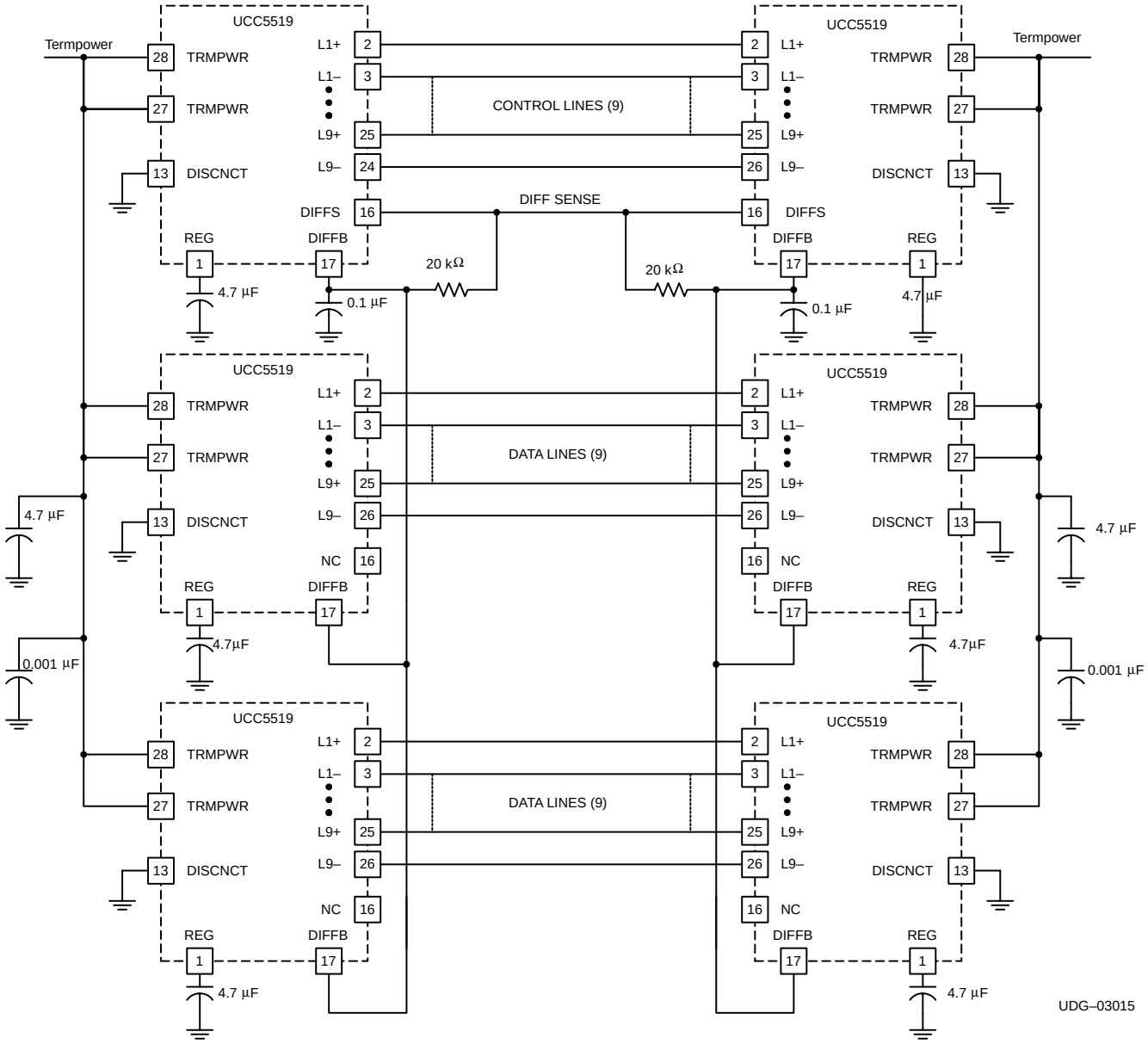
Layout is very critical for Ultra160 and Ultra320 systems. Multilayer boards need to adhere to the impedance 120-Ω standard, including connectors and feed-throughs. This is normally done on the outer layers with 4-mil etch and 4-mil spacing between the runs within a pair, and a minimum of 8-mil spacing to the next pair. The spacing between the pairs reduces potential cross-talk. Beware of feed-throughs and through-hole connectors, each of which adds a lot of capacitance. The standard power and ground plane spacing yields about 1 pF to each plane; each feed-through adds about 2.5 pF to 3.5 pF. Enlarging the clearance holes on both power and ground planes can reduce the capacitance, and opening up the power and ground planes under the connector can reduce the capacitance for through-hole connector applications. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50-Ω not 120-Ω differential systems.

Capacitance balance is critical for Ultra160 and beyond; the balance capacitance is 0.5 pF per line with the balance between pairs is 2 pF. The components are designed with very tight balance, typically 0.1 pF between pins in a pair and 0.3 pF between pairs. Layout balance is critical, feed-throughs and etch length must be balanced, and preferably no feed-throughs would be used. Capacitance for devices should be measured in the typical application. Materials and components above and below the circuit board effect the capacitance.

In 3.3-V Termpwr systems, the UCC3912 or UCC3918 should be used to replace the diode and fuse function. This reduces the voltage drop, allowing for the cable voltage drop for the terminators on the far end of the cable. 3.3-V battery systems have a 10% tolerance; the UCC3912 or UCC3918 has less than 150-mV drop under load, allowing for 150-mV drop in the cable system. All Texas Instrument LVD and multimode terminators are designed for 3.3-V systems, operating down to 2.7 V.

In 5-V Termpwr systems the UCC3916, UCC3912 or UCC3918 can be used to replace the diode and fuse function. These reduce the voltage drop and protect the systems better than the diode and fuse or polyfuse.

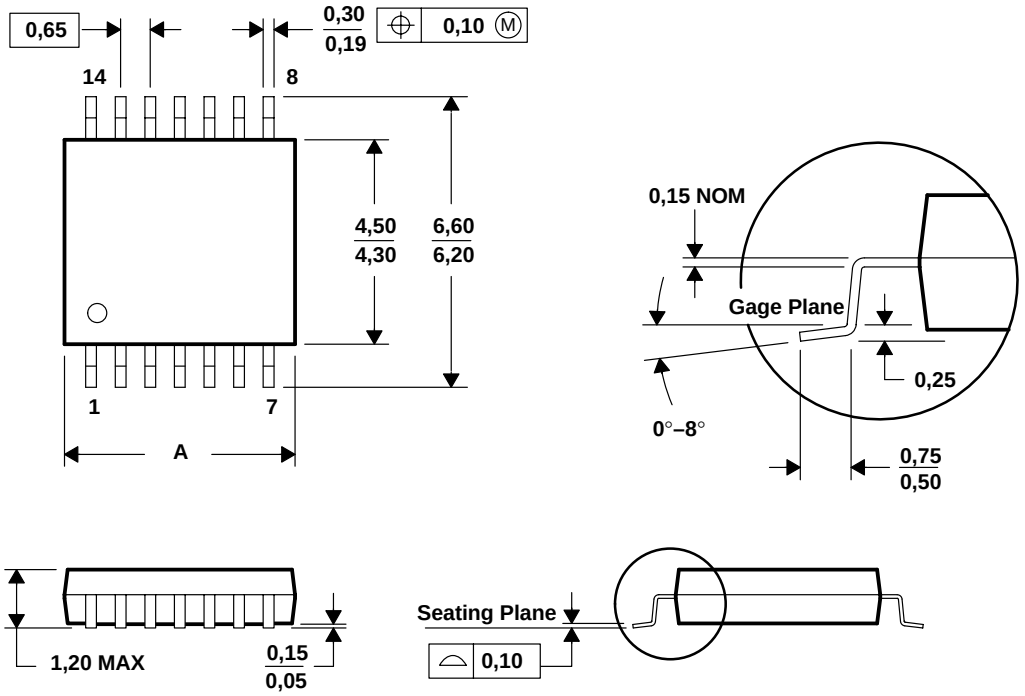
TYPICAL APPLICATION DIAGRAM



MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

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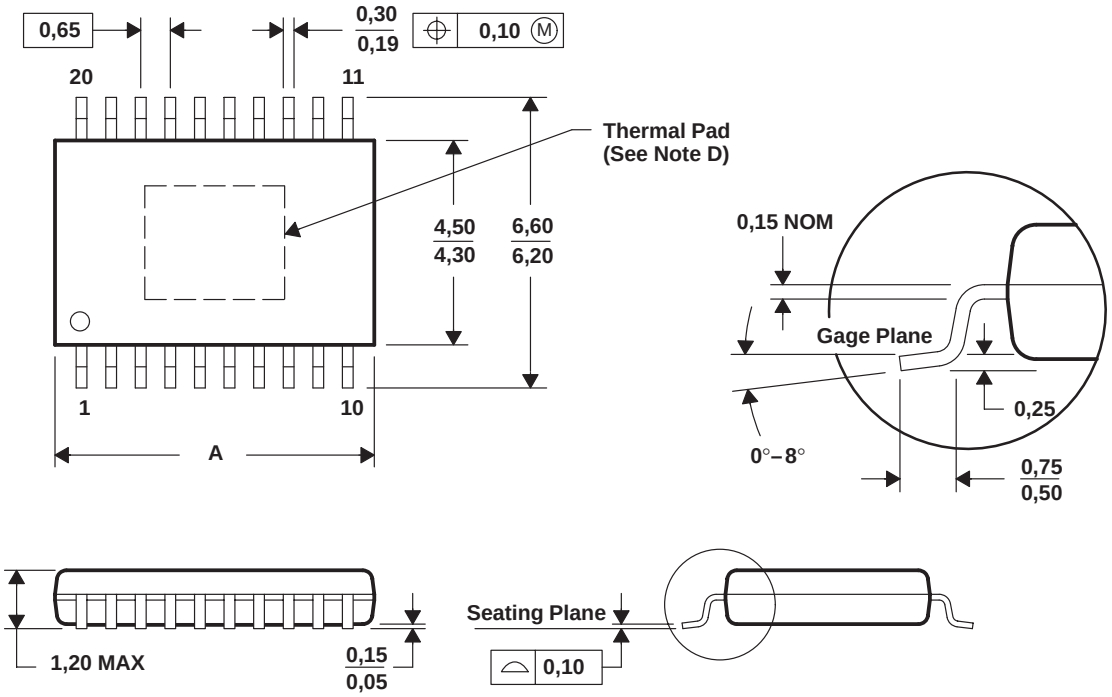
PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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