Using the TPS40180EVM, A 20A Stackable Single Phase Synchronous Buck Converter

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1 Introduction

The TPS40180EVM evaluation module (EVM) is a stackable single phase synchronous buck converter. The EVM delivers 1.5V at 20A. Each EVM is stackable with another EVM to provide higher output current. The module uses the TPS40180 Synchronous Buck Controller.

2 Description

TPS40180EVM is designed to use a regulated 10.8V to 13.2V bus to produce a high current, regulated output. The output is capable of supplying up to 20A of load current. The TPS40180EVM is designed to demonstrate the TPS40180 in a typical regulated bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40180 in a given application.

2.1 Applications

- Point of Load Converters
- Graphics Cards
- Internet Servers
- Networking Equipment
- Telecommunications Equipment
- DC Power Distributed Systems

2.2 Features

- 10.8V – 13.2V input range
- 1.5V fixed output
- 20-A DC Steady State Current
- 285kHz switching frequency per phase
- Single Main Switch N-channel MOSFET and Two Synchronous Rectifier N-channel MOSFETs per Phase
- Stackable With Another EVM to Provide Higher Output Current
- Convenient Test Points for Probing Critical Waveforms and Non-Invasive Loop Response Testing

3 TPS40180EVM Electrical Performance Specifications

Table 1. TPS40180EVM Electrical and Performance Specifications

Parameter	Notes and Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input voltage range (V_{IN})		10.8		13.2	V
Max input current	V_{IN} = 10.8 V, I_{OUT} = 20 A		3.3		A
No-load input current	V_{IN} = 13.2 V, I_{OUT} = 0A		60		mA
OUTPUT CHARACTERISTICS					
OUTPUT (V_{OUT})					
Output voltage			1.5		V
Output voltage regulation	Line Regulation (10.8 V < V_{IN} < 13.2 V, I_{OUT} = 20 A)			0.2%	
	Load Regulation (0A < I_{OUT} < 20 A, V_{IN} = 12 V)			0.2%	
Output voltage ripple	V_{IN} = 13.2 V, I_{OUT} = 20 A		20		mVpp
Output load current	I_{OUT}	0		20	A
Output over current			29		A
SYSTEM CHARACTERISTICS					
Switching Frequency			285		kHz
Peak efficiency	V_{OUT} = 1.5 V, 8A < I_{OUT} < 12A, V_{IN} = 12 V		90.1%		
Full load efficiency	V_{OUT} = 1.5 V, I_{OUT} = 20 A, V_{IN} = 12 V		88.3%		

4 Schematic

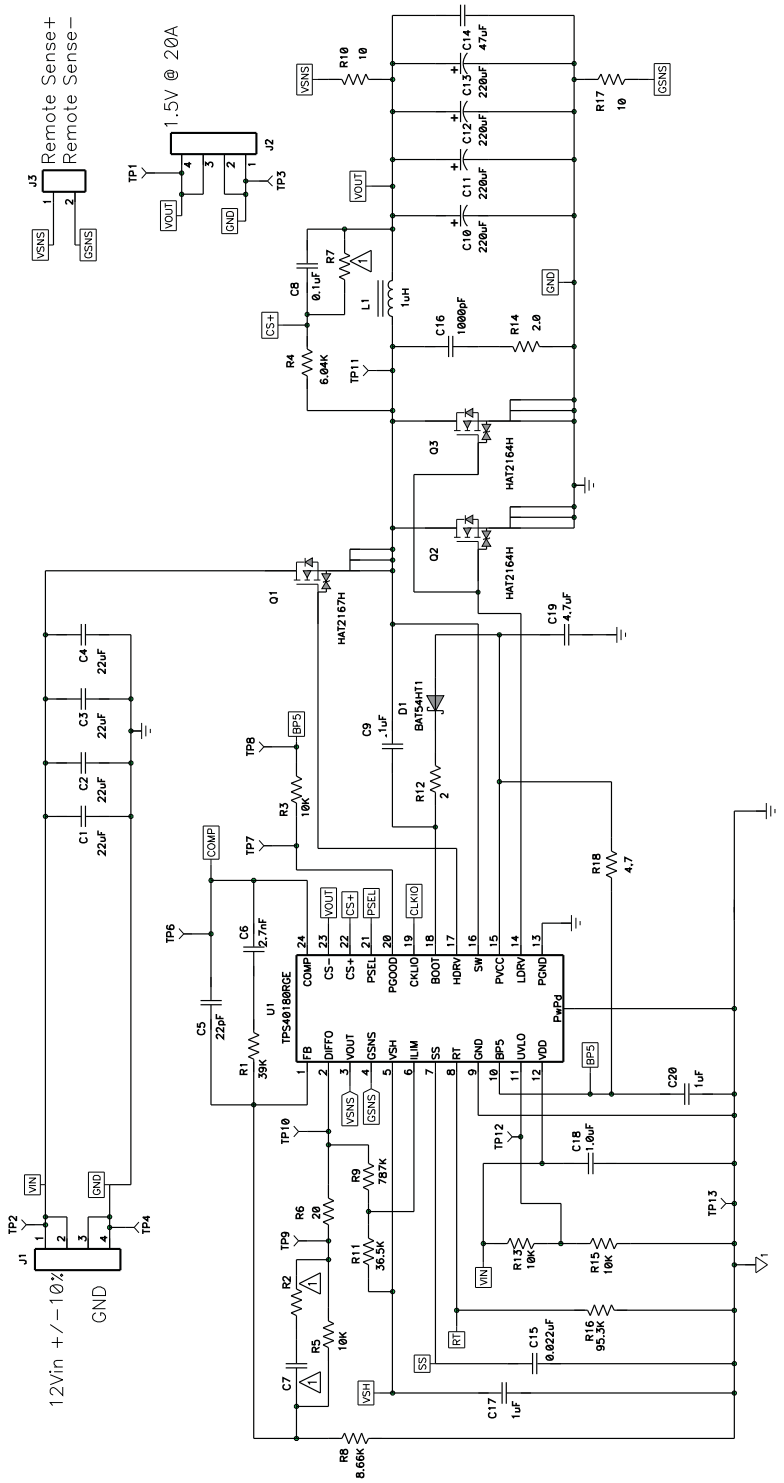


Figure 1. TPS40180EVM Power Stage/Control Schematic
For Reference Only, See Table 6: Bill of Materials for Specific Values

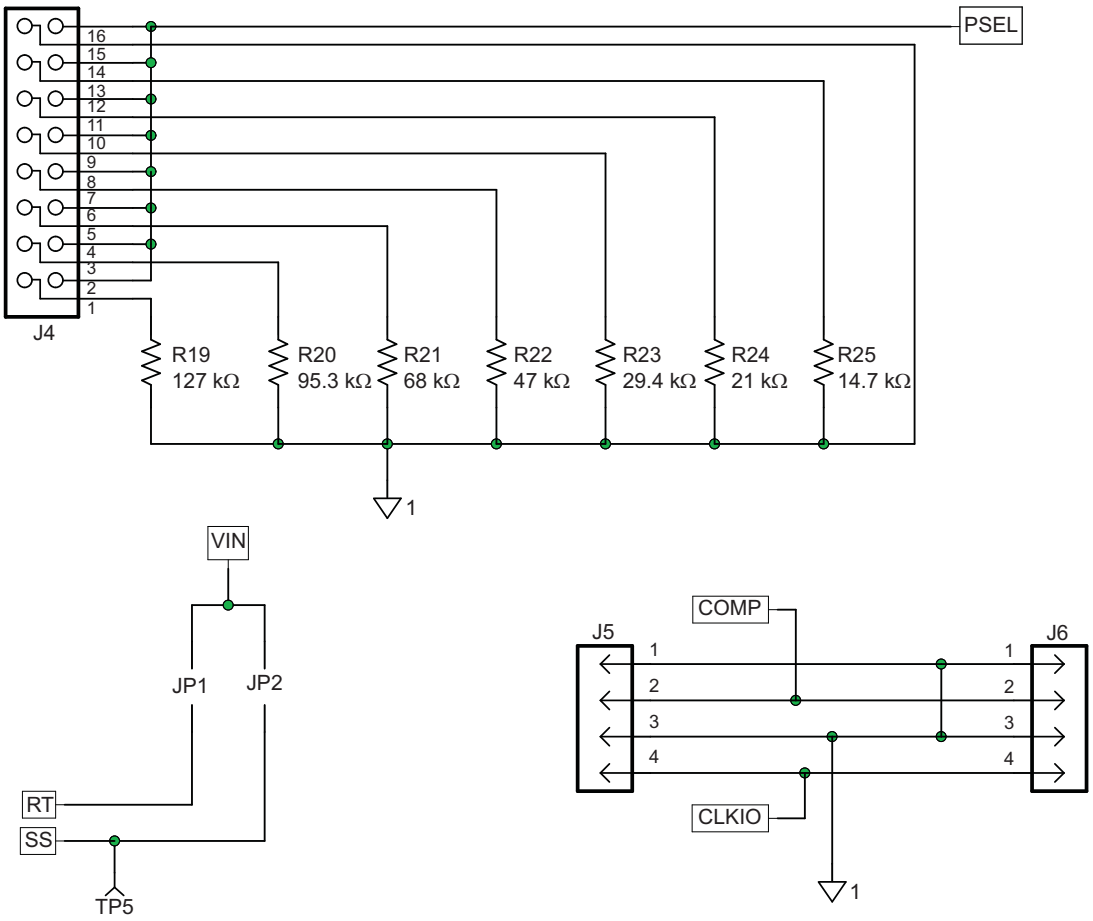


Figure 2. TPS40180EVM Configuration Schematic

5 Test Set Up

5.1 Recommended Test Equipment

5.1.1 Voltage Source

The input voltage source V_{IN} should be a 0–15 V variable DC source capable of 10 A. Connect V_{IN1} to J1 as shown in Figure 3.

The input voltage source V_{IN2} should be a 0–6 V variable DC source capable of 2 A. Connect V_{IN2} to J2 as shown in Figure 3.

5.1.2 Meters

V1: V_{IN} 0–15 V voltmeter
V2: V_{OUT} 0–5 V voltmeter
I1: I_{IN}, 0–10 A current meter

5.1.3 Loads

The output load (LOAD) should be an electronic constant current mode load capable of 0–30 A DC at 1.5 V.

5.1.4 Oscilloscope

A digital or analog oscilloscope can be used to measure the ripple voltage on V_{OUT}. The oscilloscope should be set for 1 MΩ impedance, 20MHz Bandwidth, AC coupling, 1µs/division horizontal resolution, 10mV/division vertical resolution for taking output ripple measurements. Test points TP1 and TP3 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP1 and holding the ground barrel TP3 as shown in Figure 4. Using a leaded ground connection may induce additional noise due to the large ground loop area.

5.1.5 Recommended Wire Gauge

V_{IN} to J1
The connection between the source voltage, V_{IN} and J1 of the EVM can carry as much as 5 Amps DC. The recommended wire size is 1x AWG #16 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).

J2 to LOAD (Power)
The power connection between J2 of the EVM and LOAD can carry as much as 20-A DC. The minimum recommended wire size is 2x AWG #16, with the total length of wire less than 4 feet (2 feet output, 2 feet return).

5.1.6 Other

FAN
This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200–400 lfm is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

5.2 Equipment Setup

Shown in Figure 3 is the basic test set up recommended to evaluate the TPS40180EVM.

Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.

5.2.1 Input Connections

Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 10A maximum. Make sure V_{IN} is initially set to 0V and connected as shown in Figure 3.

5.2.2 Output Connections

1. Connect LOAD to J2, set LOAD to constant current mode to sink 0A DC before V_{IN} is applied.
2. Connect voltmeter, V2, across TP1 and TP3, as shown in Figure 3.

5.2.3 Other Connections

1. Place Fan as shown in Figure 3 and turn on, making sure air is flowing across the EVM.

5.2.4 Set Up Diagram

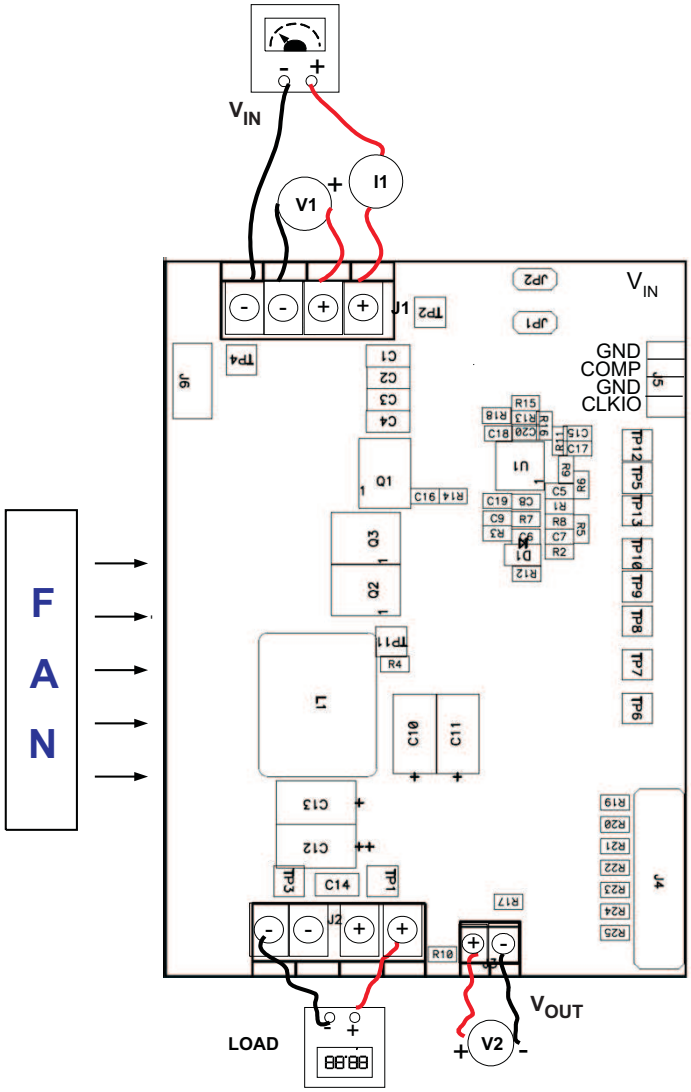
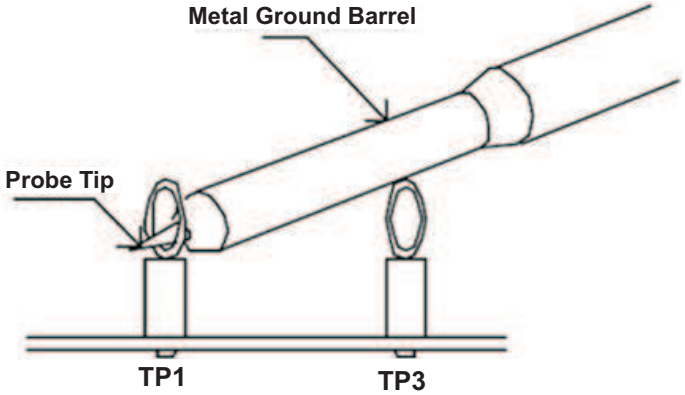


Figure 3. TPS40180EVM Recommended Test Set-Up



Tip and Barrel Output Ripple Measurement

Figure 4. Output Ripple Measurement

5.3 Start Up and Test Procedure

1. Ensure LOAD is set to constant current mode and to sink 0A DC.
2. Increase V_{IN} from 0V to 12V, V_{OUT} should be in regulation per Table 1.
3. Vary LOAD from 0–20Adc, V_{OUT} should remain in regulation per Table 1 for all combinations of load on LOAD up to 20A.
4. Vary V_{IN} from 10.8V to 13.2V, V_{OUT} should remain in regulation per Table 1 for all combinations of load on LOAD up to 20A.

5.4 Control Loop Gain and Phase Measurement Procedure

1. Connect 1 kHz–1MHz isolation transformer to test points marked TP9 and TP10.
2. Connect input signal amplitude measurement probe (channel A) to TP9.
3. Connect output signal amplitude measurement probe (channel B) to TP10.
4. Connect ground lead of channel A and channel B to TP13.
5. Inject 25mV or less signal through the isolation transformer.
6. Sweep the frequency from 100Hz to 1MHz with 10Hz or lower post filter.
7. The control loop gain can be measured by $20 \times \mathrm{LOG}\left(\frac{\mathrm{ChannelB}}{\mathrm{ChannelA}}\right)$.
8. Control loop phase is measured by the phase difference between Channel A and Channel B.
9. Disconnect isolation transformer from the bode plot test points before making other measurements (Signal Injection into Feedback may interfere with accuracy of other measurements).

5.5 Stackable EVM Configuration

5.5.1 Single Phase Operation (Default)

JP1 and JP2 are used to set master and slave configuration. J4 is used to configure the clock scheme. In default, for a single phase operation, JP1, JP2 are left open to configure the IC as a master. To configure as a slave insert jumpers on JP1 and JP2. J4 is also left open to generate an 8 phase CLKIO for interleaving with 45 degree separation. If a 6 phase CLKIO is desired, then short J4 to R23 which is 29.4kΩ.

Table 2. Master Clock Scheme Selection

J4 (PSEL Resistance to GND)	Mode	
0	No CLKIO	Single phase operation
open	8 phase CLKIO	Multi phase operation 2, 4, 8, 12, 16
29.4kΩ (R23)	6 phase CLKIO	Multi phase operation 2, 3, 6, 9, 12,15

5.5.2 Multi-Phase Operation

Here, a two phase operation is given as an example. Two identical TPS40180 EVM boards are stacked together to construct a two phase converter as shown in Figure 5. The boards are connected with J5 or J6. J5 and J6 are basically the same however located on the different side of the board. Select one EVM as the master board and configure it as shown in 5.5.1. Then use jumpers to short JP1 and JP2 to configure the other board as a slave. J4 on the slave board will determine the slave IC synchronization phase angle. Short J4 at the appropriate position to get the desired phase angle. Table 3 and Table 4 show the relationship between phase angle and PSEL resistance.

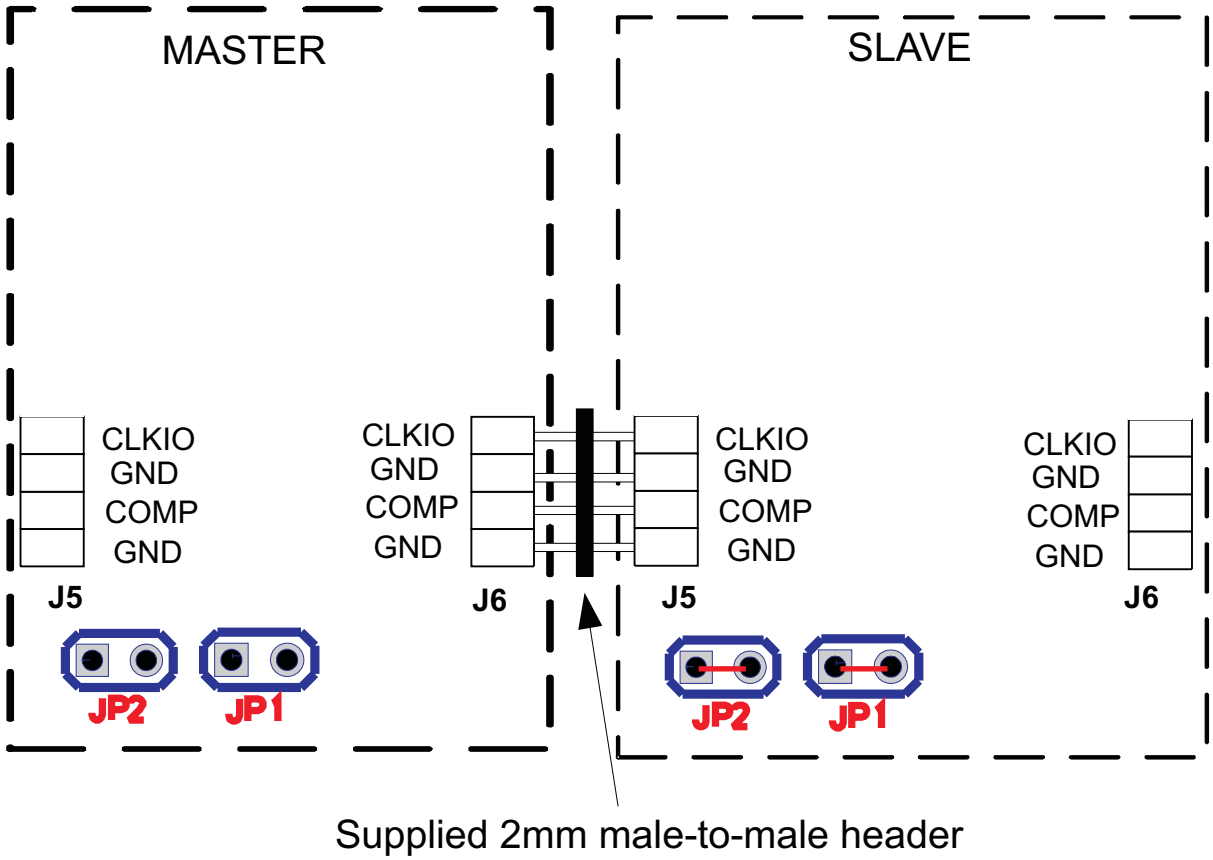


Figure 5. Master/Slave Configuration

Table 3. Slave Phase Programming With 8 Phase CLKIO

PSEL Resistor Designator	PSEL Resistance (kΩ)	Phase Angle(^{0})
Open	Open	Standby
GND	0	45
R25	14.7	90
R23	29.4	135
R22	47	180
R21	68	225
R20	95.3	270
R19	315	127

Table 4. Slave Phase Programming With 6 Phase CLKIO

PSEL Resistor Designator	PSEL Resistance (kΩ)	Phase Angle(^{0})
Open	Open	Standby
R20	95.3	0
GND	0	60
R25	14.7	120
R23	29.4	180
R22	47	240
R21	68	300

5.6 Test Points

Several test points are located around the board. These can be used to sense what is occurring at different points of the converter. Table 5 lists these test points and what they are used for.

Table 5. List of Test Points

Name	Test Point Label	Description
TP1	VOUT	Output voltage positive sense point
TP2	VIN	Input voltage positive sense point
TP3	PGND	Output voltage negative sense point
TP4	PGND	Input voltage negative sense point
TP5	SS	Soft Start
TP6	COMP	Error Amplifier Output
TP7	PGOOD	Power Good
TP8	BP5	Internal Linear Regulator Output
TP9	CHA	Loop Injection Point
TP10	CHB	Loop Injection Point
TP11	SW	Switch Node
TP12	UVLO	IC Enable Voltage
TP13	AGND	Signal Ground

5.7 Equipment Shutdown

A. Shut down LOAD
B. Shut down V_{IN}
C. Shut down FAN

6 TPS40180EVM Typical Performance Data and Characteristic Curves

Figure 6 through Figure 9 present typical performance curves for the TPS40180EVM. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

6.1 Efficiency

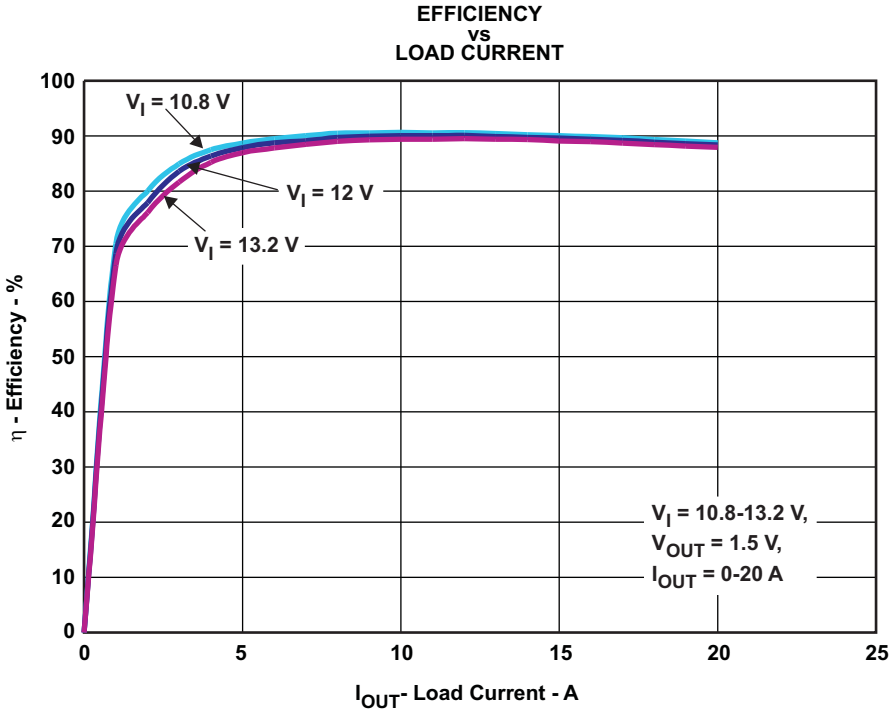


Figure 6. TPS40180EVM Efficiency

6.2 Line and Load Regulation

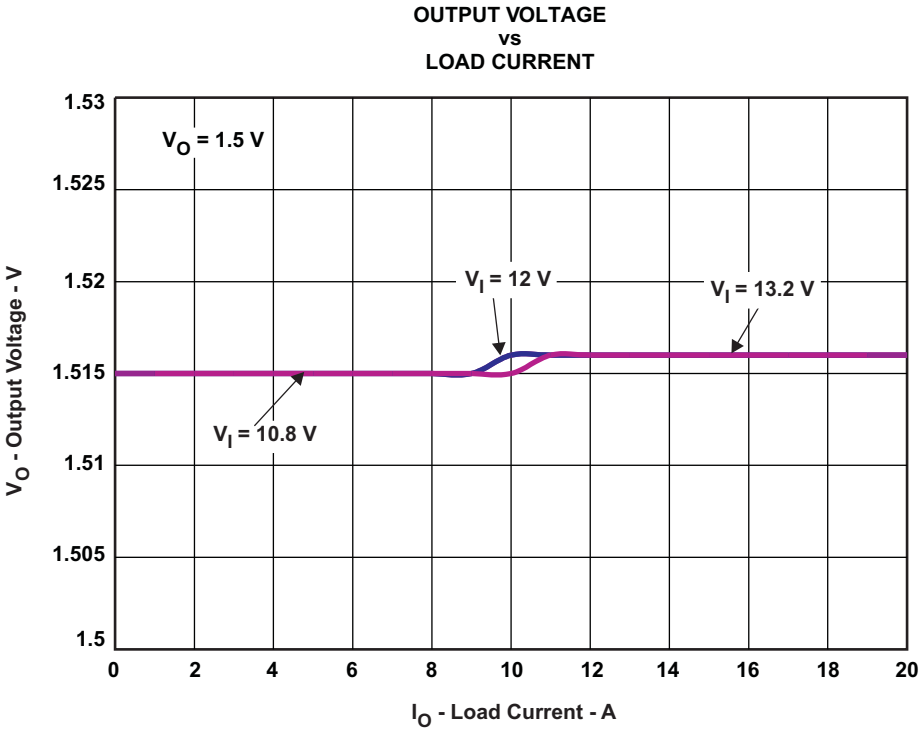


Figure 7. TPS40180EVM V_{OUT} = 1.5V Load Regulation

6.3 Bode Plot

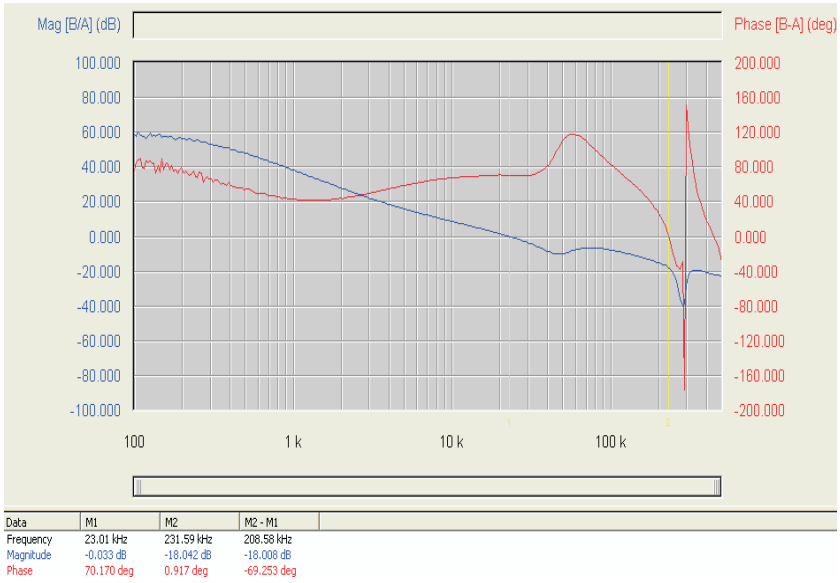


Figure 8. Loop Gain When V_{IN} = 12V and I_{OUT} = 20A, Cross Over Frequency = 23kHz, Phase Margin = 70°

6.4 Transient Response

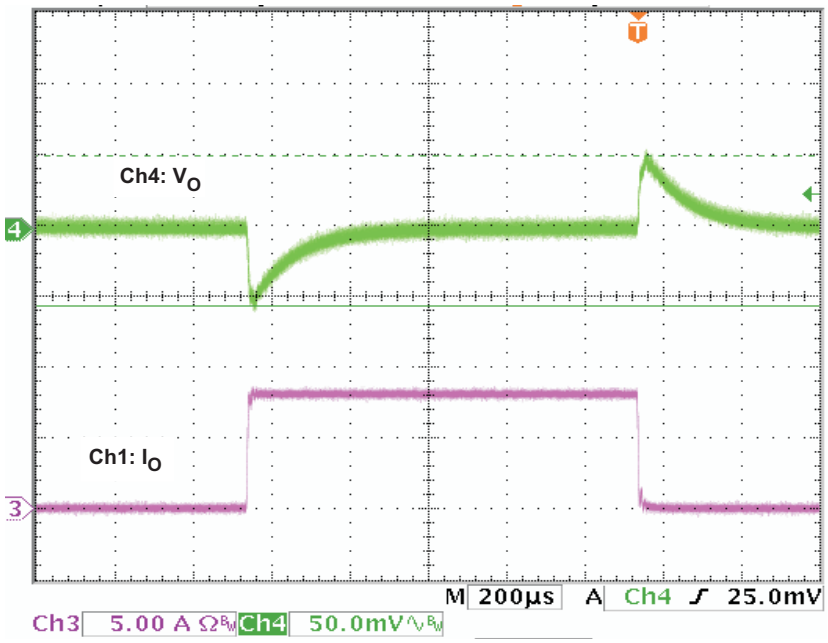


Figure 9. 0–8A Load Step, Ch1: I_{OUT} ; Ch4: V_{OUT}

7 EVM Assembly Drawings and Layout

(Figure 10 through Figure 14) show the design of the TPS40180EVM printed circuit board. The EVM has been designed using a four layer, 2-ounce, copper-clad circuit board with all components on the top side, allowing the user to easily view, probe and evaluate the TPS40180 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

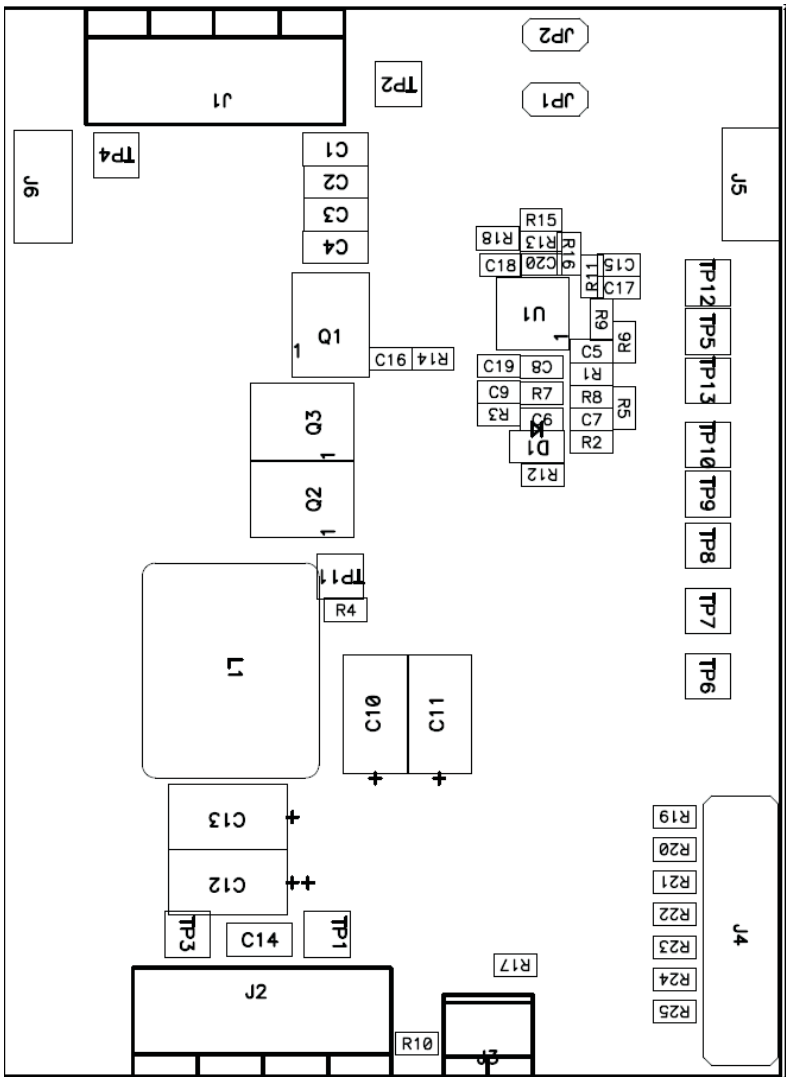


Figure 10. TPS40180EVM Component Placement (Viewed from Top)

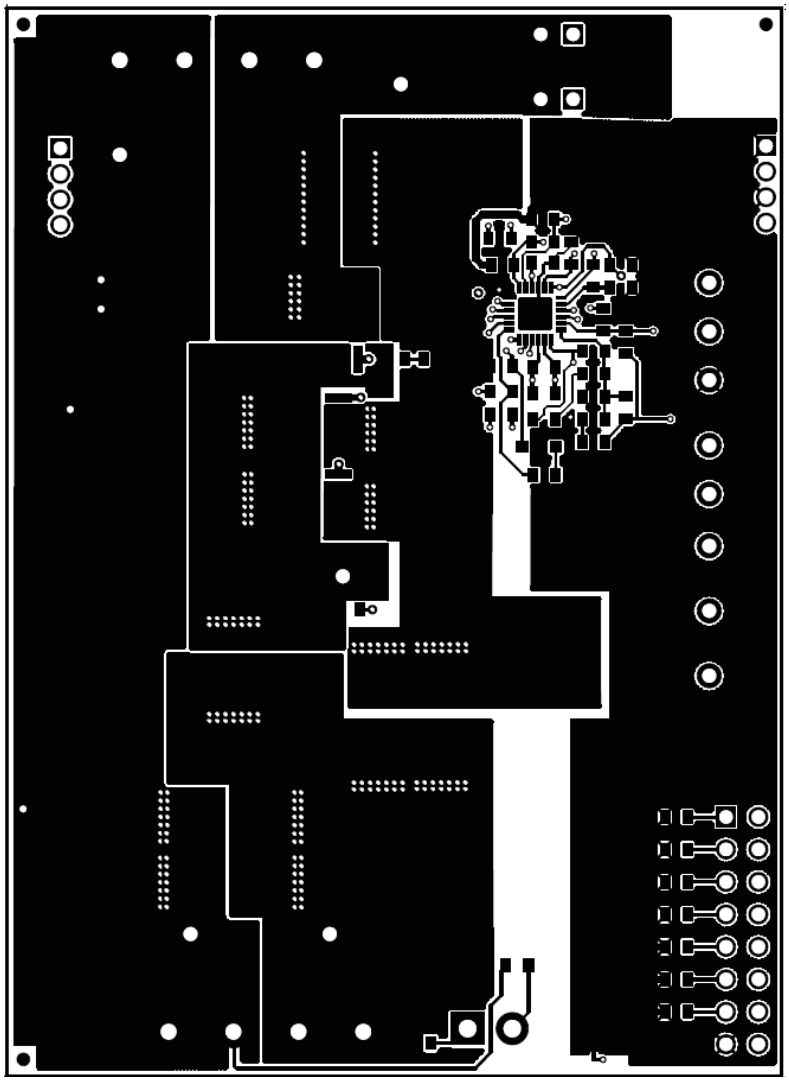


Figure 11. TPS40180EVM Top Copper (Viewed from Top)

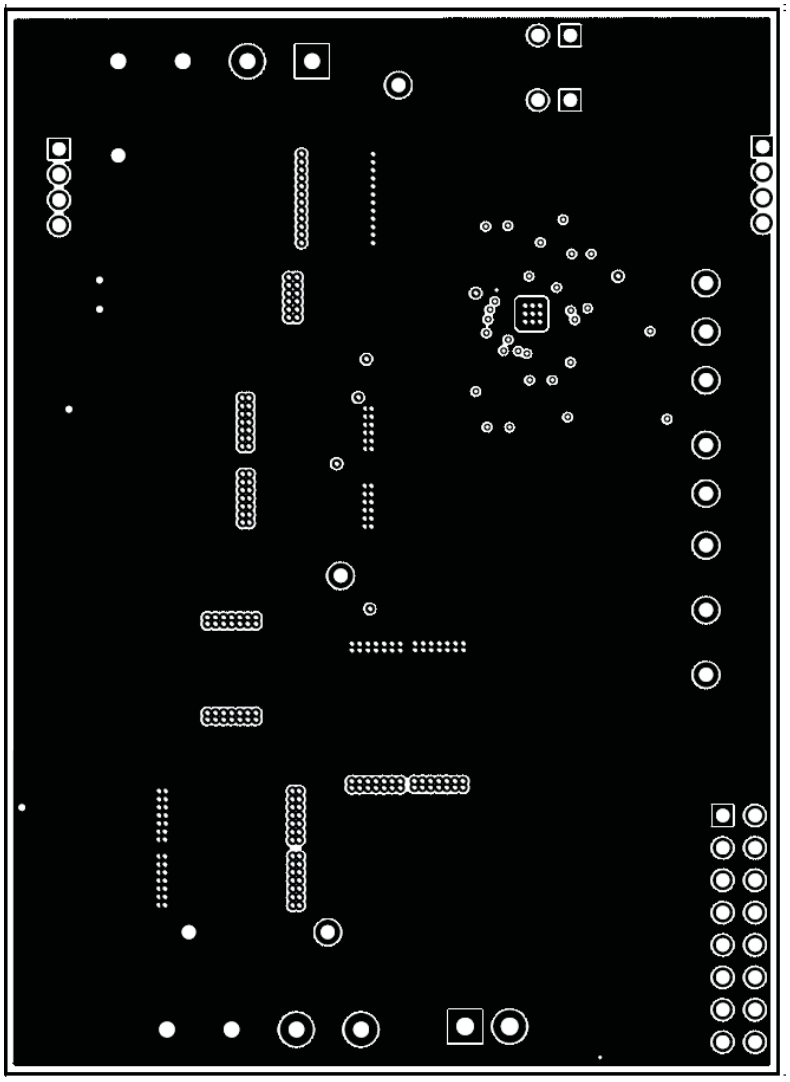


Figure 12. TPS40180EVM Layer 2 Copper (X-Ray View from Top)

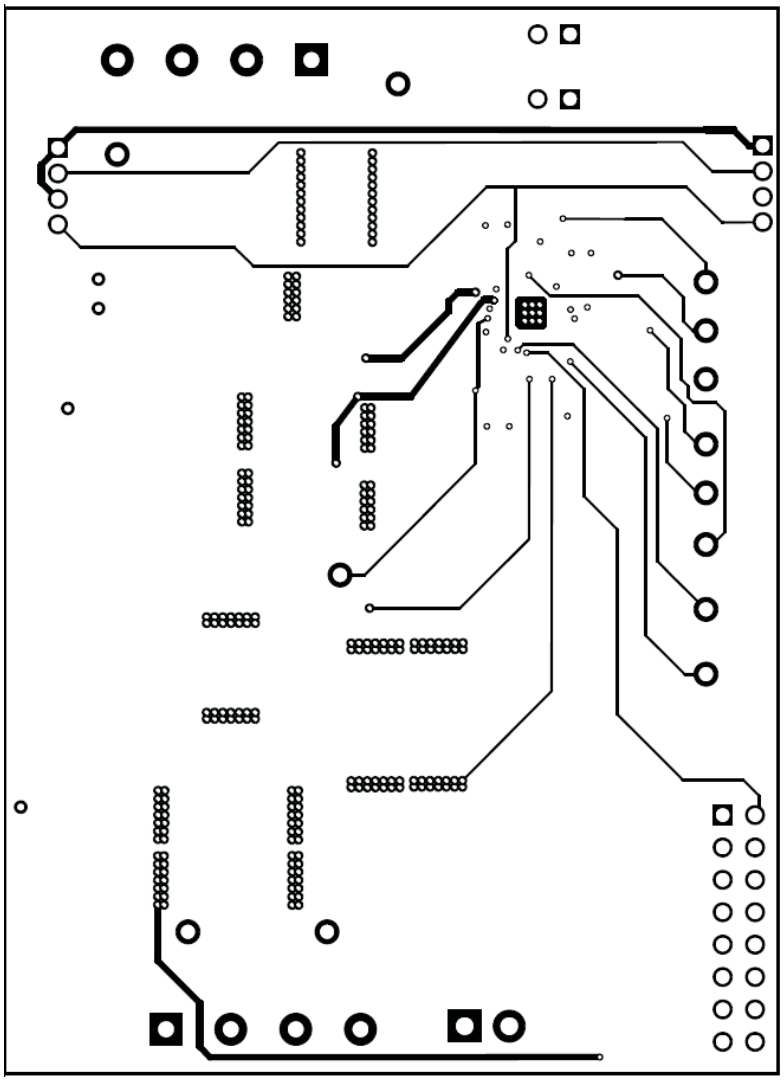


Figure 13. TPS40180EVM Layer 3 Copper (X-Ray View from Top)

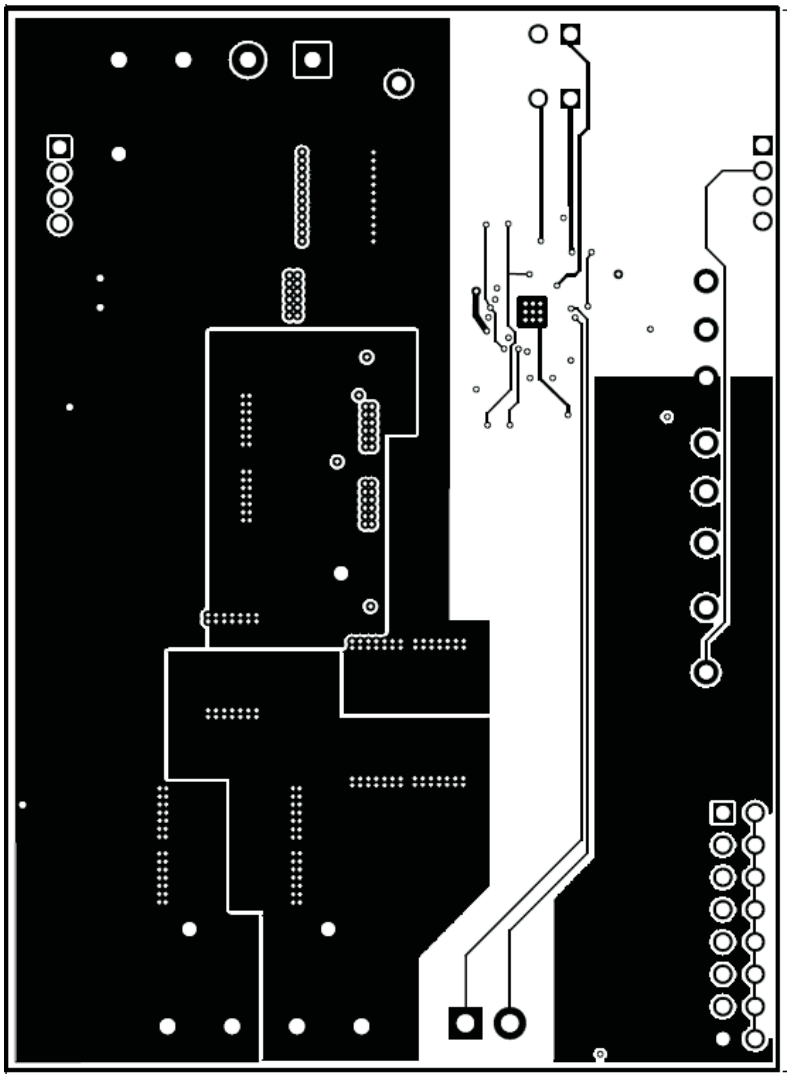


Figure 14. TPS40180EVM Bottom Copper (X-Ray View from Top)

8 List of Materials

Table 6 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 6. TPS40180EVM Bill of Materials

RefDes	Value	Description	Size	Part Number	MFR
C1–C4	22µF	Capacitor, Ceramic, 16V, X5R, 20%	1206	Std	Std
C10–C13	220µF	Capacitor, Aluminum-SE, 220-µF, 4-V, 5 mΩ	7343	EEFSE0G221R	Panasonic
C14	47µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	Std	Std
C15	0.022µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
C16	1000pF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
C17,C18,C20	1µF	Capacitor, Ceramic, 16V, X5R, 20%	0603	Std	Std
C19	4.7µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	Std	Std
C5	22pF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
C6	2.7nF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
C7	OPEN	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
C8,C9	0.1µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
D1		Diode, Schottky, 30V, 0.35Vf, SOD-323	SOD323	BAT54HT1	On Semi
J1, J2		Terminal Block, 4-pin, 15-A, 5,1mm	0.80 × 0.35	ED2227	OST
J3		Terminal Block, 2-pin, 6-A, 3.5mm	0.27 × 0.25 inch	ED1514	OST
J4		Header, 2x8 pin, 100mil spacing (36 pin strip)	0.100 inch X2X8	PTC36DAAN	Sullins
J5,J6		Conn,recept, 2mm, 4-pin Right Angle, Female (36-pin Strip)	0.079 x 4	PPPN041FGGN	Sullins
JP1, JP2		Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 inch × 2	PTC36SAAN	Sullins
L1	1µH	Inductor, SMT, 1µH	0.512 × 0.571 inch	1HLP-5050FD	Vishay
Q1		MOSFET, N-Ch, Vds 30V, Rds 4.2 mΩ, Id 40A	LFPAK	HAT2167H	Hitachi
Q2, Q3		MOSFET, N-Ch, Vds 30V, Rds 2.5 mΩ, Id 60A	LFPAK	HAT2164H	Hitachi
R1	39K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R10, R17	10	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R11	36.5K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R12, R14	2	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R16, R20	95.3K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R18	4.7	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R19	127K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R2, R7	OPEN	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R21	68K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R22	47K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R23	29.4K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R24	21K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R25	14.7K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R3, R5, R13, R15	10K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R4	6.04K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R6	20	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R8	8.66K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R9	787K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
U1		IC, Single Phase Stackable Buck Controller	QFN-24	TPS40180RGE	TI
		Jumper, 0.1", 2 contacts		2-382811-1	Tyco/ AMP

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 10.8 V to 13.2 V, and the output voltage range of 1.5 V at 20 A.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 70°C . The EVM is designed to operate properly with certain components above 70°C as long as the input and output ranges are maintained. These components include but are not limited to, switching transistors, inductor, and IC. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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