Data Sheet | July 2003 | FN9036.2

SAM (Supervisor And Monitor)

The ISL6550 is a precision, flexible, VID-code-controlled reference and voltage monitor for high-end microprocessor and memory power supplies. It monitors various input signals, and supervises the system (typically a DC/DC converter) with its output signals. See the Block Diagram for reference.

The ISL6550 includes a 5-bit DAC (Digital-to-Analog Converter), which is programmed by the five VID inputs. The voltage range of the BDAC (Buffered DAC output) is determined by the DACHI and DACLO voltage levels, which are externally adjustable through the R1, R2, R3 resistor divider network. VREF5 is a precision-trimmed 5V reference, and is used to set the voltage at the top of the resistor divider.

Programmable window comparators monitor Over-Voltage (OV) and Under-Voltage (UV) levels. The OVUVSEN input, usually coming from the associated power converter device is monitored and compared with BDAC; an error band is established via the R4 and R5 resistor setting on the OVUVTH pin. An optional external capacitor on the UVDLY pin gives a programmable delay on the UV. A high gain operational amplifier is available at pins VOPP, VOPM, and VOPOUT; it can be used as a gain stage to permit monitoring voltages that are different from the BDAC levels.

The PEN (Power supply ENable) input, driven from an open-collector source, enables (when logic high) the external converter output, via the PGOOD or START outputs (both open-drain). They both basically indicate that the power supply is enabled (PEN = high) and there are no fault conditions. There are three logic options available, which determine the START and PGOOD states; see the block diagram or the Logic Options Table for more detail. The three logic options are identified with a suffix letter A, B, or C in the ordering information.

Features

- 12V supply operation
- 5V reference output
- 5-bit digital-to-analog converter
- Programmable DAC Range, within 0.8–5.0V
- Programmable undervoltage and overvoltage thresholds, and latched fault detection
- Optional delayed undervoltage (programmable with external capacitor)
- Undervoltage lockout (power-on-reset)
- Status Indicators (START, PGOOD)
- Uncommitted operational amplifier
- Compatible with ISL6551 full bridge controller
- 20 Lead SOIC and 20 lead QFN (5x5) packages

Applications

- Power Supplies for High End Microprocessors and Servers
- Can be paired with the ISL6551 FBC for a complete full-bridge 48V-input converter, or used independently

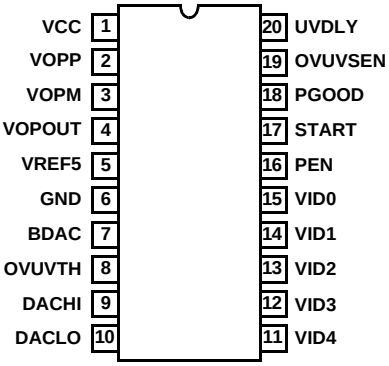
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
ISL6550AIB	-40 to 85	20 Lead SOIC	M20.3
ISL6550BIB	-40 to 85	20 Lead SOIC	M20.3
ISL6550CIB	-40 to 85	20 Lead SOIC	M20.3
ISL6550AIR	-40 to 85	20 Lead QFN	L20.5x5
ISL6550BIR	-40 to 85	20 Lead QFN	L20.5x5
ISL6550CIR	-40 to 85	20 Lead QFN	L20.5x5

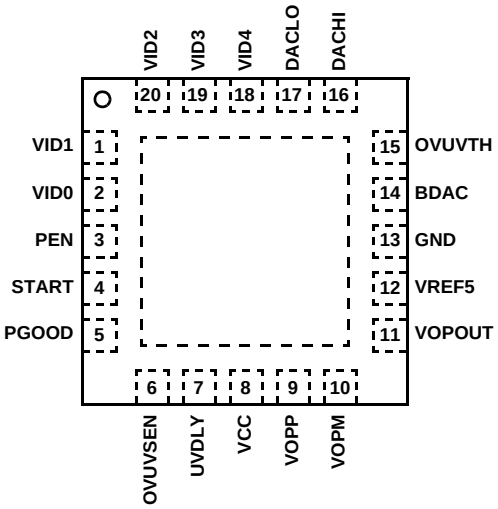
NOTE: The same part numbers with a “-T” suffix are available as Tape and Reel.

Pinout

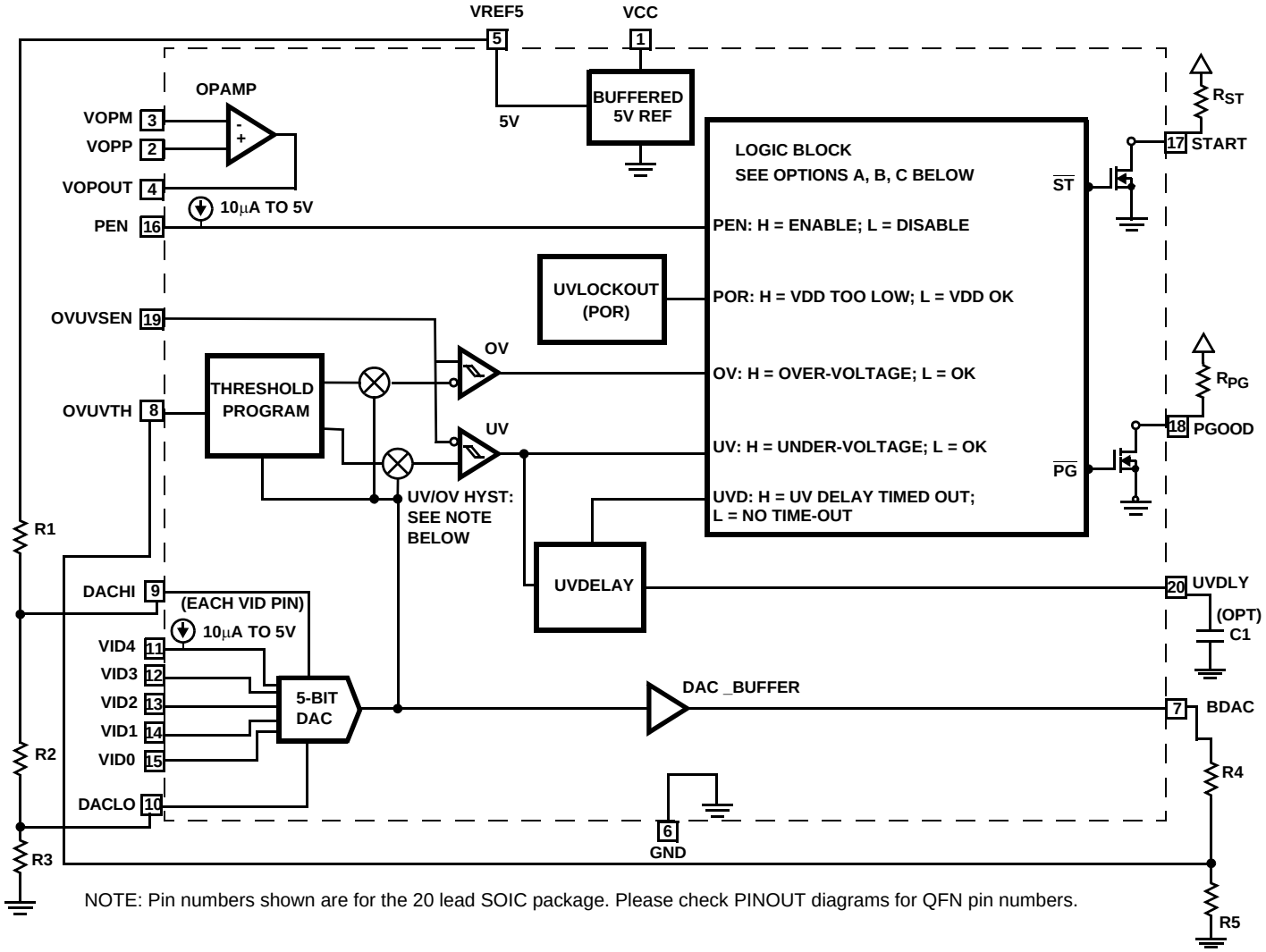
20 PIN WIDE BODY (SOIC)
TOP VIEW



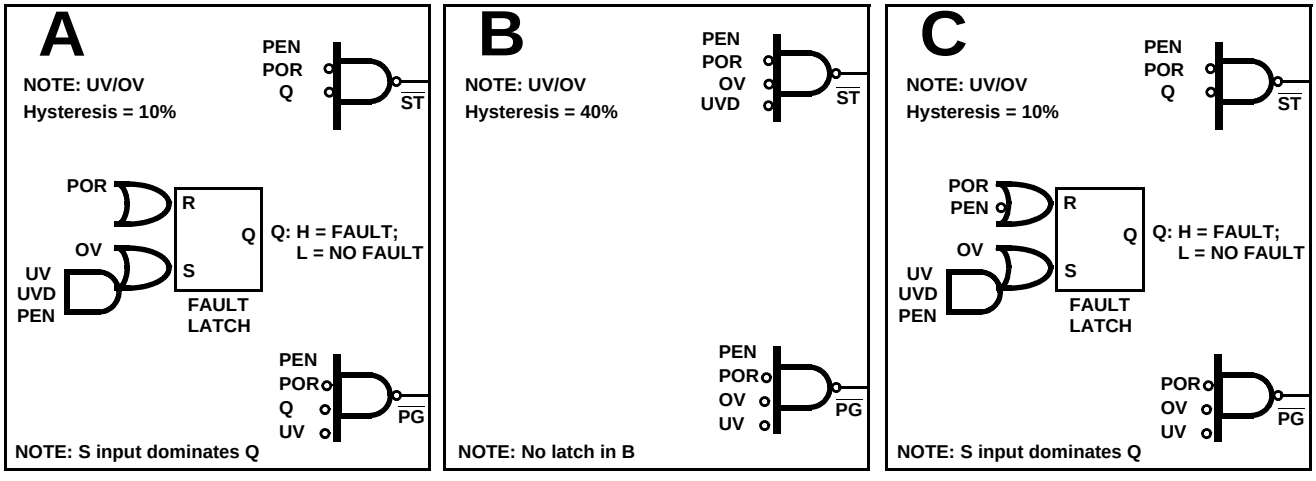
20 PIN 5X5 (QFN)
TOP VIEW



Block Diagram



NOTE: Pin numbers shown are for the 20 lead SOIC package. Please check PINOUT diagrams for QFN pin numbers.



Pin Descriptions

NOTE: Pin numbers refer to the 20 lead SOIC package. Please check PINOUT diagrams for QFN pin numbers.

VCC (Positive Supply Voltage) Pin 1 - This power pin supplies power to the IC; nominally 12V. It should be bypassed directly to the GND pin with a 0.1µF low ESR/ESL capacitor.

GND (Signal Ground) Pin 6 - This power pin is the reference ground connection for the IC, and any circuitry that provides input/output to/from it.

VID0-VID4 (DAC Digital Input Code Control) Pins 15-11 - These are the DAC digital input control code lines. VID0 represents the least significant bit (LSB) and VID4 represents the most significant bit (MSB). Table 1 shows all of the codes, and their results. Note that setting all input codes low produces the maximum voltage at BDAC. The minimum voltage results when all codes are set high. Logic zero is considered system ground. A floated input or an input held higher than 2.0V is considered a logic one level. An internal 10µA current source pulls open VID pins to a logic high (nominal 1.6V). The pins are also TTL and LVTTL compatible.

PEN (Power Supply Enable) Pin 18 - This digital input pin enables the external converter through the START or PGOOD pins. A logic high (or float) enables the output voltage, and a logic low disables it. This pin has a 10µA pull-up current source, so it can interface with an open-collector or open-drain driver. When disabled, the START output is low and the PGOOD output is low.

OVUVTH (Over-Voltage/Under-Voltage THreshold) Pin 8 - This analog input pin is used to program the window thresholds for the OV and UV comparators. The OV-UV window is centered around the BDAC voltage and can be programmed from ±5% to ±40% about the BDAC voltage. This pin's voltage sets the undervoltage threshold. Internal circuitry sets the overvoltage threshold such that the two thresholds are centered about BDAC, the DAC output voltage. For example, if BDAC is 2.5V, and OVUVTH is 2.0V (0.5V below BDAC), then the internal OV threshold is 3.0V (0.5V above BDAC).

OVUVSEN (Over-Voltage/Under-Voltage SENse) Pin 19 - This analog input pin is the sense voltage for Under-Voltage and Over-Voltage purposes. A resistor divider from the BDAC output sets the UV level, on the OVTH/UVTH pin; the IC will internally mirror a similar voltage for OV, and then compare them both to the OVUVSEN input.

DACHI (HIgh Limit of BDAC Voltage Range) Pin 9 - This analog input pin sets the high level of the BDAC, and is programmed through the external 3-resistor divider (R1, R2, R3) shown in the block diagram.

DACLO (LOw Limit of BDAC Voltage Range) Pin 10 - This analog input pin sets the low level of the BDAC, and is programmed through the external 3-resistor divider shown in the block diagram.

NOTE: A total resistance of around 50K is optimal for R1, R2, and R3. Adjust the ratios of these resistors to get the desired DACHI and DACLO voltage levels.

UVDLY (Under Voltage Delay) Pin 20 - This is an analog input/output pin. When the Under-Voltage threshold is exceeded, a potential fault is detected. A capacitor tied to the UVDLY pin is charged by an internal 10 uA source. The ramp time of the capacitor to the threshold voltage (5V nominal) determines the delay. (no capacitor gives essentially no delay).

VOPP (Positive Opamp Input) Pin 2 - This analog input pin is the positive input of the Opamp.

VOPM (Minus Opamp Input) Pin 3 - This analog input pin is the minus input of the Opamp.

VOPOUT (Opamp Output) Pin 4 - This analog output pin is the output of the Opamp.

BDAC (Buffered Digital-to-Analog Converter) Pin 7 - This analog output pin is the output of the 5-bit DAC. Setting all input codes low produces the maximum voltage at BDAC. The minimum voltage results when all codes are set high. See Table 1 for codes.

VREF5 (5 Volt Reference Voltage) Pin 5 - This is an analog output pin, which provides a precision reference voltage for setting DACHI and DACLO voltage levels.

START Pin 17 - This is an open-drain pull-down digital output pin; it is pulled low when one or more of the monitored conditions is not valid; the output goes high impedance (to be pulled high externally through a pull-up resistor or equivalent) if all conditions are met. See Logic Options Table for the various conditions.

PGOOD (Power Good) Pin 18 - This is an open-drain pull-down digital output pin; it is pulled low when one or more of the monitored conditions is not valid; the output goes high impedance (to be pulled high externally through a pull-up resistor or equivalent)) if all conditions are met. See Logic Options Table for the various conditions.

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +15V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3kV
Machine Model (Per EIAJ ED-4701 Method C-111) 200V

Operating Conditions

Supply Voltage, V_{CC} . . . . . +12V ±10%
Temperature Range . . . . . -40^oC to 85^oC
Junction Temperature Range . . . . . -40^oC to 125^oC

Thermal Information

Thermal Resistance	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SOIC Package (Typical, Note 1)	65	N/A
QFN Package (Typical, Note 2)	35	5
Maximum Junction Temperature (Plastic Package) . .		150
Maximum Storage Temperature Range		-65 to 150
Maximum Lead Temperature (Soldering 10s)		300
(SOIC - Lead Tips Only)		

For Recommended soldering conditions see Tech Brief TB389.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. θ_{JC}, the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

$T_A = 25^oC$, and VDD = 12V, unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Input Current	I_{IN}	VCC = 12V	-	5	6	mA
UNDER-VOLTAGE LOCKOUT						
V_{CC} UVLO Turn-on Threshold			9.2	9.4	9.9	-
V_{CC} UVLO Turn-off Threshold			8.2	8.4	8.9	-
V_{CC} UVLO Threshold Hysteresis			-	1.0	-	-
DAC REFERENCE						
DAC Output Error (See Notes 3, 4)		Step Size = 25mV Vdaclo = 0.8V to 4.225V Ibdac = 0.1mA to -1mA	-2	-	+2	mV
DAC Output Error (See Notes 3, 4)		Step Size = 50mV Vdaclo = 0.8V to 3.45V Ibdac = 0.1mA to -1mA	-2	-	+4	mV
DAC Output Error (See Notes 3, 4)		Step Size = 100mV Vdaclo = 0.8V to 1.9V Ibdac = 0.1mA to -1mA	-2	-	+6	mV
VREF5 Voltage			4.95	-	5.05	V
VID0-VID4 Input LPUL (Vih)			2.0	-	-	V
VID0-VID4 Input MPDL (Vil)			-	-	0.8	V
VID0-VID4 Input Pull-Up Current		Vvidx = 0V	-15	-10	-	mA
VID0-VID4 Input Leakage Current		Vvidx = 5V	-	-	1	µA
Output Settling Time		±1LSB Error Band	-	-	20	µS
UVDLY						
Source Current			-	-10	-	µA
Sink Current			-	10	-	mA
Threshold			-	5	-	V

Electrical Specifications $T_A = 25^oC$, and VDD = 12V, unless otherwise specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE AMPLIFIER						
Input Offset Voltage		All Conditions	-	-	3.0	mV
Input Bias Current		All Conditions	-	-	200	nA
Input Offset Current		All Conditions	-	20	50	nA
Open Loop Gain		All Conditions	85	-	-	dB
Common-Mode Rejection Ratio		Vin ranges from 0V to 6V	80	-	-	dB
Power Supply Rejection Ratio		1mA Load	90	-	-	dB
Output		2mA source or 0.2mA sink	0.15	-	5	V
Maximum output current source		All	-2	-7	-	mA
Maximum output current sink		All	0.2	4	-	mA
Slew Rate		All	4	-	-	v/µS
Phase Margin		100pF load Condition	-	45	-	deg
Input Common Mode Voltage			0	-	6	V
Gain-Bandwidth Product		All	7.4	-	-	MHz
MONITOR CIRCUITRY						
Input Common Mode Range		OV, UV Comparators	0	-	6	V
Propagation Delay		OV, UV Comparators	-	-	1.0	µS
PGOOD, START Outputs						
PGOOD Voltage Low		IPGOOD = 5.0mA	-	0.27	0.4	V
START Voltage Low		ISTART = 5.0mA	-	0.21	0.4	V
Transistor Breakdown Voltage		All Conditions	15	-	-	V
Transistor Leakage		All Conditions	-	-	5	µA
PEN						
Input LPUL (Vih)			2	-	-	V
Input MPDL (Vil)			-	-	0.8	V
Input Pull-Up Current		PEN = 0V	-15	-10	-	µA
Input Leakage Current		PEN = 5V	-	-	1	µA
OV/UV						
UV and OV Threshold Hysteresis		% of (Vbdac-Vovuvth); logic option B	-	40	-	%
UV and OV Threshold Hysteresis		% of (Vbdac-Vovuvth); logic options A, C	-	10	-	%

NOTES:

3. The total resistance of R1 + R2 + R3 of 50kΩ is preferred to minimize error due to DACHI and DACLO input currents. Choose the values within this limitation such that the voltages at DACHI and DACLO are those desired for the high and low limits of the programming range. For example, Choosing R1 and R2 to be 15K and R3 to be 20K will produce a DAC range of 2.0V to 3.5V.
4. DAC Output Error as defined here assumes that the voltages applied to DACHI and DACLO are exact. The limits include errors introduced by source impedance up to 12.5K and DACHI and DACLO. The error in Vdachi and Vdaclo (i.e. VREF5 error + external resistor divider error) must be included to arrive at the total BDAC output error.

TABLE 1. DIGITAL-TO-ANALOG (DAC) PROGRAMMING CODE

VID4	VID3	VID2	VID1	VID0	DACOUT Vstep = (Vdachi-Vdaclo)/31
1	1	1	1	1	Vdaclo
1	1	1	1	0	Vdaclo + 1*Vstep
1	1	1	0	1	Vdaclo + 2*Vstep
1	1	1	0	0	Vdaclo + 3*Vstep
1	1	0	1	1	Vdaclo + 4*Vstep
1	1	0	1	0	Vdaclo + 5*Vstep
1	1	0	0	1	Vdaclo + 6*Vstep
1	1	0	0	0	Vdaclo + 7*Vstep
1	0	1	1	1	Vdaclo + 8*Vstep
1	0	1	1	0	Vdaclo + 9*Vstep
1	0	1	0	1	Vdaclo + 10*Vstep
1	0	1	0	0	Vdaclo + 11*Vstep
1	0	0	1	1	Vdaclo + 12*Vstep
1	0	0	1	0	Vdaclo + 13*Vstep
1	0	0	0	1	Vdaclo + 14*Vstep
1	0	0	0	0	Vdaclo + 15*Vstep
0	1	1	1	1	Vdaclo + 16*Vstep
0	1	1	1	0	Vdaclo + 17*Vstep
0	1	1	0	1	Vdaclo + 18*Vstep
0	1	1	0	0	Vdaclo + 19*Vstep
0	1	0	1	1	Vdaclo + 20*Vstep
0	1	0	1	0	Vdaclo + 21*Vstep
0	1	0	0	1	Vdaclo + 22*Vstep
0	1	0	0	0	Vdaclo + 23*Vstep
0	0	1	1	1	Vdaclo + 24*Vstep
0	0	1	1	0	Vdaclo + 25*Vstep
0	0	1	0	1	Vdaclo + 26*Vstep
0	0	1	0	0	Vdaclo + 27*Vstep
0	0	0	1	1	Vdaclo + 28*Vstep
0	0	0	1	0	Vdaclo + 29*Vstep
0	0	0	0	1	Vdaclo + 30*Vstep
0	0	0	0	0	Vdaclo + 31*Vstep = Vdachi

Logic Options

OPTION DEFINITIONS	A	B	C
START Pin: PEN input is high AND VCC is above the UVLO threshold AND	X	X	X
OV condition does not exist AND UVDLY condition does not exist.		X	
Fault Latch is not set.	X		X
PGOOD Pin: VCC is above the UVLO threshold AND UV condition does not exist AND	X	X	X
OV condition does not exist AND		X	X
PEN input is high AND	X	X	
Fault latch is not set.	X		
Fault Latch Set by: OV condition OR UVDLY condition (UV has persisted past the UVDLY time-out)	X	(Fault Latch not used)	X
Fault Latch Reset by: OV condition does not exist AND UVDLY condition does not exist AND VCC below UVLO threshold OR	X	(Fault Latch not used)	X
PEN input low			X
OVUV Detection: UV detect threshold = Vovuvth (voltage at OVUVTH pin) OV detect threshold = Vbdac + (Vbdac - Vovuvth)	X	X	X
UV and OV threshold hysteresis = 10% of (Vbdac - Vovuvth)	X		X
UV and OV threshold hysteresis = 40% of (Vbdac - Vovuvth)		X	

Applications Information

Here are some step-by-step guidelines to help set up a circuit. Use the block diagram for reference.

1. Use a 12V (±10%) Power Supply; connect to VCC and GND. Connect a 0.1μF bypass capacitor across the pins.
2. Determine the minimum and maximum DAC values required. VREF5 is a precision 5V buffered output; connect R1, R2, R3 as a divider, to select the upper and lower range for the DAC. A total of 50kΩ for the 3 resistors is recommended. The maximum for DACHI is 5.0V; the minimum for DACLO is 0.8V. The difference between DACHI and DACLO, divided by 31, determines the step size of the DAC.

   DACLO = (5V) * (R3)/(R1 + R2 + R3)

   DACHI = (5V) * (R3 + R2)/(R1 + R2 + R3)

   STEP = (DACHI - DACLO) / 31

   For example, if R1 is 24K, R2 is 16K, and R3 is 10K, then DACLO = 1.0V, DACHI = 2.6V, and STEP = 0.05V
3. Within the above range, select the VID code for the desired BDAC output voltage. (This is typically used as a reference for a DC/DC converter system). Connect the VID bits accordingly (GND is a logic low; open/floating or 2V and above is a logic high).
4. Now that BDAC is set up as the desired reference voltage, the next step is to decide how far from this voltage the system voltage (typically the DC/DC converter output) is allowed to go, before shutting down the system. Select R4 and R5 to create the Under-Voltage threshold. R4 + R5 should total around 50kΩ, so as not to load the BDAC.

   OVUVTH = BDAC * (R5) / (R4 + R5).

   The threshold is a percentage of whatever the BDAC voltage is. If we define delta = (BDAC - OVUVTH), then the SAM will take that voltage, and mirror it up, to create an internal Over-Voltage trip point of BDAC + delta, which is the same voltage above the BDAC that the UV trip point is below BDAC (the trip points are symmetrical by design). For example, if BDAC is 2.5V, R5 is 40K, and R4 is 10K, then OVUVTH = 2.0V. Since the UV threshold is 0.5V below BDAC, the internal OV threshold will be 0.5V above BDAC, or 3.0V. So, if during normal operation, the converter output voltage is pulled past either trip point, the START and PGOOD signals will change state, and can be used to shut down the converter. Note that there is also hysteresis for both trip points; it varies with each logic option; see Logic Options Table.

   If an opamp is needed to help condition or filter the input signal at OVUVSEN, the spare one can be used. It can also be used to change the gain, if the voltage to be compared is not equal to the BDAC voltage. And if the opamp is not needed here, it can still be used for any other purpose.

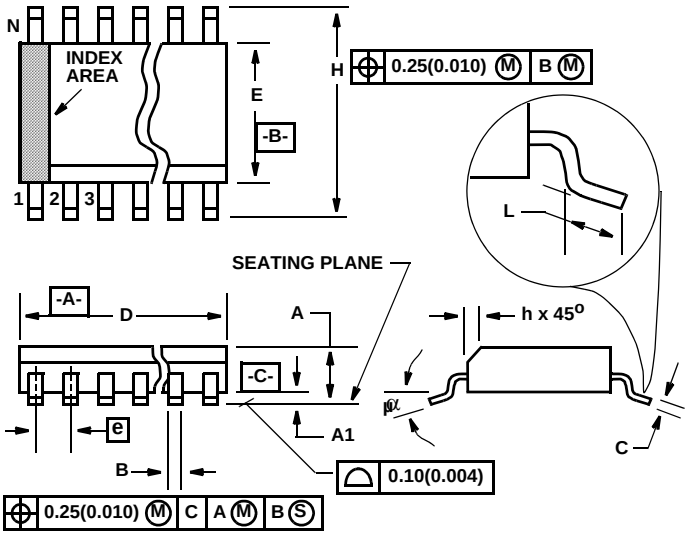
   There is an optional Under-Voltage Delay circuit. This allows the system to ignore an excursion below the UV trip point for a short time period (for example, during a power-up sequence). When the UV trip point is exceeded, an external capacitor (C1 to GND) on the UVDLY pin gets charged through an internal 20μA current source. If the OVUVSEN input is still below the trip point when the UVDLY pin reaches a nominal 5V, it will make the internal UVD signal a logic high, and the START or PGOOD will react accordingly.

   The delay time dt uses the formula I = C * dv/dt. In this case, dt = C1 * 5V/20μA. Or solve for C1 = (20μA) * (dt)/5V. Practical values for C range from 100pF (for 25μs) up to 0.1μF (for 25ms).
5. There is an UVLO (Under-Voltage Lock-Out); also called POR (Power-On-Reset), so as not to be confused with the Under-Voltage detection. This block monitors the VDD voltage; it releases around 9.4V as the power supply turns on, and has about 1.0V of hysteresis. This block only affects the START and PGOOD outputs.
6. The Logic block takes the various input and internal conditions (PEN, UV, OV, UVDLY, POR), and combines them logically to create the START and PGOOD outputs. These pins require some kind of external pull-up resistor (or equivalent); the pull-ups can be to the 12V supply, or any lower voltage compatible with the external logic. The value of the resistors depend on the pull-up voltage, the current desired, the logic voltage levels, rise or fall time considerations, etc.; A typical value would be 5kΩ. The FAULT latch is set by a combination of input conditions; it is reset by POR or PEN (see Logic Options).

   The advantage of the latch is that a momentary fault can be saved, and the user must do something (power down or toggle PEN) to recover. But some users might call that same scenario a disadvantage. So there are three different logic options to choose from. Which one is best? Which logic signals should you use?

   It depends upon what's available in the system. The PEN input is useful, for example, because it can reset the FAULT latch of the C version; the A version requires the user to power down to reset. But does the system have a signal available to do that function? The B version doesn't use a latch; if a fault condition occurs, the START and PGOOD will reflect the change; but if the fault goes away, the outputs can potentially recover on their own. So part of the choice among the logic options is whether the system is smart enough to diagnose and correct a problem, or does it just shut everything down, and wait for help.

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)

20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

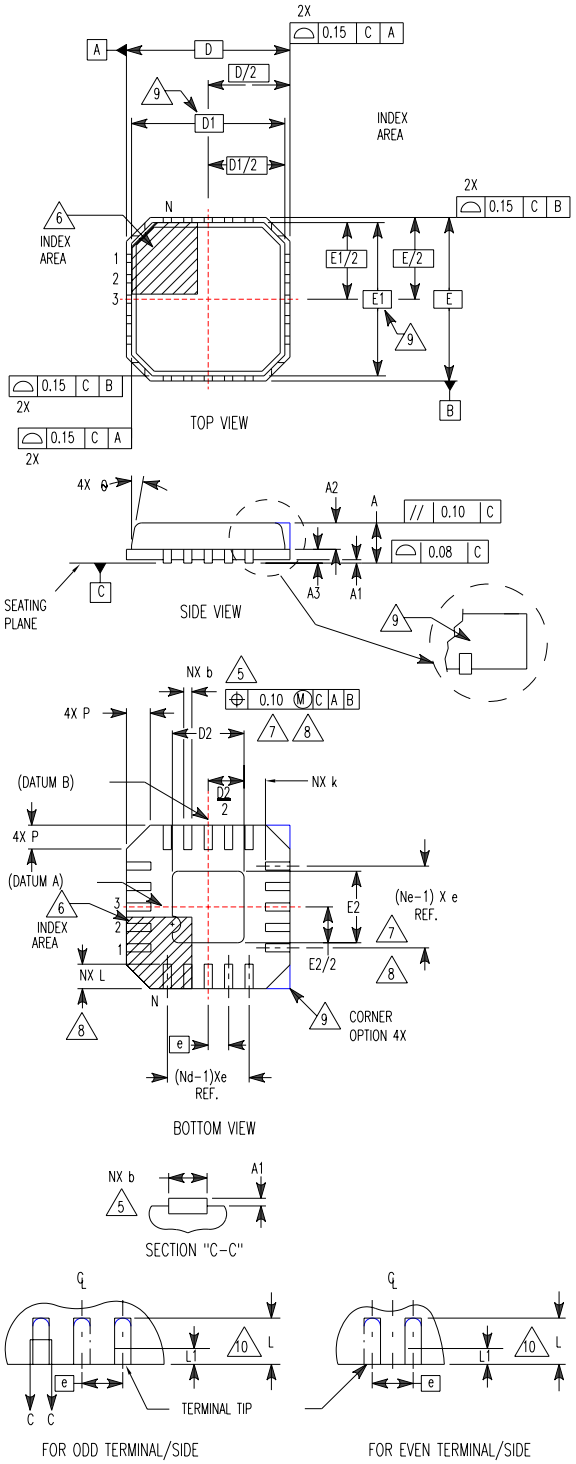
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.014	0.019	0.35	0.49	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

Rev. 1 1/02

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.5x5

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.38	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		20		2
Nd		5		3
Ne		5		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.