12A µModule Regulators with PLL, Output Tracking and Margining

FEATURES

- **Complete Switch Mode Power Supply**
- **Wide Input Voltage Range: 4.5V to 20V**
- **12A DC Typical, 14A Peak Output Current**
- **0.6V to 5V Output Voltage**
- **Output Voltage Tracking and Margining**
- **Redundant Mounting Pads for Enhanced Solder-Joint Strength**
- **Parallel Multiple µModules for Current Sharing**
- **Differential Remote Sensing for Precision Regulation (LTM4601A Only)**
- **PLL Frequency Synchronization**
- **±1.5% Total DC Error**
- **Current Foldback Protection (Disabled at Start-Up)**
- Pb-Free RoHS Compliant Package
  Gold Finish LGA (e4) or SAC 305 BGA (e1)
- UltraFast™ Transient Response
- Current Mode Control
- Up to 95% Efficiency at $5V_{IN}$, $3.3V_{OUT}$
- Programmable Soft-Start
- Output Overvoltage Protection
- Enhanced (15mm × 15mm × 2.82mm) Surface Mount LGA and (15mm × 15mm × 3.42mm) BGA Packages

APPLICATIONS

- Telecom and Networking Equipment
- Servers

DESCRIPTION

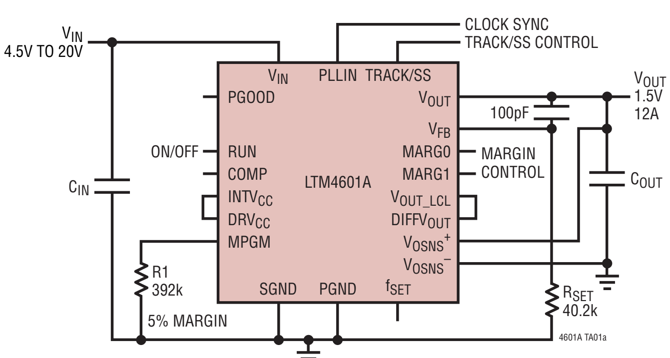
The LTM®4601A is a complete 12A step-down switch mode DC/DC power supply with onboard switching controller, MOSFETs, inductor and all support components. The µModule® regulator is housed in a small surface mount 15mm × 15mm × 2.82mm LGA or 15mm × 15mm × 3.42mm BGA package. The LTM4601A LGA and BGA packages are designed with redundant mounting pads to enhance solder-joint strength for extended temperature cycling endurance. Operating over an input voltage range of 4.5V to 20V, the LTM4601A supports an output voltage range of 0.6V to 5V as well as output voltage tracking and margining. The high efficiency design delivers 12A continuous current (14A peak). Only bulk input and output capacitors are needed to complete the design.

The low profile and light weight package easily mounts on the back side of PC boards. The µModule regulator can be synchronized with an external clock for reducing undesirable frequency harmonics and allows PolyPhase® operation for high load currents.

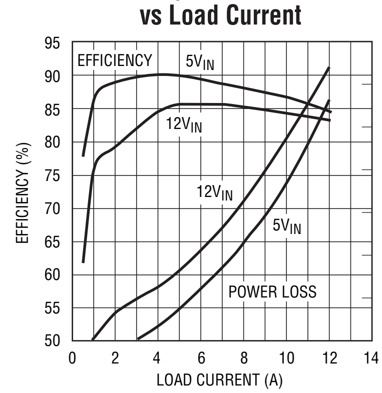
An onboard differential remote sense amplifier can be used to accurately regulate an output voltage independent of load current. The onboard remote sense amplifier is not available in the LTM4601A-1.

TYPICAL APPLICATION

1.5V/12A Power Supply with 4.5V to 20V Input



Efficiency and Power Loss vs Load Current



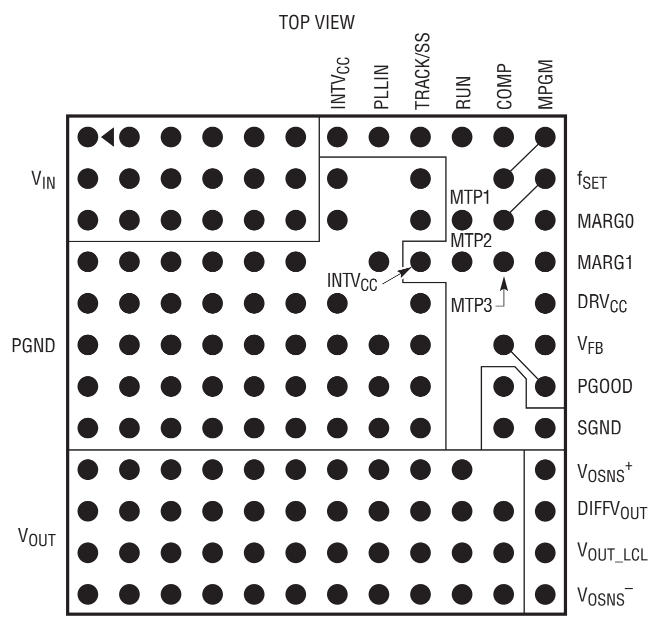
ABSOLUTE MAXIMUM RATINGS

(Note 1)

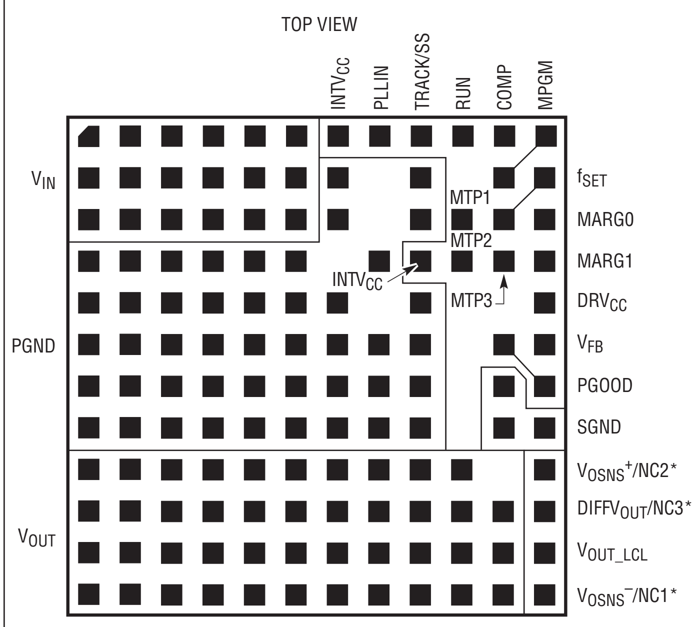
$INTV_{CC}$, DRV_{CC}, V_{OUT_LCL}, V_{OUT} ($V_{OUT} \leq 3.3V$ with $DIFFV_{OUT}$) ....−0.3V to 6V
PLLIN, TRACK/SS, MPGM, MARG0, MARG1, PGOOD, f_{SET} ....−0.3V to $INTV_{CC}$ + 0.3V
RUN ....−0.3V to 5V
V_{FB}, COMP ....−0.3V to 2.7V
V_{IN} ....−0.3V to 20V
V_{OSNS}^+, V_{OSNS}^-..........................−0.3V to $INTV_{CC}$ + 0.3V
Operating Temperature Range (Note 2)....−40°C to 85°C
Junction Temperature .... 125°C
Storage Temperature Range ....−55°C to 125°C

PIN CONFIGURATION

(See Table 5. Pin Assignment)



BGA PACKAGE
133-LEAD (15mm × 15mm × 3.42mm)
T_{JMAX} = 125°C, θ_{JA} = 15.5°C/W, $\theta_{JCbottom}$ = 6.5°C/W
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS
WEIGHT = 1.9g



LGA PACKAGE
133-LEAD (15mm × 15mm × 2.82mm)
T_{JMAX} = 125°C, θ_{JA} = 15°C/W, θ_{JC} = 6°C/W
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS
WEIGHT = 1.7g
*LTM4601A-1 ONLY

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE (NOTE 2)
LTM4601AEV#PBF	LTM4601AEV#PBF	LTM4601AV	133-Lead (15mm × 15mm × 2.82mm) LGA	−40°C to 85°C
LTM4601AIV#PBF	LTM4601AIV#PBF	LTM4601AV	133-Lead (15mm × 15mm × 2.82mm) LGA	−40°C to 85°C
LTM4601AEV-1#PBF	LTM4601AEV-1#PBF	LTM4601AV-1	133-Lead (15mm × 15mm × 2.82mm) LGA	−40°C to 85°C
LTM4601AIV-1#PBF	LTM4601AIV-1#PBF	LTM4601AV-1	133-Lead (15mm × 15mm × 2.82mm) LGA	−40°C to 85°C
LTM4601AEY#PBF	LTM4601AEY#PBF	LTM4601AY	133-Lead (15mm × 15mm × 3.42mm) BGA	−40°C to 85°C
LTM4601AIY#PBF	LTM4601AIY#PBF	LTM4601AY	133-Lead (15mm × 15mm × 3.42mm) BGA	−40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V, per typical application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage		●	4.5		20	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF ×3, C_{OUT} = 200µF, R_{SET} = 40.2k V_{IN} = 5V to 20V, I_{OUT} = 0A to 12A (Note 5)	●	1.478	1.5	1.522	V
Input Specifications							
$V_{IN(UVLO)}$	Undervoltage Lockout Threshold	I_{OUT} = 0A			3.2	4	V
$I_{INRUSH(VIN)}$	Input Inrush Current at Startup	I_{OUT} = 0A. V_{OUT} = 1.5V V_{IN} = 5V V_{IN} = 12V			 0.6 0.7		 A A
$I_{Q(VIN,NOLOAD)}$	Input Supply Bias Current	V_{IN} = 12V, No Switching V_{IN} = 12V, V_{OUT} = 1.5V, Switching Continuous V_{IN} = 5V, No Switching V_{IN} = 5V, V_{OUT} = 1.5V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 12V			3.8 38 2.5 42 22		mA mA mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 12A V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 12A V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 12A			1.81 3.63 4.29		A A A
$INTV_{CC}$	V_{IN} = 12V, RUN > 2V	No Load		4.7	5	5.3	V
Output Specifications							
I_{OUTDC}	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Note 5)		0		12	A
$\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A, V_{IN} from 4.5V to 20V	●			0.3	%
$\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, 0A to 12A (Note 5) V_{IN} = 12V, with Remote Sense Amplifier V_{IN} = 12V (LTM4601A-1)	 ● ●			 0.25 1	 % %
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 2× 100µF X5R Ceramic V_{IN} = 12V, V_{OUT} = 1.5V V_{IN} = 5V, V_{OUT} = 1.5V			 20 18		 mV_{P-P} mV_{P-P}
f_S	Output Ripple Voltage Frequency	I_{OUT} = 5A, V_{IN} = 12V, V_{OUT} = 1.5V			850		kHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 200µF, V_{OUT} = 1.5V, I_{OUT} = 0A, TRACK/SS = 10nF V_{IN} = 12V V_{IN} = 5V			 20 20		 mV mV
t_{START}	Turn-On Time	C_{OUT} = 200µF, V_{OUT} = 1.5V, TRACK/SS = Open, I_{OUT} = 1A Resistive Load V_{IN} = 12V V_{IN} = 5V			 0.5 0.5		 ms ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 2 × 22µF Ceramic, 470µF4V Sanyo POSCAP V_{IN} = 12V V_{IN} = 5V			 35 35		 mV mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50%, or 50% to 0% of Full Load V_{IN} = 12V			 25		 µs
I_{OUTPK}	Output Current Limit	C_{OUT} = 200µF Ceramic V_{IN} = 12V, V_{OUT} = 1.5V V_{IN} = 5V, V_{OUT} = 1.5V			 17 17		 A A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V, per typical application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Remote Sense Amp (Note 3) (LTM4601A Only, Not Supported in the LTM4601A-1)							
V_{OSNS}^+, V_{OSNS}^- CM Range	Common Mode Input Voltage Range	V_{IN} = 12V, RUN > 2V		0		$INTV_{CC}$ – 1	V
$DIFFV_{OUT}$ Range	Output Voltage Range	V_{IN} = 12V, $DIFFV_{OUT}$ Load = 100k		0		$INTV_{CC}$ – 1	V
V_{OS}	Input Offset Voltage Magnitude					1.25	mV
A_V	Differential Gain				1		V/V
GBP	Gain-Bandwidth Product				3		MHz
SR	Slew Rate				2		V/µs
R_{IN}	Input Resistance	V_{OSNS}^+ to GND			20		kΩ
CMRR	Common Mode Rejection Mode				100		dB
Control Stage							
V_{FB}	Error Amplifier Input Voltage Accuracy	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.594	0.6	0.606	V
V_{RUN}	RUN Pin On/Off Threshold			1	1.5	1.9	V
$I_{TRACK/SS}$	Soft-Start Charging Current	$V_{TRACK/SS}$ = 0V		–1	–1.5	–2	µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			50	100	ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 4)			250	400	ns
R_{PLLIN}	PLLIN Input Resistance				50		kΩ
I_{DRVCC}	Current into DRV_{CC} Pin	V_{OUT} = 1.5V, I_{OUT} = 1A, DRV_{CC} = 5V			18	25	mA
R_{FBHI}	Resistor Between V_{OUT_LCL} and V_{FB}			60.098	60.4	60.702	kΩ
V_{MPGM}	Margin Reference Voltage				1.18		V
V_{MARG0}, V_{MARG1}	MARG0, MARG1 Voltage Thresholds				1.4		V
PGOOD Output							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising		7	10	13	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling		–7	–10	–13	%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning			1.5		%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.15	0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4601A is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4601AE/LTM4601AE-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4601AI/LTM4601AI-1 are guaranteed over the –40°C to 85°C operating temperature range.

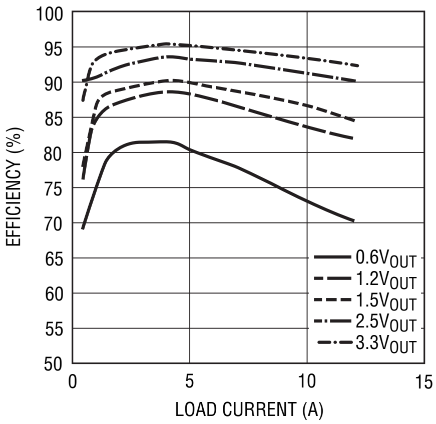
Note 3: Remote sense amplifier recommended for ≤3.3V output.

Note 4: 100% tested at wafer level only.

Note 5: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

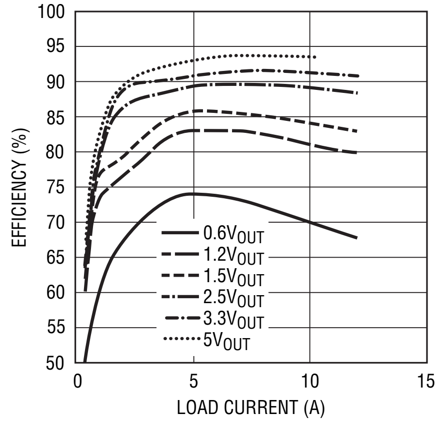
TYPICAL PERFORMANCE CHARACTERISTICS (See Figure 18 for all curves)

Efficiency vs Load Current with $5V_{IN}$



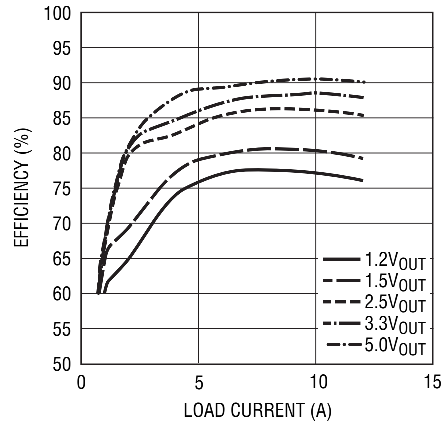
4601A G01

Efficiency vs Load Current with $12V_{IN}$



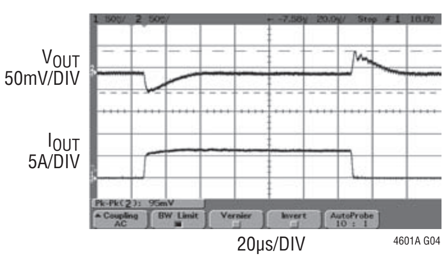
4601A G02

Efficiency vs Load Current with $20V_{IN}$



4601A G03

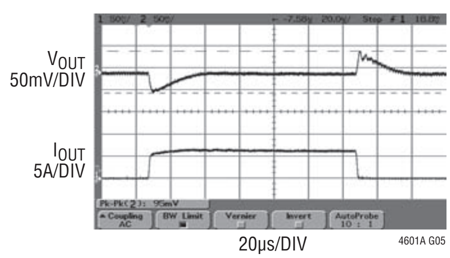
1.2V Transient Response



4601A G04

1.2V AT 6A/µs LOAD STEP
C_{OUT} = 3 • 22µF 6.3V CERAMICS,
470µF 4V SANYO POSCAP
C3 = 100pF

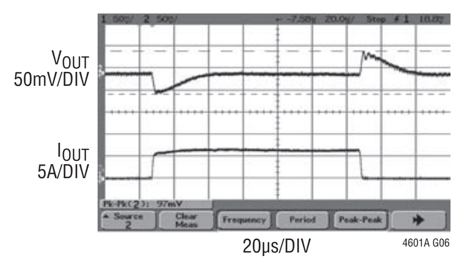
1.5V Transient Response



4601A G05

1.5V AT 6A/µs LOAD STEP
C_{OUT} = 3 • 22µF 6.3V CERAMICS,
470µF 4V SANYO POSCAP
C3 = 100pF

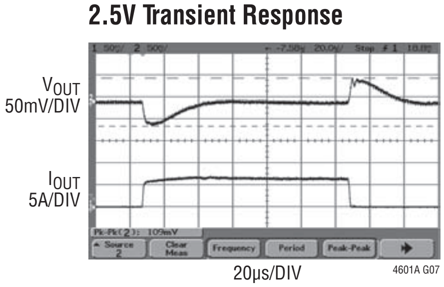
1.8V Transient Response



4601A G06

1.8V AT 6A/µs LOAD STEP
C_{OUT} = 3 • 22µF 6.3V CERAMICS,
470µF 4V SANYO POSCAP
C3 = 100pF

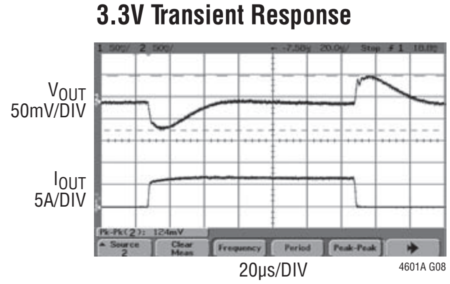
2.5V Transient Response



4601A G07

2.5V AT 6A/µs LOAD STEP
C_{OUT} = 3 • 22µF 6.3V CERAMICS,
470µF 4V SANYO POSCAP
C3 = 100pF

3.3V Transient Response

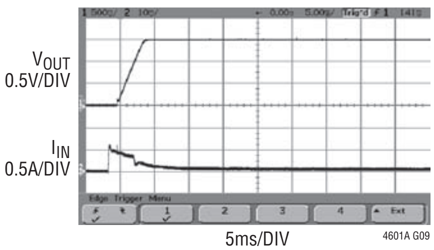


4601A G08

3.3V AT 6A/µs LOAD STEP
C_{OUT} = 3 • 22µF 6.3V CERAMICS,
470µF 4V SANYO POSCAP
C3 = 100pF

TYPICAL PERFORMANCE CHARACTERISTICS (See Figure 18 for all curves)

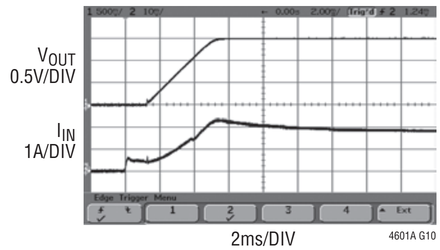
Start-Up, I_{OUT} = 0A



4601A G09

V_{IN} = 12V
V_{OUT} = 1.5V
C_{OUT} = 470µF, 3 × 22µF
SOFT-START = 10nF

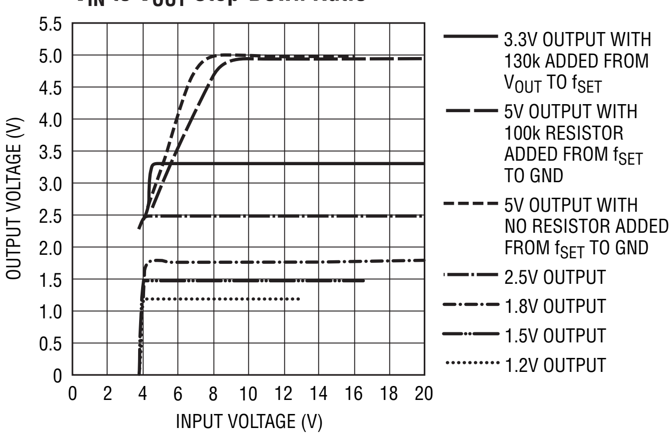
Start-Up, I_{OUT} = 12A (Resistive Load)



4601A G10

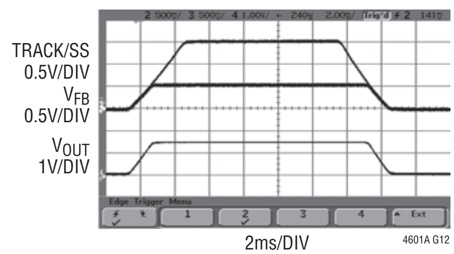
V_{IN} = 12V
V_{OUT} = 1.5V
C_{OUT} = 470µF, 3 × 22µF
SOFT-START = 10nF

V_{IN} to V_{OUT} Step-Down Ratio



4601A G11

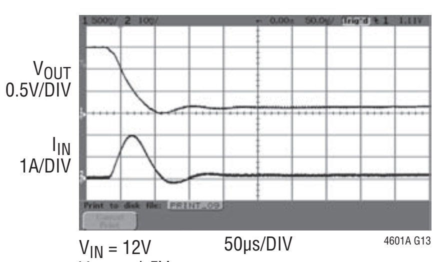
Track, I_{OUT} = 12A



4601A G12

V_{IN} = 12V
V_{OUT} = 1.5V
C_{OUT} = 470µF, 3 × 22µF
SOFT-START = 10nF

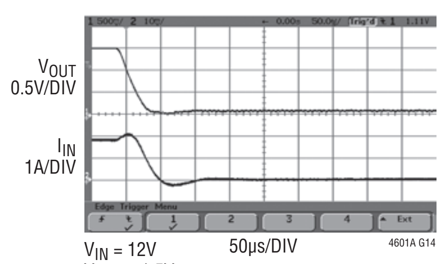
Short-Circuit Protection, I_{OUT} = 0A



4601A G13

V_{IN} = 12V
V_{OUT} = 1.5V
C_{OUT} = 470µF, 3 × 22µF
SOFT-START = 10nF

Short-Circuit Protection, I_{OUT} = 12A



4601A G14

V_{IN} = 12V
V_{OUT} = 1.5V
C_{OUT} = 470µF, 3 × 22µF
SOFT-START = 10nF

PIN FUNCTIONS (See Package Description for Pin Assignment)

V_{IN} (Bank 1): Power Input Pins. Apply input voltage between these pins and PGND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and PGND pins.

V_{OUT} (Bank 3): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing output decoupling capacitance directly between these pins and PGND pins. See Figure 15.

PGND (Bank 2): Power ground pins for both input and output returns.

V_{OSNS}^- (Pin M12): (–) Input to the Remote Sense Amplifier. This pin connects to the ground remote sense point. The remote sense amplifier is used for $V_{OUT} \leq 3.3V$. Tie to $INTV_{CC}$ if not used.

NC1 (Pin M12): No Internal Connection on the LTM4601A-1.

V_{OSNS}^+ (Pin J12): (+) Input to the Remote Sense Amplifier. This pin connects to the output remote sense point. The remote sense amplifier is used for $V_{OUT} \leq 3.3V$. Tie to GND if not used.

NC2 (Pin J12): No Internal Connection on the LTM4601A-1.

$DIFFV_{OUT}$ (Pin K12): Output of the Remote Sense Amplifier. This pin connects to the V_{OUT_LCL} pin. Leave floating if not used.

NC3 (Pin K12): No Internal Connection on the LTM4601A-1.

DRV_{CC} (Pin E12): This pin normally connects to $INTV_{CC}$ for powering the internal MOSFET drivers. This pin can be biased up to 6V from an external supply with about 50mA capability, or an external circuit shown in Figure 16. This improves efficiency at the higher input voltages by reducing power dissipation in the module.

$INTV_{CC}$ (Pin A7, D9): This pin is for additional decoupling of the 5V internal regulator. These pins are internally connected. Pin A7 is a test pin.

PLLIN (Pin A8): External Clock Synchronization Input to the Phase Detector. This pin is internally terminated to SGND with a 50k resistor. Apply a clock with high level above 2V and below $INTV_{CC}$. See the Applications Information section.

TRACK/SS (Pin A9): Output Voltage Tracking and Soft-Start Pin. When the module is configured as a master output, then a soft-start capacitor is placed on this pin to ground to control the master ramp rate. A soft-start capacitor can be used for soft-start turn on as a stand alone regulator. Slave operation is performed by putting a resistor divider from the master output to ground, and connecting the center point of the divider to this pin. See the Applications Information section.

MPGM (Pins A12, B11): Programmable Margining Input. A resistor from this pin to ground sets a current that is equal to 1.18V/R. This current multiplied by 10kΩ will equal a value in millivolts that is a percentage of the 0.6V reference voltage. See the Applications Information section. To parallel LTM4601As, each requires an individual MPGM resistor. Do not tie MPGM pins together. Both pins are internally connected. Pin A12 is a test pin.

f_{SET} (Pins B12, C11): Frequency Set Internally to 850kHz. An external resistor can be placed from this pin to ground to increase frequency. See the Applications Information section for frequency adjustment. Both pins are internally connected. Pin B12 is a test pin.

V_{FB} (Pin F12): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT_LCL} pin with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and SGND pins. See the Applications Information section.

MARG0 (Pin C12): This pin is the LSB logic input for the margining function. Together with the MARG1 pin it will determine if margin high, margin low or no margin state is applied. The pin has an internal pull-down resistor of 50k. See the Applications Information section.

PIN FUNCTIONS (See Package Description for Pin Assignment)

MARG1 (Pin D12): This pin is the MSB logic input for the margining function. Together with the MARG0 pin it will determine if margin high, margin low or no margin state is applied. The pin has an internal pull-down resistor of 50k. See the Applications Information section.

SGND (Pins H12, H11, G11): Signal Ground. These pins connect to PGND at output capacitor point. See Figure 15.

COMP (Pin A11): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.7V corresponding to zero sense voltage (zero current).

PGOOD (Pins G12, F11): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point, after a 25µs power bad mask timer expires.

RUN (Pin A10): Run Control Pin. A voltage above 1.9V will turn on the module, and when below 1V, will turn off the module. A programmable UVLO function can be accomplished by connecting to a resistor divider from V_{IN} to ground. See Figure 1. This pin has a 5.1V Zener to ground. Maximum pin voltage is 5V. Limit current into the RUN pin to less than 1mA.

V_{OUT_LCL} (Pin L12): V_{OUT} connects directly to this pin to bypass the remote sense amplifier, or $DIFFV_{OUT}$ connects to this pin when the remote sense amplifier is used. V_{OUT_LCL} can be connected to V_{OUT} on the LTM4601A-1, V_{OUT} is internally connected to V_{OUT_LCL} with 50Ω in the LTM4601A-1.

MTP1, MTP2, MPT3 (Pins C10, D10, D11): Extra Mounting Pads. These pads must be left floating (electrical open circuit) and are used for enhanced solder joint strength.

SIMPLIFIED BLOCK DIAGRAM

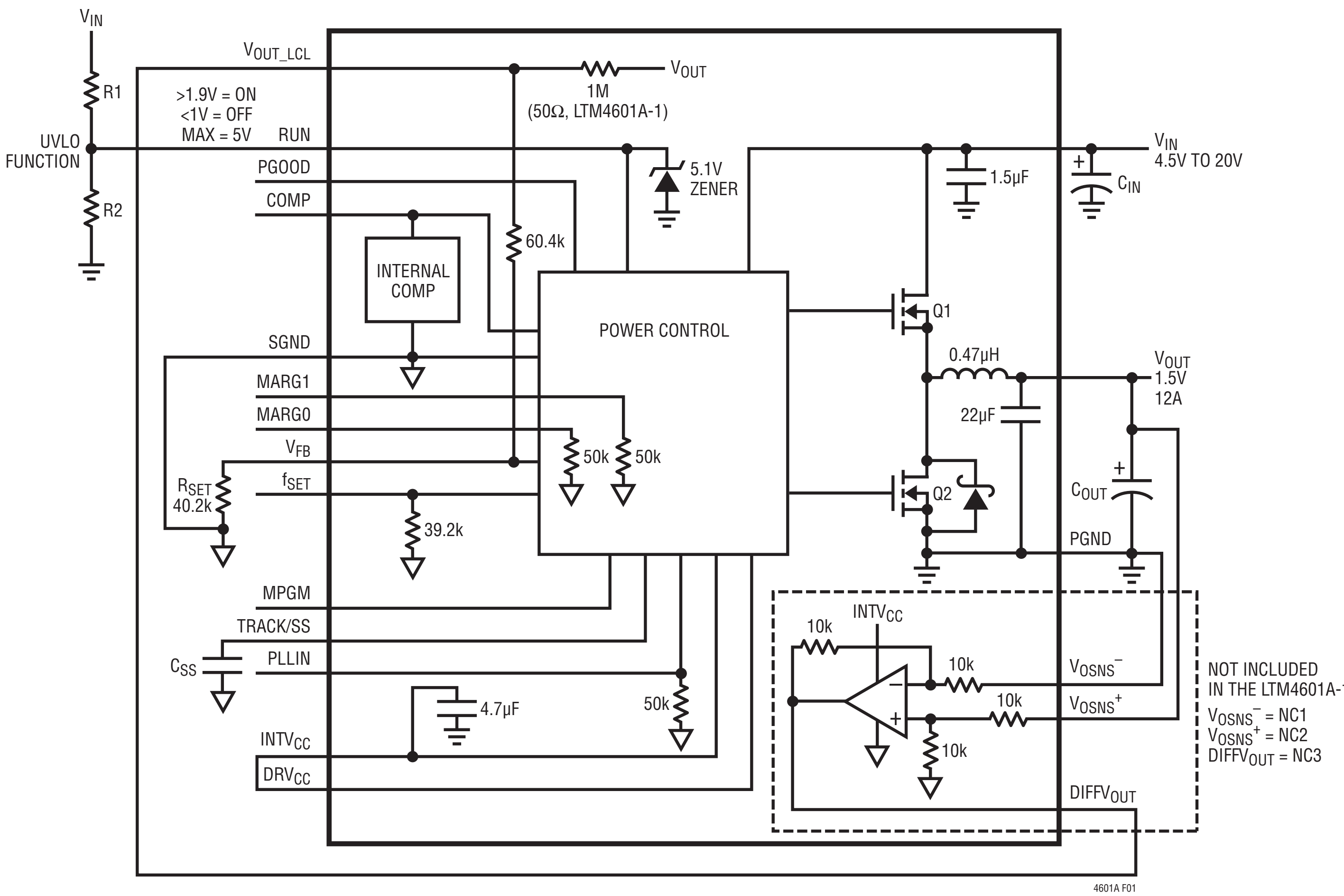


Figure 1. Simplified LTM4601A/LTM4601A-1 Block Diagram

DECOUPLING REQUIREMENTS T_A = 25°C, V_{IN} = 12V. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.5V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 12A	20	30		µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4.5V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 12A	100	200		µF

OPERATION

Power Module Description

The LTM4601A is a standalone nonisolated switching mode DC/DC power supply. It can deliver up to 12A of DC output current with few external input and output capacitors. This module provides precisely regulated output voltage programmable via one external resistor from $0.6V_{DC}$ to $5.0V_{DC}$ over a 4.5V to 20V wide input voltage. The typical application schematic is shown in Figure 18.

The LTM4601A has an integrated constant on-time current mode regulator, ultralow $R_{DS(ON)}$ FETs with fast switching speed and integrated Schottky diodes. The typical switching frequency is 850kHz at full load. With current mode control and internal feedback loop compensation, the LTM4601A module has sufficient stability margins and good transient performance under a wide range of operating conditions and with a wide range of output capacitors, even all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit. Besides, foldback current limiting is provided in an overcurrent condition while V_{FB} drops. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET Q1 is turned off and bottom FET Q2 is turned on and held on until the overvoltage condition clears.

Pulling the RUN pin below 1V forces the controller into its shutdown state, turning off both Q1 and Q2. At low load current, the module works in continuous current mode by default to achieve minimum output ripple voltage.

When DRV_{CC} pin is connected to $INTV_{CC}$ an integrated 5V linear regulator powers the internal gate drivers. If a 5V external bias supply is applied on the DRV_{CC} pin, then an efficiency improvement will occur due to the reduced power loss in the internal linear regulator. This is especially true at the high end of the input voltage range.

The LTM4601A has a very accurate differential remote sense amplifier with very low offset. This provides for very accurate output voltage measurement at the load. The MPGM pin, MARG0 pin and MARG1 pin are used to support voltage margining, where the percentage of margin is programmed by the MPGM pin, and the MARG0 and MARG1 select margining.

The PLLIN pin provides frequency synchronization of the device to an external clock. The TRACK/SS pin is used for power supply tracking and soft-start programming.

APPLICATIONS INFORMATION

The typical LTM4601A application circuit is shown in Figure 18. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 2 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step down ratio that can be achieved for a given input voltage. These constraints are shown in the Typical Performance Characteristics curves labeled "V_{IN} to V_{OUT} Step-Down Ratio". Note that additional thermal derating may apply. See the Thermal Considerations and Output Current Derating section of this data sheet.

Output Voltage Programming and Margining

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 1M and a 60.4k 0.5% internal feedback resistor connects V_{OUT} and V_{FB} pins together. The V_{OUT_LCL} pin is connected between the 1M and the 60.4k resistor. The 1M resistor is used to protect against an output overvoltage condition if the V_{OUT_LCL} pin is not connected to the output, or if the remote sense amplifier output is not connected to V_{OUT_LCL}. In these cases, the output voltage will default to 0.6V. Adding a resistor R_{SET} from the V_{FB} pin to SGND pin programs the output voltage:

$$V_{OUT} = 0.6V \frac{60.4k + R_{SET}}{R_{SET}}$$

Table 1. R_{SET} Standard 1% Resistor Values vs V_{OUT}

R_{SET} (kΩ)	Open	60.4	40.2	30.1	25.5	19.1	13.3	8.25
V_{OUT} (V)	0.6	1.2	1.5	1.8	2	2.5	3.3	5

The MPGM pin programs a current that when multiplied by an internal 10k resistor sets up the 0.6V reference ± offset for margining. A 1.18V reference divided by the R_{PGM} resistor on the MPGM pin programs the current. Calculate $V_{OUT(MARGIN)}$:

$$V_{OUT(MARGIN)} = \frac{\%V_{OUT}}{100} \bullet V_{OUT}$$

where $\%V_{OUT}$ is the percentage of V_{OUT} you want to margin, and $V_{OUT(MARGIN)}$ is the margin quantity in volts:

$$R_{PGM} = \frac{V_{OUT}}{0.6V} \bullet \frac{1.18V}{V_{OUT(MARGIN)}} \bullet 10k$$

where R_{PGM} is the resistor value to place on the MPGM pin to ground.

The margining voltage, $V_{OUT(MARGIN)}$, will be added or subtracted from the nominal output voltage as determined by the state of the MARG0 and MARG1 pins. See the truth table below:

MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

Input Capacitors

LTM4601A module should be connected to a low AC impedance DC source. Input capacitors are required to be placed adjacent to the module. In Figure 18, the 10µF ceramic input capacitors are selected for their ability to handle the large RMS current into the converter. An input bulk capacitor of 100µF is optional. This 100µF capacitor is only needed if the input source impedance is compromised by long inductive leads or traces.

APPLICATIONS INFORMATION

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1 - D)}$$

In the above equation, $\eta\%$ is the estimated efficiency of the power module. C_{IN} can be a switcher-rated electrolytic aluminum capacitor, OS-CON capacitor or high value ceramic capacitor. Note the capacitor ripple current ratings are often based on temperature and hours of life. This makes it advisable to properly derate the input capacitor, or choose a capacitor rated at a higher temperature than required. Always contact the capacitor manufacturer for derating requirements.

In Figure 18, the 10µF ceramic capacitors are together used as a high frequency input decoupling capacitor. In a typical 12A output application, three very low ESR, X5R or X7R 10µF ceramic capacitors are recommended. These decoupling capacitors should be placed directly adjacent to the module input pins in the PCB layout to minimize the trace inductance and high frequency AC noise. Each 10µF ceramic is typically good for 2A to 3A of RMS ripple current. Refer to your ceramics capacitor catalog for the RMS current ratings.

Multiphase operation with multiple LTM4601A devices in parallel will lower the effective input RMS ripple current due to the interleaving operation of the regulators. Application Note 77 provides a detailed explanation. Refer to Figure 2 for the input capacitor ripple current reduction as a function of the number of phases. The figure provides a ratio of RMS ripple current to DC load current as function of duty cycle and the number of paralleled phases. Pick the corresponding duty cycle and the number of phases to arrive at the correct ripple current value. For example, the 2-phase parallel LTM4601A design provides 24A at 2.5V output from a 12V input. The duty cycle is DC = 2.5V/12V = 0.21. The 2-phase curve has a ratio of ~0.25 for a duty cycle of 0.21. This 0.25 ratio of RMS ripple current to a DC load current of 24A equals ~6A of input RMS ripple current for the external input capacitors.

Output Capacitors

The LTM4601A is designed for low output ripple voltage. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output ripple voltage and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or a ceramic capacitor. The typical capacitance is 200µF if all ceramic output capacitors are used. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 2 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 5A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to maximize transient performance.

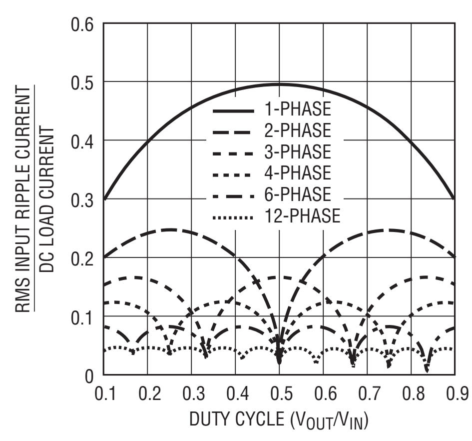


Figure 2. Normalized Input RMS Ripple Current vs Duty Cycle for One to Six Modules (Phases)

APPLICATIONS INFORMATION

Multiphase operation with multiple LTM4601A devices in parallel will lower the effective output ripple current due to the interleaving operation of the regulators. For example, each LTM4601A's inductor current in a 12V to 2.5V multiphase design can be read from the Inductor Ripple Current vs Duty Cycle graph (Figure 3). The large ripple current at low duty cycle and high output voltage can be reduced by adding an external resistor from f_{SET} to ground which increases the frequency. If the duty cycle is DC = 2.5V/12V = 0.21, the inductor ripple current for 2.5V output at 21% duty cycle is ~6A in Figure 3.

Figure 4 provides a ratio of peak-to-peak output ripple current to the inductor current as a function of duty cycle and the number of paralleled phases. Pick the corresponding duty cycle and the number of phases to arrive at the correct output ripple current ratio value. If a 2-phase operation is chosen at a duty cycle of 21%, then 0.6 is the ratio. This 0.6 ratio of output ripple current to inductor ripple of 6A equals 3.6A of effective output ripple current. Refer to Application Note 77 for a detailed explanation of output ripple current reduction as a function of paralleled phases.

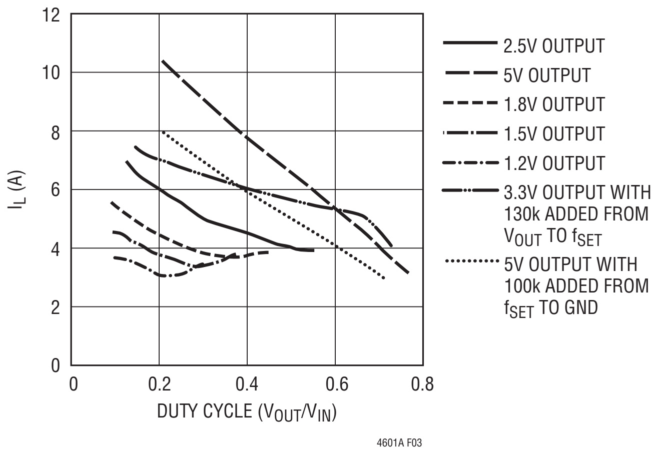


Figure 3. Inductor Ripple Current vs Duty Cycle

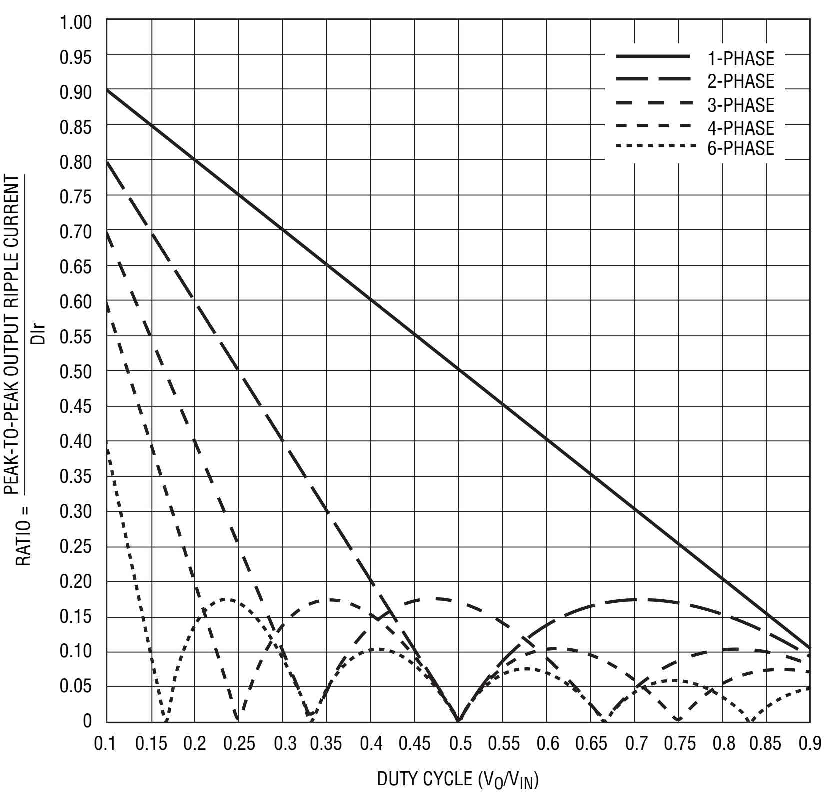


Figure 4. Normalized Output Ripple Current vs Duty Cycle, DIr = $V_O T/L_I$, DIr = Each Phase's Inductor Current

APPLICATIONS INFORMATION

The output ripple voltage has two components that are related to the amount of bulk capacitance and effective series resistance (ESR) of the output bulk capacitance. Therefore, the output ripple voltage can be calculated with the known effective output ripple current. The equation: $\Delta V_{OUT(P-P)} \approx (\Delta I_L/(8 \bullet f \bullet m \bullet C_{OUT}) + ESR \bullet \Delta I_L)$, where f is frequency and m is the number of parallel phases. This calculation process can be easily accomplished by using LTpowerCAD™.

Fault Conditions: Current Limit and Overcurrent Foldback

LTM4601A has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in response to transients.

To further limit current in the event of an overload condition, the LTM4601A provides foldback current limiting. If the output voltage falls by more than 50%, then the maximum output current is progressively lowered to about one sixth of its full current limit value.

Soft-Start and Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on this pin will program the ramp rate of the output voltage. A 1.5µA current source will charge up the external soft-start capacitor to 80% of the 0.6V internal voltage reference plus or minus any margin delta. This will control the ramp of the internal reference and the output voltage. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.8 \bullet \left(0.6V \pm V_{OUT(MARGIN)}\right) \bullet \frac{C_{SS}}{1.5\mu A}$$

When the RUN pin falls below 1.5V, then the TRACK/SS pin is reset to allow for proper soft-start control when the regulator is enabled again. Current foldback and forced continuous mode are disabled during the soft-start process. The soft-start function can also be used to control the output ramp up time, so that another regulator can be easily tracked to it.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider. Figure 5 shows an example of coincident tracking. Ratiometric modes of tracking can be achieved by selecting different resistor values to change the output tracking ratio. The master output must be greater than the slave output for the tracking to work. Figure 6 shows the coincident output tracking characteristics.

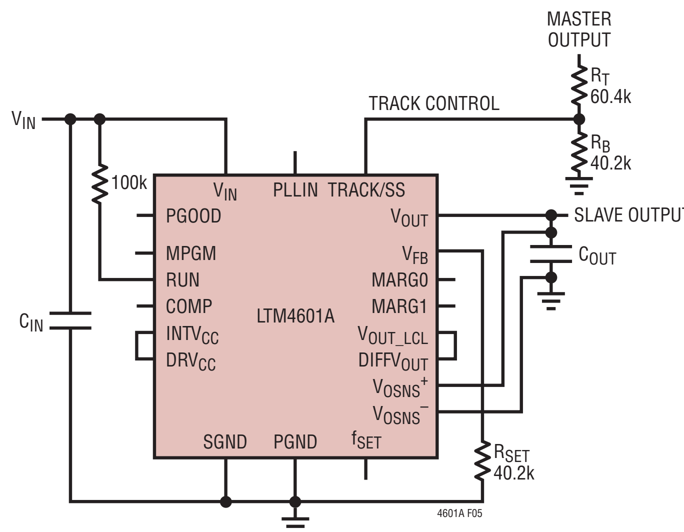


Figure 5. Coincident Tracking Schematic

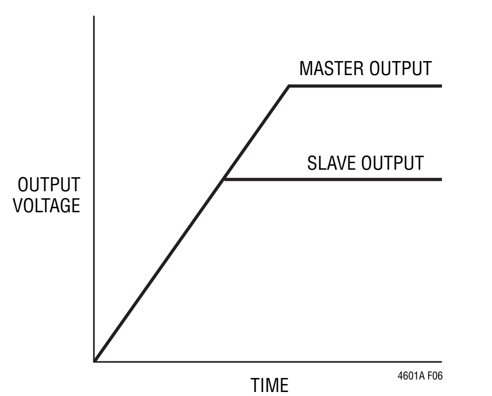


Figure 6. Coincident Output Tracking Characteristics

APPLICATIONS INFORMATION

Run Enable

The RUN pin is used to enable the power module. The pin has an internal 5.1V zener to ground. The pin can be driven with a logic input not to exceed 5V.

The RUN pin can also be used as an undervoltage lockout (UVLO) function by connecting a resistor divider from the input supply to the RUN pin:

$$V_{UVLO} = \frac{R1 + R2}{R2} \bullet 1.5V$$

See Figure 1, Simplified Block Diagram.

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin monitors a ±10% window around the regulation point and tracks with margining.

COMP Pin

This pin is the external compensation pin. The module has already been internally compensated for most output voltages. Table 2 is provided for most application requirements. LTpowerCAD is available for other control loop optimization.

PLLIN

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on to be locked to the rising edge of an external clock. The frequency range is ±30% around the operating frequency of 850kHz. A pulse detection circuit is used to detect a clock on the PLLIN pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 400ns and the amplitude at least 2V. The PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin. During startup of the regulator, the phase-locked loop function is disabled.

$INTV_{CC}$ and DRV_{CC} Connection

An internal low dropout regulator produces an internal 5V supply that powers the control circuitry and DRV_{CC} for driving the internal power MOSFETs. Therefore, if the system does not have a 5V power rail, the LTM4601A can be directly powered by V_{IN}. The gate drive current through the LDO is about 20mA. The internal LDO power dissipation can be calculated as:

$$P_{LDO\_LOSS} = 20mA \bullet (V_{IN} - 5V)$$

The LTM4601A also provides the external gate drive voltage pin DRV_{CC}. If there is a 5V rail in the system, it is recommended to connect the DRV_{CC} pin to the external 5V rail. This is especially true for higher input voltages. Do not apply more than 6V to the DRV_{CC} pin. A 5V output can be used to power the DRV_{CC} pin with an external circuit as shown in Figure 16.

Parallel Operation of the Module

The LTM4601A device is an inherently current mode controlled device. Parallel modules will have very good current sharing. This will balance the thermals on the design. Figure 19 shows the schematic of a parallel design. The voltage feedback equation changes with the variable N as modules are paralleled:

$$V_{OUT} = 0.6V \frac{\frac{60.4k}{N} + R_{SET}}{R_{SET}}$$

N is the number of paralleled modules.

Figure 19 shows an LTM4601A and an LTM4601A-1 used in a parallel design. The 2nd LTM4601A device does not require the remote sense amplifier, therefore, the LTM4601A-1 device is used. An LTM4601A device can be used without the diff amp. V_{OSNS}^+ can be tied to ground and the V_{OSNS}^- can be tied to $INTV_{CC}$. $DIFFV_{OUT}$ can float. When using multiple LTM4601A-1 devices in parallel with an LTM4601A, limit the number to five for a total of six modules in parallel.

APPLICATIONS INFORMATION

Thermal Considerations and Output Current Derating

The power loss curves in Figures 7 and 8 can be used in coordination with the load current derating curves in Figures 9 to 14 for calculating an approximate θ_{JA} for the module with various heat sinking methods. Thermal models are derived from several temperature measurements at the bench and thermal modeling analysis. Thermal Application Note 103 provides a detailed explanation of the analysis for the thermal models and the derating curves. Tables 3 and 4 provide a summary of the equivalent θ_{JA} for the noted conditions. These equivalent θ_{JA} parameters are correlated to the measured values, and are improved with air flow. The case temperature is maintained at 100°C or below for the derating curves. The maximum case temperature of 100°C is to allow for a rise of about 13°C to 25°C inside the µModule regulator with a thermal resistance θ_{JC} from junction to case between 6°C/W to 9°C/W. This will maintain the maximum junction temperature inside the µModule regulator below 125°C.

Safety Considerations

The LTM4601A modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

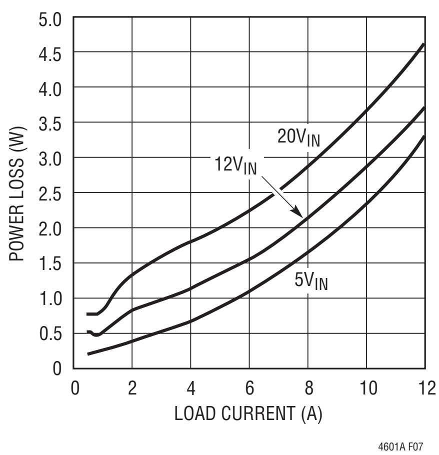


Figure 7. 1.5V Power Loss

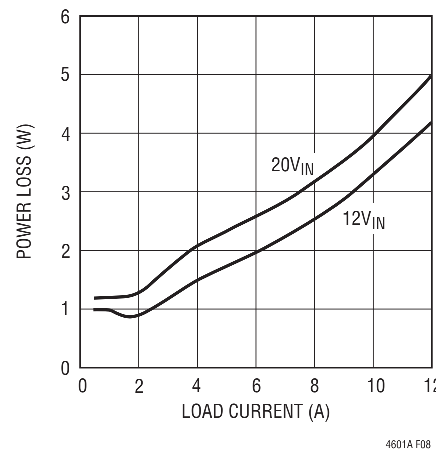


Figure 8. 3.3V Power Loss

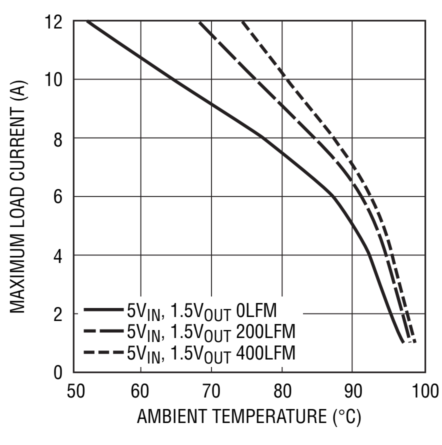


Figure 9. No Heat Sink $5V_{IN}$

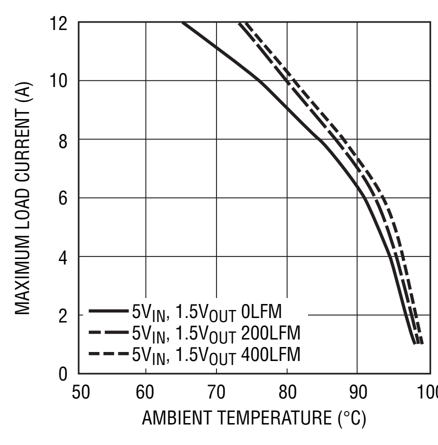


Figure 10. BGA Heat Sink $5V_{IN}$

APPLICATIONS INFORMATION

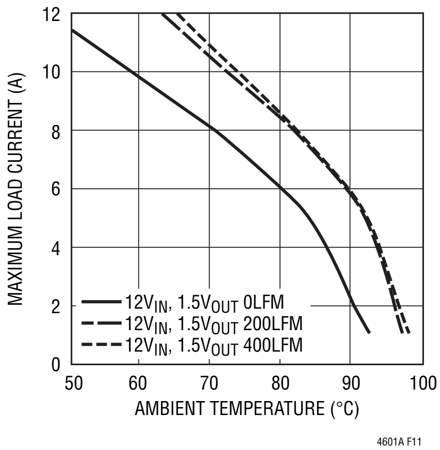


Figure 11. No Heat Sink $12V_{IN}$

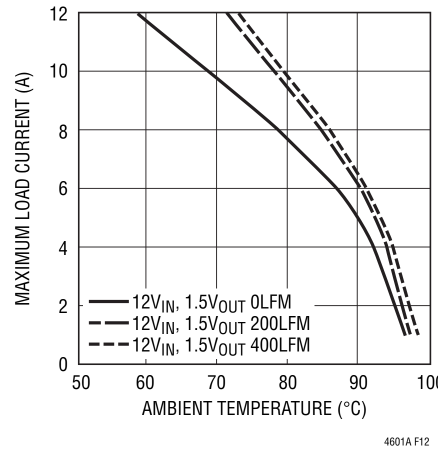


Figure 12. BGA Heat Sink $12V_{IN}$

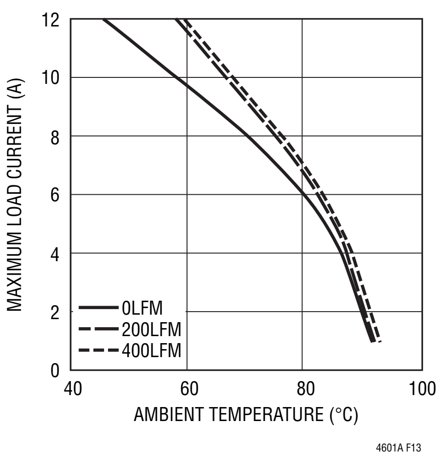


Figure 13. $12V_{IN}$, $3.3V_{OUT}$, No Heat Sink

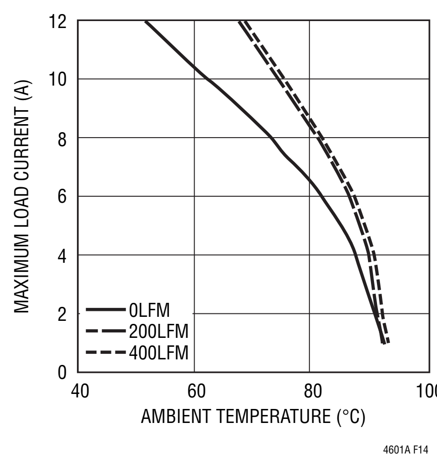


Figure 14. $12V_{IN}$, $3.3V_{OUT}$, BGA Heat Sink

APPLICATIONS INFORMATION

Table 2. Output Voltage Response Versus Component Matrix (Refer to Figure 18), 0A to 6A Load Step

TYPICAL MEASURED VALUES

C_{OUT1} VENDORS	PART NUMBER	C_{OUT2} VENDORS	PART NUMBER
TDK	C4532X5R0J107MZ (100µF, 6.3V)	SANYO POSCAP	6TPE330MIL (330µF, 6.3V)
TAIYO YUDEN	JMK432BJ107MU-T (100µF, 6.3V)	SANYO POSCAP	2R5TPE470M9 (470µF, 2.5V)
TAIYO YUDEN	JMK316BJ226ML-T501 (22µF, 6.3V)	SANYO POSCAP	4TPE470MCL (470µF, 4V)

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	C_{COMP}	C3	V_{IN} (V)	DROOP (mV)	PEAK TO PEAK (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{SET} (kΩ)
1.2	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	47pF	5	70	140	30	6	60.4
1.2	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	100pF	5	35	70	20	6	60.4
1.2	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	22pF	5	70	140	20	6	60.4
1.2	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	5	40	93	30	6	60.4
1.2	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	12	70	140	30	6	60.4
1.2	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	100pF	12	35	70	20	6	60.4
1.2	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	22pF	12	70	140	20	6	60.4
1.2	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	12	49	98	20	6	60.4
1.5	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	5	48	100	35	6	40.2
1.5	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	33pF	5	54	109	30	6	40.2
1.5	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	5	44	84	30	6	40.2
1.5	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	5	61	118	30	6	40.2
1.5	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	12	48	100	35	6	40.2
1.5	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	33pF	12	54	109	30	6	40.2
1.5	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	12	44	89	25	6	40.2
1.5	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	12	54	108	25	6	40.2
1.8	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	47pF	5	48	100	30	6	30.1
1.8	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	100pF	5	44	90	20	6	30.1
1.8	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	5	68	140	30	6	30.1
1.8	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	5	65	130	30	6	30.1
1.8	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	12	60	120	30	6	30.1
1.8	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	100pF	12	60	120	30	6	30.1
1.8	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	12	68	140	30	6	30.1
1.8	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	12	65	130	20	6	30.1
2.5	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 4V	NONE	100pF	5	48	103	30	6	19.1
2.5	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	220pF	5	56	113	30	6	19.1
2.5	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	NONE	5	57	116	30	6	19.1
2.5	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	5	60	115	25	6	19.1
2.5	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 4V	NONE	100pF	12	48	103	30	6	19.1
2.5	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	NONE	12	51	102	30	6	19.1
2.5	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	220pF	12	56	113	30	6	19.1
2.5	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	220pF	12	70	140	25	6	19.1
3.3	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	7	120	240	30	6	13.3
3.3	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 4V	NONE	100pF	7	110	214	30	6	13.3
3.3	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	7	110	214	30	6	13.3
3.3	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	7	114	230	30	6	13.3
3.3	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 4V	NONE	100pF	12	110	214	30	6	13.3
3.3	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	150pF	12	110	214	35	6	13.3
3.3	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	12	110	214	35	6	13.3
3.3	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	12	114	230	30	6	13.3
5	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	22pF	15	188	375	25	6	8.25
5	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	22pF	20	159	320	25	6	8.25

APPLICATIONS INFORMATION

Table 3. 1.5V Output at 12A

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W) LGA	θ_{JA} (°C/W) BGA
Figures 9, 11	5, 12	Figure 7	0	None	15.2	15.7
Figures 9, 11	5, 12	Figure 7	200	None	14	14.5
Figures 9, 11	5, 12	Figure 7	400	None	12	12.5
Figures 10, 12	5, 12	Figure 7	0	BGA Heat Sink	13.9	14.4
Figures 10, 12	5, 12	Figure 7	200	BGA Heat Sink	11.3	11.8
Figures 10, 12	5, 12	Figure 7	400	BGA Heat Sink	10.25	10.75

Table 4. 3.3V Output at 12A

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W) LGA	θ_{JA} (°C/W) BGA
Figure 13	12	Figure 8	0	None	15.2	15.7
Figure 13	12	Figure 8	200	None	14.6	15.0
Figure 13	12	Figure 8	400	None	13.4	13.9
Figure 14	12	Figure 8	0	BGA Heat Sink	13.9	14.4
Figure 14	12	Figure 8	200	BGA Heat Sink	11.1	11.6
Figure 14	12	Figure 8	400	BGA Heat Sink	10.5	11

Heat Sink Manufacturer

Aavid Thermalloy	Part No: 375424B00034G	Phone: 603-224-9988

APPLICATIONS INFORMATION

Layout Checklist/Example

The high integration of LTM4601A makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, PGND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit. Refer frequency synchronization source to power ground.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads unless they are capped.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.

Figure 15 gives a good example of the recommended layout.

Frequency Adjustment

The LTM4601A is designed to typically operate at 850kHz across most input conditions. The f_{SET} pin is normally left open. The switching frequency has been optimized for maintaining constant output ripple noise over most operating ranges. The 850kHz switching frequency and the 400ns minimum off-time can limit operation at higher duty cycles like 5V to 3.3V, and produce excessive inductor ripple currents for lower duty cycle applications like 20V to 5V. The $5V_{OUT}$ and $3.3V_{OUT}$ drop out curves are modified by adding an external resistor on the f_{SET} pin to allow for lower input voltage operation, or higher input voltage operation.

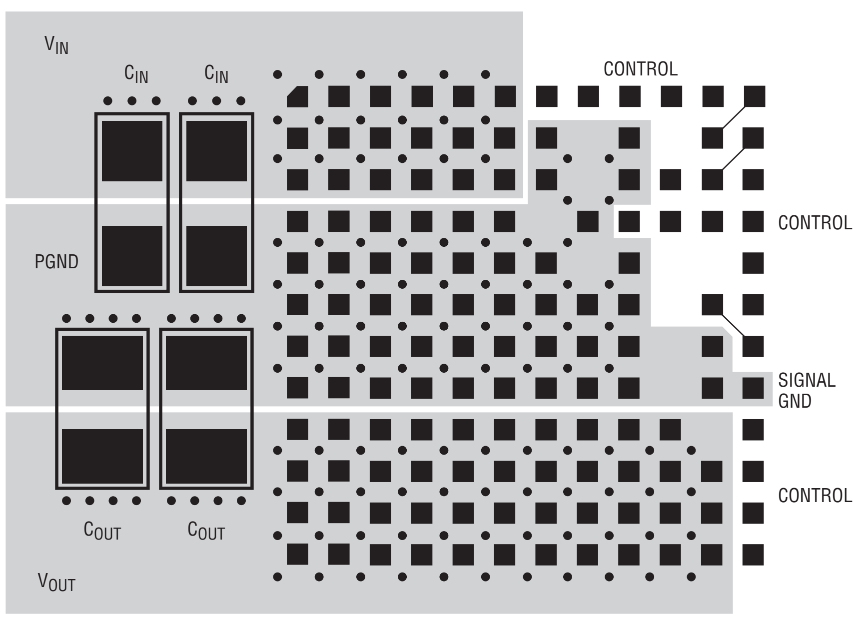


Figure 15. Recommended Layout
(LGA and BGA PCB Layouts Are Identical with the Exception of Circle Pads for BGA, See Package Description.)

APPLICATIONS INFORMATION

Example for 5V Output

LTM4601A minimum on-time = 100ns
t_{ON} = ((V_{OUT} • 10pF)/I_{fSET}), for V_{OUT} > 4.8V use 4.8V

LTM4601A minimum off-time = 400ns
t_{OFF} = t – t_{ON}, where t = 1/Frequency

Duty Cycle = t_{ON}/t or V_{OUT}/V_{IN}

Equations for setting frequency:

I_{fSET} = (V_{IN}/(3 • R_{fSET})), for 20V operation, I_{fSET} = 170μA, t_{ON} = ((4.8 • 10pF)/I_{fSET}), t_{ON} = 282ns, where the internal R_{fSET} is 39.2k. Frequency = (V_{OUT}/(V_{IN} • t_{ON})) = (5V/(20 • 282ns)) ≈ 886kHz. The inductor ripple current begins to get high at the higher input voltages due to a larger voltage across the inductor. This is noted in the Inductor Ripple Current vs Duty Cycle graph (Figure 3) where I_L ≈ 10A at 25% duty cycle. The inductor ripple current can be lowered at the higher input voltages by adding an external resistor from f_{SET} to ground to increase the switching frequency. An 8A ripple current is chosen, and the total peak current is equal to 1/2 of the 8A ripple current plus the output current. The 5V output current is limited to 8A, so the total peak current is less than 12A. This is below the 14A peak specified value. A 100k resistor is placed from f_{SET} to ground, and the parallel combination of 100k and 39.2k equates to 28k. The I_{fSET} calculation with 28k and 20V input voltage equals 238μA. This equates to a t_{ON} of 200ns. This will increase the switching frequency from ~886kHz to ~1.25MHz for the 20V to 5V conversion. The minimum on-time is above 100ns at 20V input. Since the switching frequency is approximately constant over input and output conditions, then the lower input voltage range is limited to 10V for the 1.25MHz operation due to the 400ns minimum off-time. Equation: t_{ON} = (V_{OUT}/V_{IN}) • (1/Frequency) equates to a 400ns on-time, and a 400ns off-time. The V_{IN} to V_{OUT} Step-Down Ratio curve reflects an operating range of 10V to 20V for 1.25MHz operation with a 100k resistor to ground, and an 8V to 16V operation for f_{SET} floating. These modifications are made to provide wider input voltage ranges for the 5V output designs while limiting the inductor ripple current, and maintaining the 400ns minimum off-time.

Example for 3.3V Output

LTM4601A minimum on-time = 100ns
t_{ON} = ((V_{OUT} • 10pF)/I_{fSET})

LTM4601A minimum off-time = 400ns
t_{OFF} = t – t_{ON}, where t = 1/Frequency

Duty Cycle (DC) = t_{ON}/t or V_{OUT}/V_{IN}

Equations for setting frequency:

I_{fSET} = (V_{IN}/(3 • R_{fSET})), for 20V operation, I_{fSET} = 170μA, t_{ON} = ((3.3 • 10pF)/I_{fSET}), t_{ON} = 195ns, where the internal R_{fSET} is 39.2k. Frequency = (V_{OUT}/(V_{IN} • t_{ON})) = (3.3V/(20 • 195ns)) ≈ 846kHz. The minimum on-time and minimum off-time are within specification at 195ns and 980ns. The 4.5V minimum input for converting 3.3V output will not meet the minimum off-time specification of 400ns. t_{ON} = 868ns, Frequency = 850kHz, t_{OFF} = 315ns.

Solution

Lower the switching frequency at lower input voltages to allow for higher duty cycles, and meet the 400ns minimum off-time at 4.5V input voltage. The off-time should be about 500ns, which includes a 100ns guard band. The duty cycle for (3.3V/4.5V) ≈ 73%. Frequency = (1 – DC)/t_{OFF}, or (1 – 0.73)/500ns = 540kHz. The switching frequency needs to be lowered to 540kHz at 4.5V input. t_{ON} = DC/frequency, or 1.35μs. The f_{SET} pin voltage is 1/3 of V_{IN}, and the I_{fSET} current equates to 38μA with the internal 39.2k. The I_{fSET} current needs to be 24μA for 540kHz operation. A resistor can be placed from V_{OUT} to f_{SET} to lower the effective I_{fSET} current out of the f_{SET} pin to 24μA. The f_{SET} pin is 4.5V/3 =1.5V and V_{OUT} = 3.3V, therefore 130k will source 14μA into the f_{SET} node and lower the I_{fSET} current to 24μA. This enables the 540kHz operation and the 4.5V to 20V input operation for down converting to 3.3V output. The frequency will scale from 540kHz to 1.1MHz over this input range. This provides for an effective output current of 8A over the input range.

APPLICATIONS INFORMATION

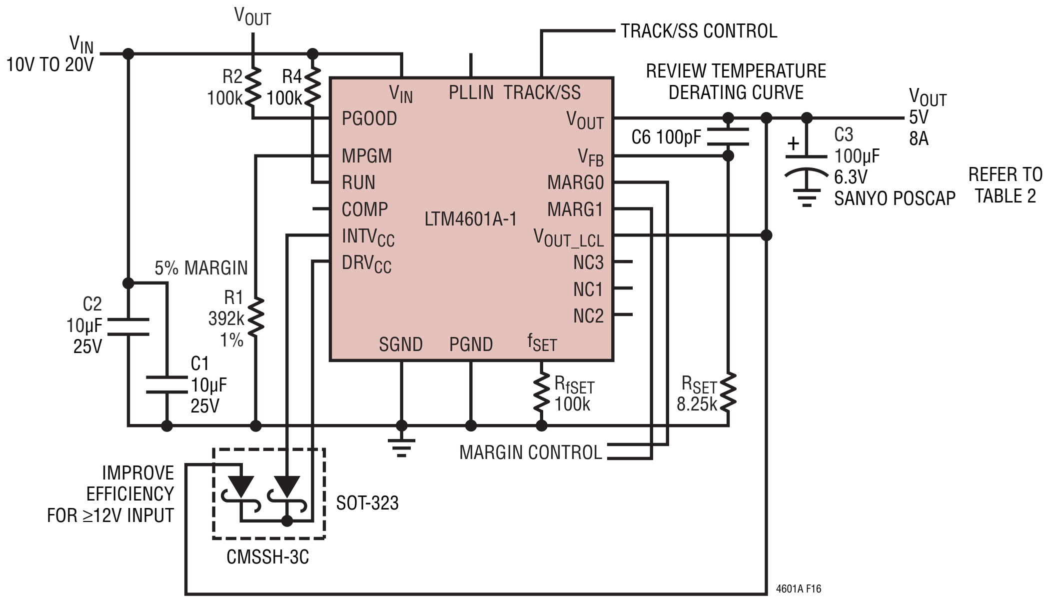


Figure 16. 5V at 8A Design Without Differential Amplifier

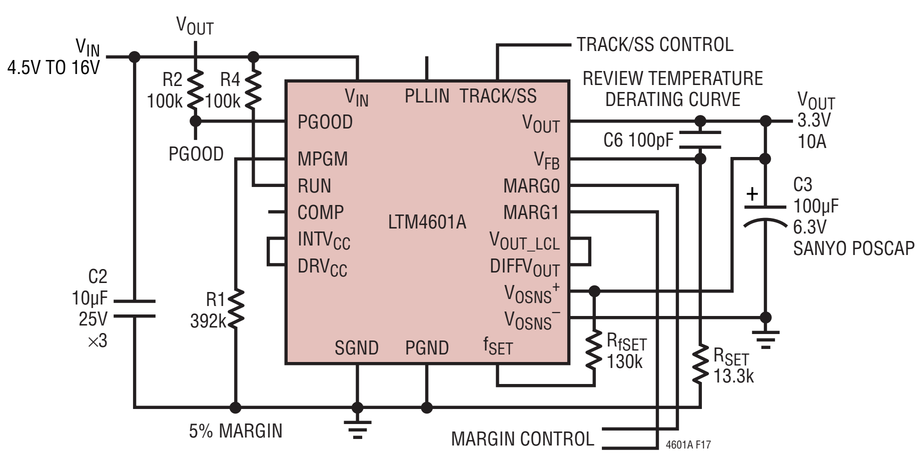


Figure 17. 3.3V at 10A Design

APPLICATIONS INFORMATION

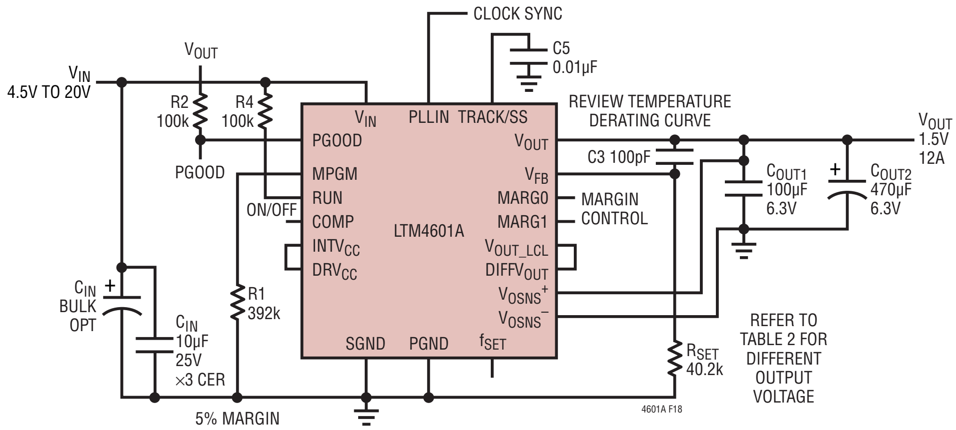
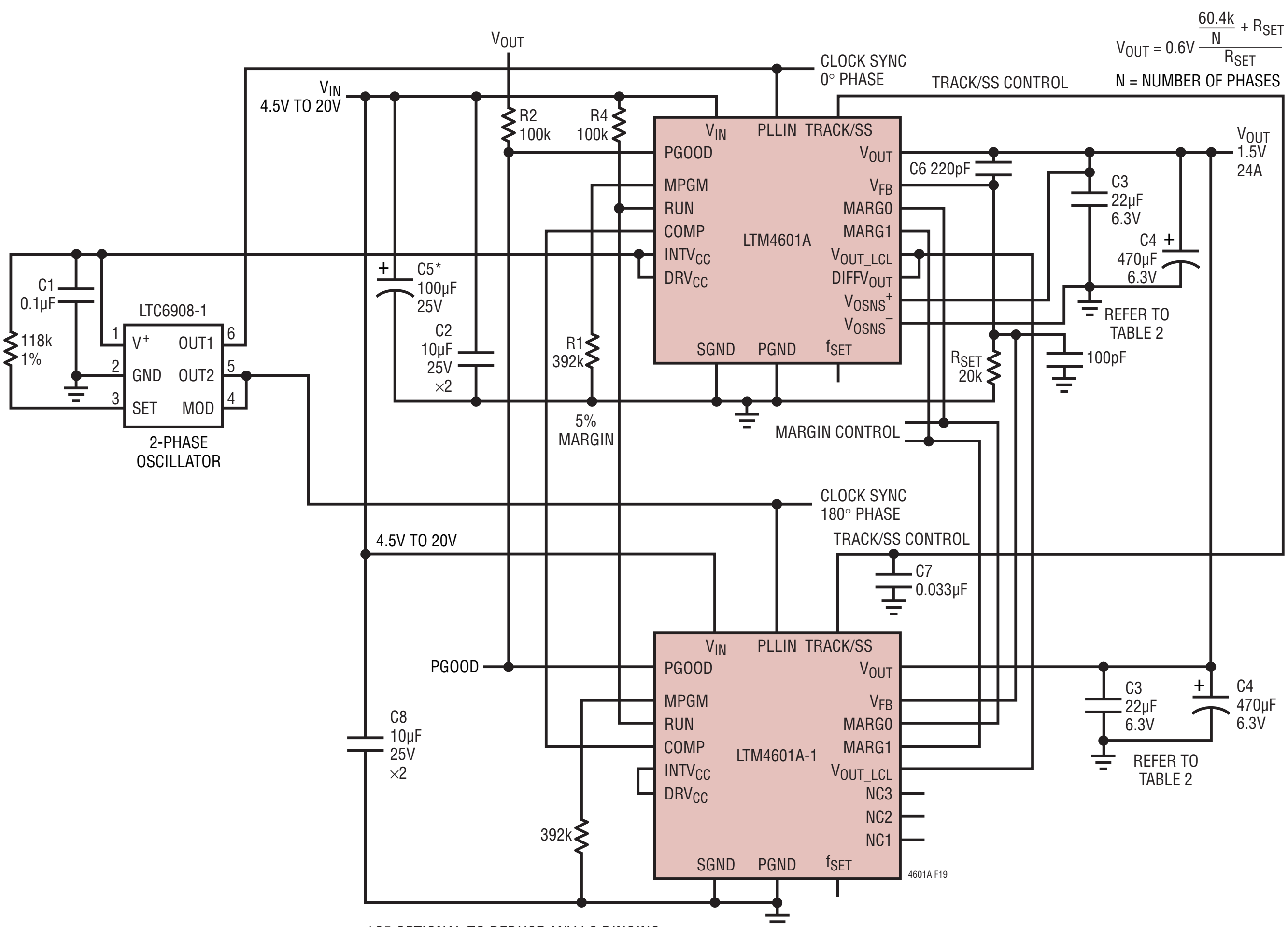


Figure 18. Typical 4.5V to 20V, 1.5V at 12A Design



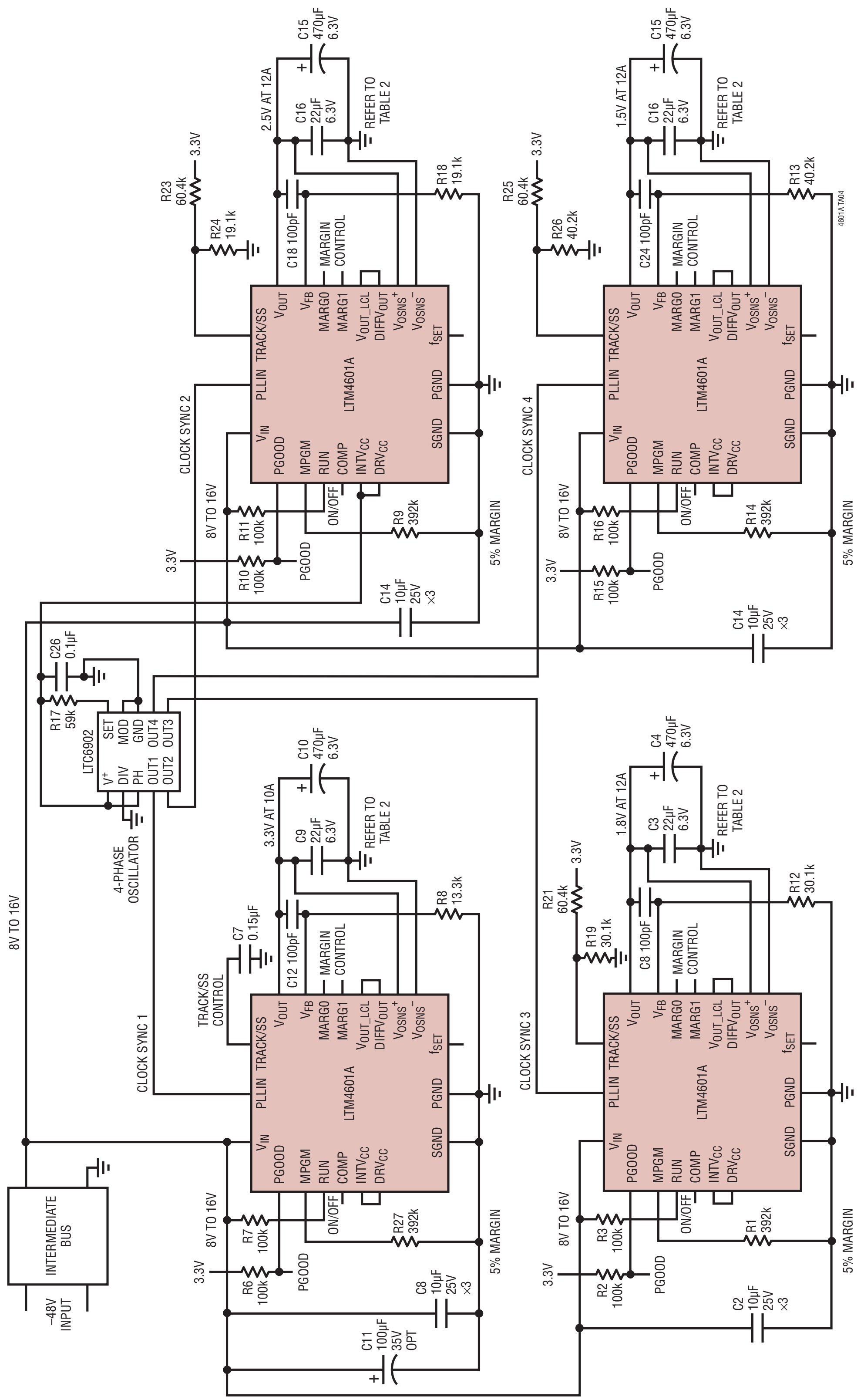
$V_{OUT} = 0.6V \dfrac{\frac{60.4k}{N} + R_{SET}}{R_{SET}}$

*C5 OPTIONAL TO REDUCE ANY LC RINGING.
NOT NEEDED FOR LOW INDUCTANCE PLANE CONNECTION

Figure 19. 2-Phase Parallel, 1.5V at 24A Design

TYPICAL APPLICATIONS

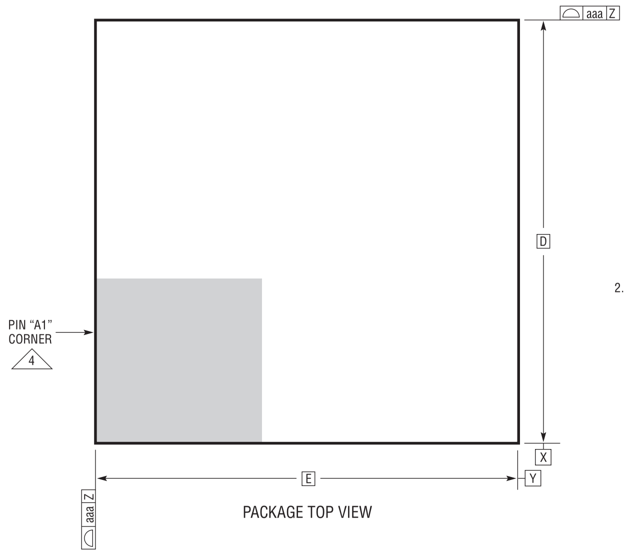
4-Phase, Four Outputs (3.3V, 2.5V, 1.8V and 1.5V) with Coincident Tracking



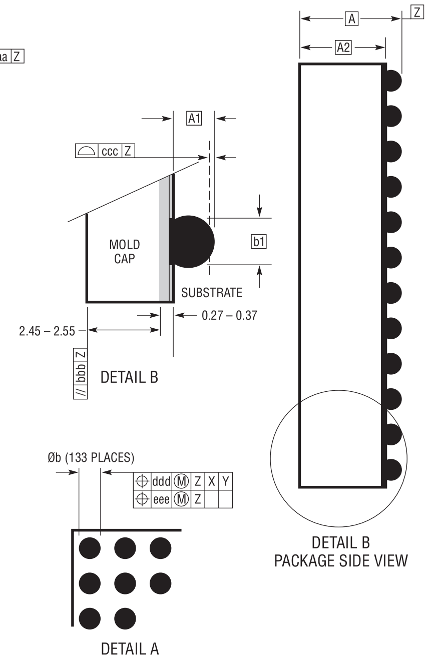
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

BGA Package
133-Lead (15mm × 15mm × 3.42mm)
(Reference LTM DWG # 05-08-1877 Rev B)



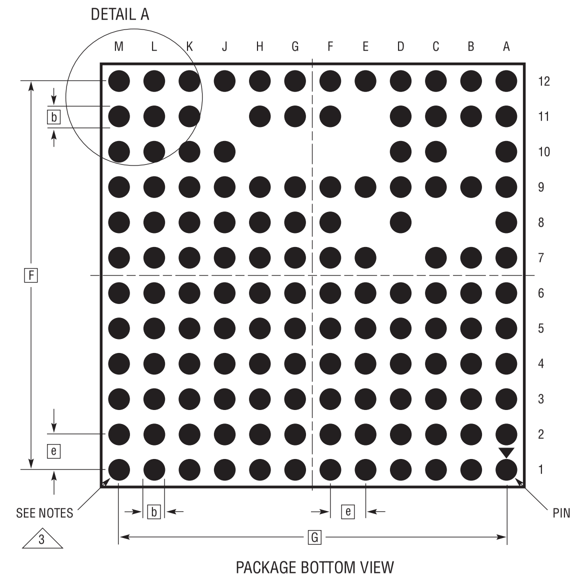
PACKAGE TOP VIEW



DETAIL B

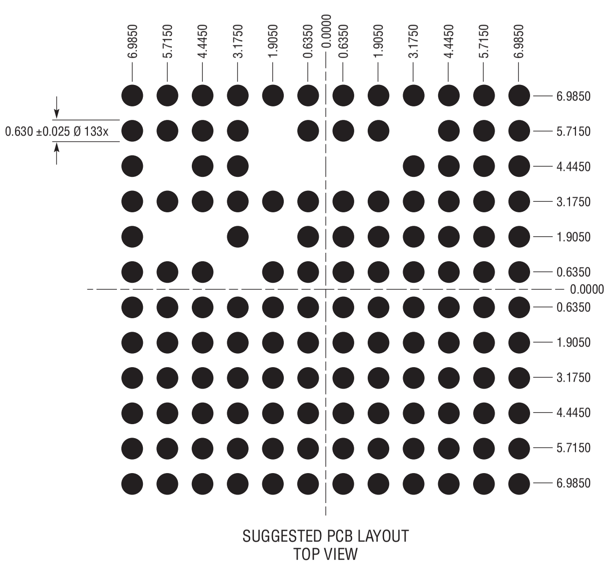
DETAIL A

DETAIL B
PACKAGE SIDE VIEW



PACKAGE BOTTOM VIEW

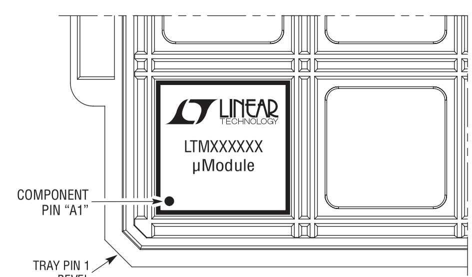
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE



SUGGESTED PCB LAYOUT
TOP VIEW

	DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.0		
E		15.0		
e		1.27		
F		13.97		
G		13.97		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	

TOTAL NUMBER OF BALLS: 133



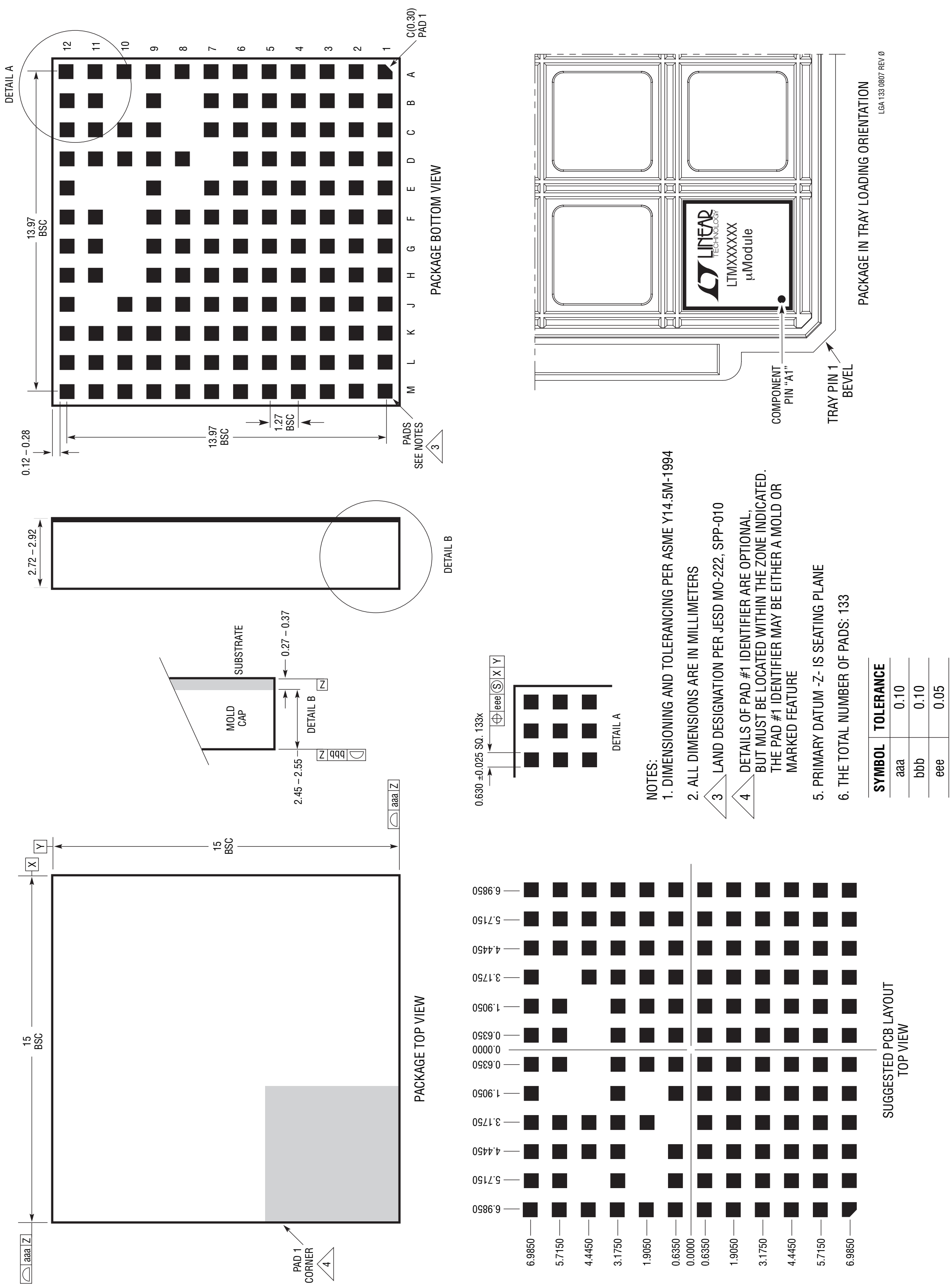
PACKAGE IN TRAY LOADING ORIENTATION

BGA 133 0511 REV B

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

LGA Package
133-Lead (15mm × 15mm × 2.82mm)
(Reference LTM DWG # 05-08-1755, Rev Ø)



4601afc

PACKAGE DESCRIPTION

**Pin Assignment Table 5
(Arranged by Pin Number)**

PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME	
A1	V_{IN}	B1	V_{IN}	C1	V_{IN}	D1	PGND	E1	PGND	F1	PGND
A2	V_{IN}	B2	V_{IN}	C2	V_{IN}	D2	PGND	E2	PGND	F2	PGND
A3	V_{IN}	B3	V_{IN}	C3	V_{IN}	D3	PGND	E3	PGND	F3	PGND
A4	V_{IN}	B4	V_{IN}	C4	V_{IN}	D4	PGND	E4	PGND	F4	PGND
A5	V_{IN}	B5	V_{IN}	C5	V_{IN}	D5	PGND	E5	PGND	F5	PGND
A6	V_{IN}	B6	V_{IN}	C6	V_{IN}	D6	PGND	E6	PGND	F6	PGND
A7	$INTV_{CC}$	B7	PGND	C7	PGND	D7	-	E7	PGND	F7	PGND
A8	PLLIN	B8	-	C8	-	D8	PGND	E8	-	F8	PGND
A9	TRACK/SS	B9	PGND	C9	PGND	D9	$INTV_{CC}$	E9	PGND	F9	PGND
A10	RUN	B10	-	C10	MTP1	D10	MPT2	E10	-	F10	-
A11	COMP	B11	MPGM	C11	f_{SET}	D11	MPT3	E11	-	F11	PGOOD
A12	MPGM	B12	f_{SET}	C12	MARG0	D12	MARG1	E12	DRV_{CC}	F12	V_{FB}

PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME	
G1	PGND	H1	PGND	J1	V_{OUT}	K1	V_{OUT}	L1	V_{OUT}	M1	V_{OUT}
G2	PGND	H2	PGND	J2	V_{OUT}	K2	V_{OUT}	L2	V_{OUT}	M2	V_{OUT}
G3	PGND	H3	PGND	J3	V_{OUT}	K3	V_{OUT}	L3	V_{OUT}	M3	V_{OUT}
G4	PGND	H4	PGND	J4	V_{OUT}	K4	V_{OUT}	L4	V_{OUT}	M4	V_{OUT}
G5	PGND	H5	PGND	J5	V_{OUT}	K5	V_{OUT}	L5	V_{OUT}	M5	V_{OUT}
G6	PGND	H6	PGND	J6	V_{OUT}	K6	V_{OUT}	L6	V_{OUT}	M6	V_{OUT}
G7	PGND	H7	PGND	J7	V_{OUT}	K7	V_{OUT}	L7	V_{OUT}	M7	V_{OUT}
G8	PGND	H8	PGND	J8	V_{OUT}	K8	V_{OUT}	L8	V_{OUT}	M8	V_{OUT}
G9	PGND	H9	PGND	J9	V_{OUT}	K9	V_{OUT}	L9	V_{OUT}	M9	V_{OUT}
G10	-	H10	-	J10	V_{OUT}	K10	V_{OUT}	L10	V_{OUT}	M10	V_{OUT}
G11	SGND	H11	SGND	J11	-	K11	V_{OUT}	L11	V_{OUT}	M11	V_{OUT}
G12	PGOOD	H12	SGND	J12	V_{OSNS}^{+}	K12	$DIFFV_{OUT}$	L12	V_{OUT_LCL}	M12	V_{OSNS}^{-}

PACKAGE DESCRIPTION

Pin Assignment Table 6 (Arranged by Pin Function)

PIN	NAME
A1	V_{IN}
A2	V_{IN}
A3	V_{IN}
A4	V_{IN}
A5	V_{IN}
A6	V_{IN}
B1	V_{IN}
B2	V_{IN}
B3	V_{IN}
B4	V_{IN}
B5	V_{IN}
B6	V_{IN}
C1	V_{IN}
C2	V_{IN}
C3	V_{IN}
C4	V_{IN}
C5	V_{IN}
C6	V_{IN}

PIN	NAME
D1	PGND
D2	PGND
D3	PGND
D4	PGND
D5	PGND
D6	PGND
D8	PGND
E1	PGND
E2	PGND
E3	PGND
E4	PGND
E5	PGND
E6	PGND
E7	PGND
F1	PGND
F2	PGND
F3	PGND
F4	PGND
F5	PGND
F6	PGND
F7	PGND
F8	PGND
F9	PGND
G1	PGND
G2	PGND
G3	PGND
G4	PGND
G5	PGND
G6	PGND
G7	PGND
G8	PGND
G9	PGND
H1	PGND
H2	PGND
H3	PGND
H4	PGND
H5	PGND
H6	PGND
H7	PGND
H8	PGND
H9	PGND

PIN	NAME
J1	V_{OUT}
J2	V_{OUT}
J3	V_{OUT}
J4	V_{OUT}
J5	V_{OUT}
J6	V_{OUT}
J7	V_{OUT}
J8	V_{OUT}
J9	V_{OUT}
J10	V_{OUT}
K1	V_{OUT}
K2	V_{OUT}
K3	V_{OUT}
K4	V_{OUT}
K5	V_{OUT}
K6	V_{OUT}
K7	V_{OUT}
K8	V_{OUT}
K9	V_{OUT}
K10	V_{OUT}
K11	V_{OUT}
L1	V_{OUT}
L2	V_{OUT}
L3	V_{OUT}
L4	V_{OUT}
L5	V_{OUT}
L6	V_{OUT}
L7	V_{OUT}
L8	V_{OUT}
L9	V_{OUT}
L10	V_{OUT}
L11	V_{OUT}
M1	V_{OUT}
M2	V_{OUT}
M3	V_{OUT}
M4	V_{OUT}
M5	V_{OUT}
M6	V_{OUT}
M7	V_{OUT}
M8	V_{OUT}
M9	V_{OUT}
M10	V_{OUT}
M11	V_{OUT}

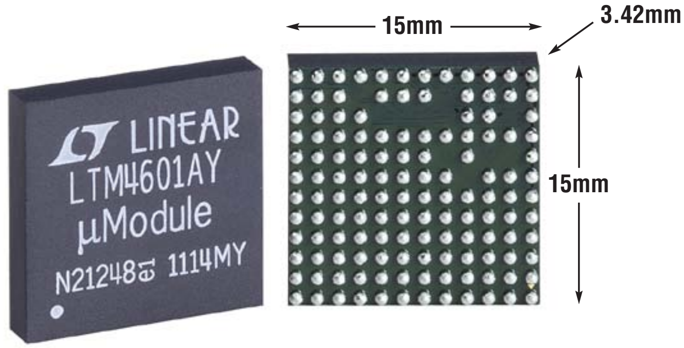
PIN	NAME
A7	$INTV_{CC}$
A8	PLLIN
A9	TRACK/SS
A10	RUN
A11	COMP
A12	MPGM
B12	f_{SET}
C12	MARG0
D12	MARG1
E12	DRV_{CC}
F12	V_{FB}
G12	PGOOD
H12	SGND
J12	V_{OSNS}^+
K12	$DIFFV_{OUT}$
L12	V_{OUT_LCL}
M12	V_{OSNS}^-

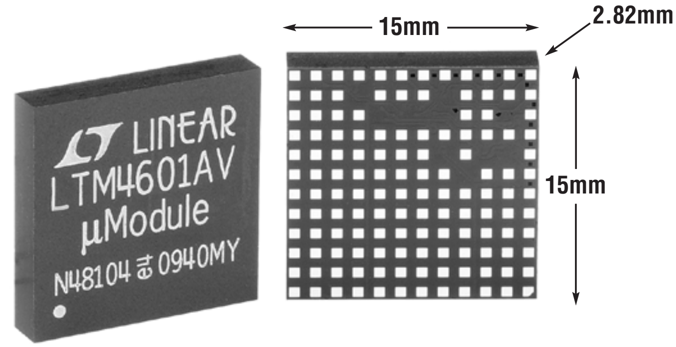
PIN	NAME
B7	PGND
B8	-
B9	PGND
B10	-
B11	MPGM
C7	PGND
C8	-
C9	PGND
C10	MTP1
C11	f_{SET}
D7	-
D8	PGND
D9	$INTV_{CC}$
D10	MTP2
D11	MTP3
E8	-
E9	PGND
E10	-
E11	-
F10	-
F11	PGOOD
G10	-
G11	SGND
H10	-
H11	SGND
J11	-

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	8/11	Added BGA package. Changes reflected throughout the data sheet.	1 to 30

PACKAGE PHOTOS





RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2900	Quad Supply Monitor with Adjustable Reset Timer	Monitors Four Supplies; Adjustable Reset Timer
LTC2923	Power Supply Tracking Controller	Tracks Both Up and Down; Power Supply Sequencing
LT3825/LT3837	Synchronous Isolated Flyback Controllers	No Opto-coupler Required; 3.3V, 12A Output; Simple Design
LTM4600	10A DC/DC µModule Regulator	Basic 10A DC/DC µModule Regulator
LTM4601	12A DC/DC µModule Regulator with PLL, Output Tracking/ Margining and Remote Sensing	Synchronizable, PolyPhase Operation to 48A, LTM4601-1 Version Has No Remote Sensing
LTM4602	6A DC/DC µModule Regulator	Pin Compatible with the LTM4600
LTM4603	6A DC/DC µModule Regulator with PLL and Output Tracking/Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4603-1 Version Has No Remote Sensing, Pin Compatible with the LTM4601
LTM4604A	4A Low Voltage DC/DC µModule Regulator	$2.7V \le V_{IN} \le 5.5V$; $0.8V \le V_{OUT} \le 5V$, 15mm × 9mm × 2.32mm (Ultrathin) LGA Package
LTM4608A	8A Low Voltage DC/DC µModule Regulator	$2.7V \le V_{IN} \le 5.5V$; $0.6V \le V_{OUT} \le 5V$; 15mm × 9mm × 2.82mm LGA Package

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