# 1-Kbit to 16-Kbit UNI/O® Serial EEPROM Family Data Sheet

## Features

- Single I/O, UNI/O® Serial Interface Bus
- Low-Power CMOS Technology:
  - 1 mA active current, typical
  - 1 µA standby current (max.) (I-temp)
- 128 x 8 through 2,048 x 8 Bit Organizations
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kbps Max. Bit Rate – Equivalent to 100 kHz Clock Frequency
- Self-Timed Write Cycle (including Auto-Erase)
- Page-Write Buffer for up to 16 Bytes
- STATUS Register for Added Control:
  - Write enable latch bit
  - Write-In-Progress bit
- Block Write Protection:
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
- High Reliability:
  - Endurance: 1,000,000 erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4,000V
- RoHS Compliant
- Available Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- Automotive AEC-Q100 Qualified

## Packages

- 3-lead SOT-23 and TO-92 Packages
- 4-lead Chip Scale Package
- 8-lead PDIP, SOIC, MSOP and TDFN Packages

## Pin Function Table

| Name | Function |
|---|---|
| SCIO | Serial Clock, Data Input/Output |
| Vss | Ground |
| Vcc | Supply Voltage |

## Description

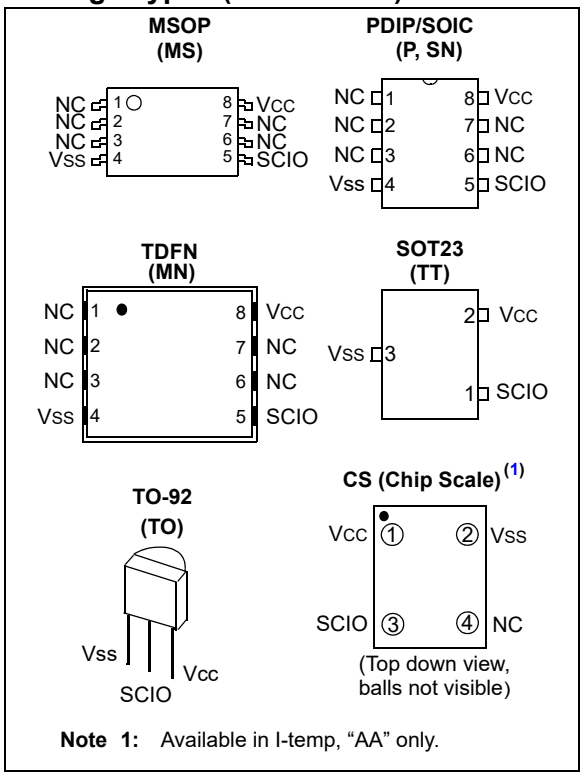
The Microchip Technology Inc. 11AAXXX/11LCXXX (11XX(1)) devices are a family of 1-Kbit through 16-Kbit Serial Electrically Erasable PROMs. The devices are organized in blocks of x8-bit memory and support the patented(2) single I/O UNI/O® serial bus. By using Manchester encoding techniques, the clock and data are combined into a single, serial bit stream (SCIO), where the clock signal is extracted by the receiver to correctly decode the timing and value of each bit.

Low-voltage design permits operation down to 1.8V (for 11AAXXX devices), with standby and active currents of only 1 µA and 1 mA, respectively.

**Note 1:** 11XX is used in this document as a generic part number for the 11 series devices.

**2:** Microchip's UNI/O® Bus products are covered by some or all of the following patents issued in the U.S.A.: 7.376,020 & 7,788,430.

## Package Types (not to scale)




**Note 1:** Available in I-temp, "AA" only.

## DEVICE SELECTION TABLE

| Part Number | Density (bits) | Organization | Vcc Range | Page Size (Bytes) | Temp. Ranges | Device Address | Packages |
|---|---|---|---|---|---|---|---|
| 11LC010 | 1 Kbit | 128 x 8 | 2.5V-5.5V | 16 | I,E | 0xA0 | P, SN, MS, MN, TO, TT |
| 11AA010 | 1 Kbit | 128 x 8 | 1.8V-5.5V | 16 | I | 0xA0 | P, SN, MS, MN, TO, TT, CS |
| 11LC020 | 2 Kbit | 256 x 8 | 2.5V-5.5V | 16 | I,E | 0xA0 | P, SN, MS, MN, TO, TT |
| 11AA020 | 2 Kbit | 256 x 8 | 1.8V-5.5V | 16 | I | 0xA0 | P, SN, MS, MN, TO, TT, CS |
| 11LC040 | 4 Kbit | 512 x 8 | 2.5V-5.5V | 16 | I,E | 0xA0 | P, SN, MS, MN, TO, TT |
| 11AA040 | 4 Kbit | 512 x 8 | 1.8V-5.5V | 16 | I | 0xA0 | P, SN, MS, MN, TO, TT, CS |
| 11LC080 | 8 Kbit | 1,024 x 8 | 2.5V-5.5V | 16 | I,E | 0xA0 | P, SN, MS, MN, TO, TT |
| 11AA080 | 8 Kbit | 1,024 x 8 | 1.8V-5.5V | 16 | I | 0xA0 | P, SN, MS, MN, TO, TT, CS |
| 11LC160 | 16 Kbit | 2,048 x 8 | 2.5V-5.5V | 16 | I,E | 0xA0 | P, SN, MS, MN, TO, TT |
| 11AA160 | 16 Kbit | 2,048 x 8 | 1.8V-5.5V | 16 | I | 0xA0 | P, SN, MS, MN, TO, TT,CS |
| 11LC161 | 16 Kbit | 2,048 x 8 | 2.5V-5.5V | 16 | I, E | 0xA1 | P, SN, MS, MN, TO, TT |
| 11AA161 | 16 Kbit | 2,048 x 8 | 1.8V-5.5V | 16 | I | 0xA1 | P, SN, MS, MN, TO, TT, CS |

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings (†)

VCC.....6.5V

SCIO w.r.t. VSS.....-0.6V to VCC+1.0V

Storage temperature.....-65°C to 150°C

Ambient temperature under bias.....-40°C to 125°C

ESD protection on all pins.....4 kV

**†** NOTICE**:** Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

| **DC CHARACTERISTICS** | | | **Electrical Characteristics:**<br>**Industrial (I):** **VCC = 2.5V to 5.5V** **TA = -40°C to +85°C**<br>**VCC = 1.8V to 2.5V** **TA = -20°C to +85°C**<br>**Extended (E):** **VCC = 2.5V to 5.5V** **TA = -40°C to +125°C** | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Max.** | **Units** | **Test Conditions** |
| D1 | VIH | High-level input voltage | 0.7*VCC | VCC+1 | V | — |
| D2 | VIL | Low-level input voltage | -0.3 | 0.3*VCC | V | VCC ≥ 2.5V |
| | | | -0.3 | 0.2*VCC | V | VCC < 2.5V |
| D3 | VHYS | Hysteresis of Schmitt Trigger inputs (SCIO) | 0.05*Vcc | — | V | VCC ≥ 2.5V **(Note 1)** |
| D4 | VOH | High-level output voltage | VCC -0.5 | — | V | IOH = -300 µA, VCC = 5.5V |
| | | | VCC -0.5 | — | V | IOH = -200 µA, Vcc = 2.5V |
| D5 | VOL | Low-level output voltage | — | 0.4 | V | IOI = 300 µA, VCC = 5.5V |
| | | | — | 0.4 | V | IOI = 200 µA, Vcc = 2.5V |
| D6 | IO | Output current limit **(Note 2)** | — | ±4 | mA | VCC = 5.5V **(Note 1)** |
| | | | — | ±3 | mA | Vcc = 2.5V **(Note 1)** |
| D7 | ILI | Input leakage current (SCIO) | — | ±1 | µA | VIN = VSS or VCC |
| D8 | CINT | Internal Capacitance (all inputs and outputs) | — | 7 | pF | TA = 25°C, FCLK = 1 MHz, VCC = 5.0V **(Note 1)** |
| D9 | ICC Read | Read Operating Current | — | 3 | mA | VCC=5.5V; FBUS=100 kHz, CB=100 pF |
| | | | — | 1 | mA | VCC=2.5V; FBUS=100 kHz, CB=100 pF |
| D10 | ICC Write | Write Operating Current | — | 5 | mA | VCC = 5.5V |
| | | | — | 3 | mA | VCC = 2.5V |
| D11 | Iccs | Standby Current | — | 5 | µA | VCC = 5.5V<br>TA = 125°C |
| | | | — | 1 | µA | VCC = 5.5V<br>TA = 85°C |
| D12 | ICCI | Idle Mode Current | — | 50 | µA | VCC = 5.5V |

**Note 1:** This parameter is periodically sampled and is not 100% tested.

**2:** The SCIO output driver impedance will vary to ensure IO is not exceeded.

**TABLE 1-2: AC CHARACTERISTICS**

| AC CHARACTERISTICS | | | Electrical Characteristics:<br>Industrial (I): VCC = 2.5V to 5.5V TA = -40°C to +85°C<br>VCC = 1.8V to 2.5V TA = -20°C to +85°C<br>Extended (E): VCC = 2.5V to 5.5V TA = -40°C to +125°C | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Max.** | **Units** | **Test Conditions** |
| 1 | FBUS | Serial bus frequency | 10 | 100 | kHz | — |
| 2 | TE | Bit period | 10 | 100 | µs | — |
| 3 | TIJIT | Input edge jitter tolerance | — | ±0.06 | UI | (Note 2) |
| 4 | FDRIFT | Serial bus frequency drift rate tolerance | — | ±0.50 | % per byte | — |
| 5 | FDEV | Serial bus frequency drift limit | — | ±5 | % per command | — |
| 6 | TOJIT | Output edge jitter | — | ±0.25 | UI | (Note 2) |
| 7 | TR | SCIO input rise time (Note 1) | — | 100 | ns | — |
| 8 | TF | SCIO input fall time (Note 1) | — | 100 | ns | — |
| 9 | TSTBY | Standby pulse time | 600 | — | µs | — |
| 10 | TSS | Start header setup time | 10 | — | µs | — |
| 11 | THDR | Start header low pulse time | 5 | — | µs | — |
| 12 | TSP | Input filter spike suppression (SCIO) | — | 50 | ns | (Note 1) |
| 13 | TWC | Write cycle time (byte or page) | — | 5 | m | Write, WRSR commands |
| | | | — | 10 | ms | ERAL, SETAL commands |
| 14 | — | Endurance (per page) | 1M | — | cycles | 25°C, VCC = 5.5V |

**Note 1:** This parameter is periodically sampled and is not 100% tested.

**2:** A Unit Interval (UI) is equal to 1-bit period (TE) at the current bus frequency.

**3:** This parameter is not tested but ensured by characterization.

**TABLE 1-3: AC TEST CONDITIONS**

| **AC Waveform:** | |
|---|---|
| VLO = 0.2V | |
| VHI = VCC - 0.2V | |
| CL = 100 pF | |
| **Timing Measurement Reference Level** | |
| Input | 0.5 VCC |
| Output | 0.5 VCC |

**FIGURE 1-1: BUS TIMING – START HEADER**

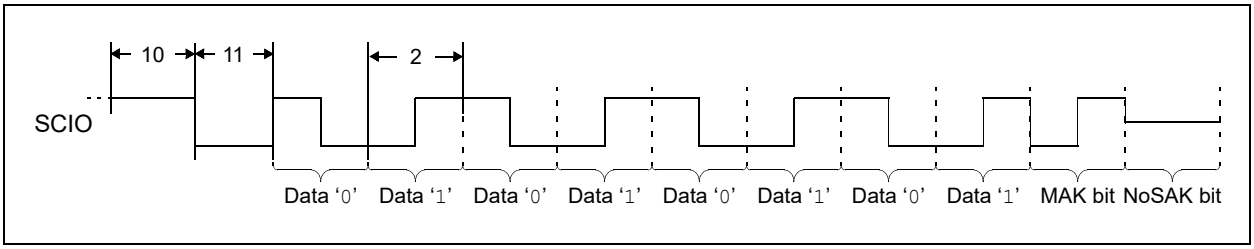



**FIGURE 1-2: BUS TIMING – DATA**

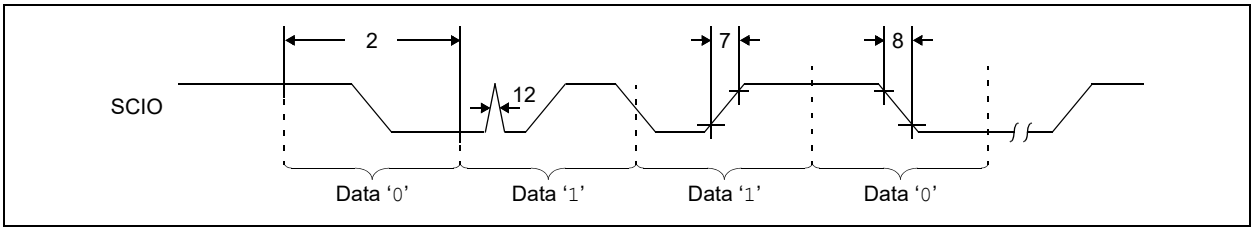



**FIGURE 1-3: BUS TIMING – STANDBY PULSE**

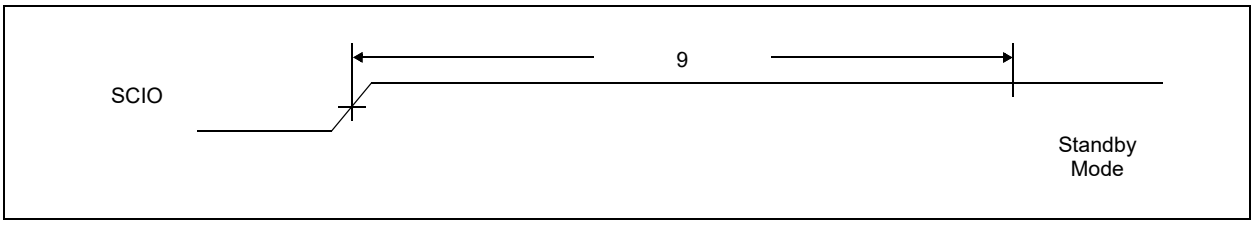
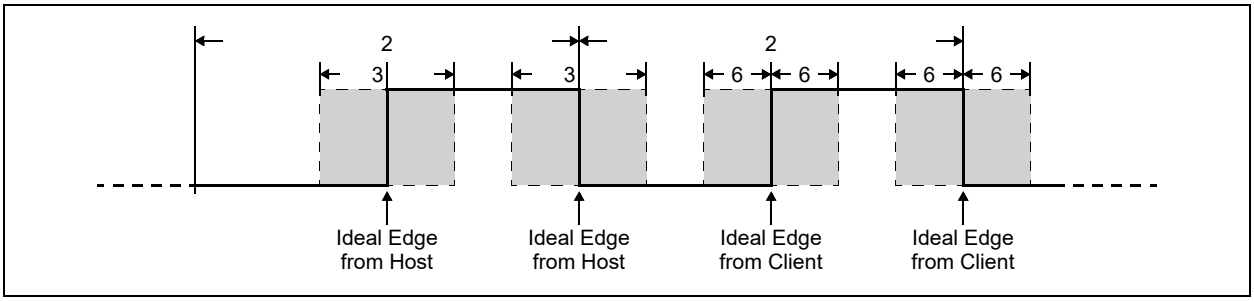



**FIGURE 1-4: BUS TIMING – JITTER**



## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Name | 3-pin SOT-23 | 3-pin TO-92 | 4-pin CS | 8-pin PDIP/SOIC/ MSOP/TDFN | Description |
|---|---|---|---|---|---|
| SCIO | 1 | 2 | 3 | 5 | Serial Clock, Data Input/Output |
| VCC | 2 | 3 | 1 | 8 | Supply Voltage |
| VSS | 3 | 1 | 2 | 4 | Ground |
| NC | — | — | 4 | 1,2,3,6,7 | No Internal Connection |

### 2.1 Serial Clock, Data Input/Output (SCIO)

SCIO is a bidirectional pin used to transfer commands and addresses into, as well as data into and out of, the device. The serial clock is embedded into the data stream through Manchester encoding. Each bit is represented by a signal transition at the middle of the bit period.

# 3.0 FUNCTIONAL DESCRIPTION

## 3.1 Principles of Operation

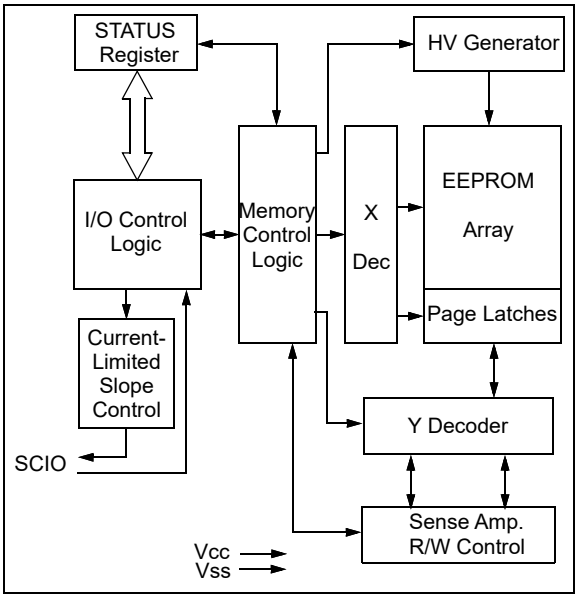
The 11AAXXX/11LCXXX family of serial EEPROMs support the UNI/O® protocol. They can be interfaced with microcontrollers, including Microchip's PIC® microcontrollers, ASICs, or any other device with an available discrete I/O line that can be configured properly to match the UNI/O protocol.

The 11AAXXX/11LCXXX devices contain an 8-bit instruction register. The devices are accessed via the SCIO pin.

Table 5-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSb first, LSb last.

Data is embedded into the I/O stream through Manchester encoding. The bus is controlled by a host device which determines the clock period, controls the bus access and initiates all operations, while the 11AAXXX/11LCXXX works as client. Both host and client can operate as transmitter or receiver, but the host device determines which mode is active.

**FIGURE 3-1: BLOCK DIAGRAM**



## 4.0 BUS CHARACTERISTICS

### 4.1 Standby Pulse

When the host has control of SCIO, a standby pulse can be generated by holding SCIO high for TSTBY. At this time, the 11AAXXX/11LCXXX will reset and return to Standby mode. Subsequently, a high-to-low transition on SCIO (the first low pulse of the header) will return the device to the active state.

Once a command is terminated satisfactorily (i.e., via a NoMAK/SAK combination during the Acknowledge sequence), performing a standby pulse is not required to begin a new command as long as the device to be selected is the same device selected during the previous command. However, a period of TSS must be observed after the end of the command and before the beginning of the start header. After TSS, the start header (including THDR low pulse) can be transmitted in order to begin the new command.

If a command is terminated in any manner other than a NoMAK/SAK combination, then the host must perform a standby pulse before beginning a new command, regardless of which device is to be selected.

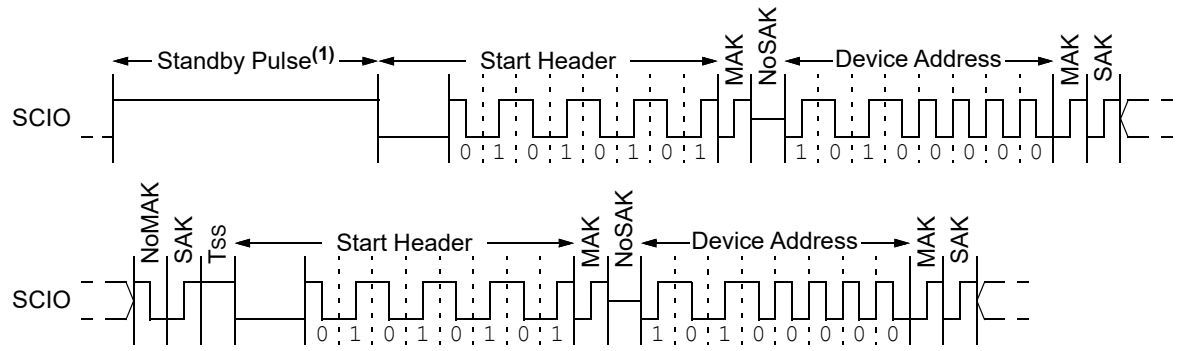
| | |
|---|---|
| **Note:** | After a POR/BOR event occurs, a low-to-high transition on SCIO must be generated before proceeding with communication, including a standby pulse. |

An example of two consecutive commands is shown in Figure 4-1. Note that the device address is the same for both commands, indicating that the same device is being selected both times.

A standby pulse cannot be generated while the client has control of SCIO. In this situation, the host must wait for the client to finish transmitting and to release SCIO before the pulse can be generated.

If, at any point during a command, an error is detected by the host, a standby pulse should be generated and the command should be performed again.

**FIGURE 4-1: CONSECUTIVE COMMANDS EXAMPLE**




**Note 1:** After a POR/BOR event, a low-to-high transition on SCIO must occur before the first standby pulse.

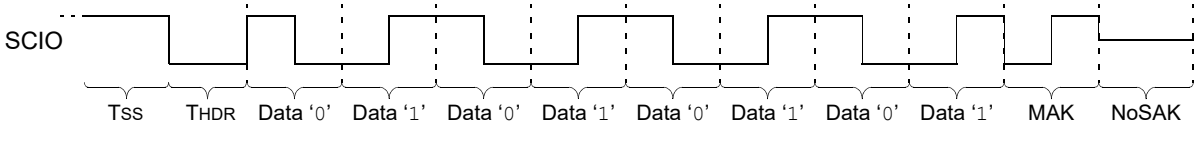
### 4.2 Start Data Transfer

All operations must be preceded by a start header. The start header consists of holding SCIO low for a period of THDR, followed by transmitting an 8-bit '01010101' code. This code is used to synchronize the client's internal clock period with the host's clock period, so accurate timing is very important.

When a standby pulse is not required (i.e., between successive commands to the same device), a period of TSS must be observed at the end of the command and before the beginning of the start header.

Figure 4-2 shows the waveform for the start header, including the required Acknowledge sequence at the end of the byte.

**FIGURE 4-2: START HEADER**



## 4.3 Acknowledge

An Acknowledge routine occurs after each byte is transmitted, including the start header. This routine consists of two bits. The first bit is transmitted by the host, and the second bit is transmitted by the client.

**Note:** A MAK must always be transmitted following the start header.

The Host Acknowledge, or MAK, is signified by transmitting a '1', and informs the client that the current operation is to be continued. Conversely, a Not Acknowledge, or NoMAK, is signified by transmitting a '0', and is used to end the current operation (and initiate the write cycle for write operations).

**Note:** When a NoMAK is used to end a WRITE or WRSR instruction, the write cycle is not initiated if no bytes of data have been received.

The Client Acknowledge, or SAK, is also signified by transmitting a '1', and confirms proper communication. However, unlike the NoMAK, the NoSAK is signified by the lack of a middle edge during the bit period.

**Note:** To guard against bus contention, a NoSAK will occur after the start header.

A NoSAK will occur for the following events:

- Following the start header
- Following the device address, if no client on the bus matches the transmitted address
- Following the command byte, if the command is invalid, including Read, CRRD, Write, WRSR, SETAL and ERAL during a write cycle.
- If the client becomes out of sync with the host
- If a command is terminated prematurely by using a NoMAK, with the exception of immediately after the device address.

See Figure 4-3 and Figure 4-4 for details.

If a NoSAK is received from the client after any byte (except the start header), an error has occurred. The host should then perform a standby pulse and begin the desired command again.

**FIGURE 4-3: ACKNOWLEDGE ROUTINE**

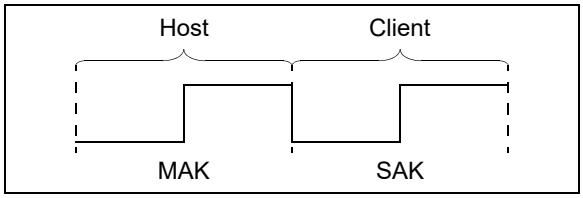
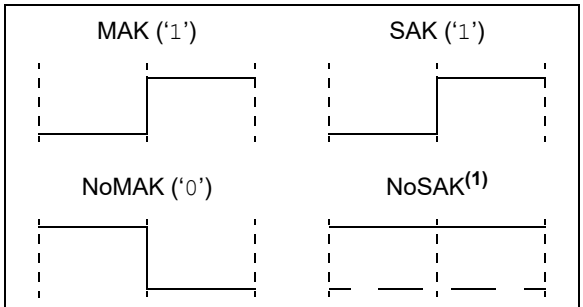



**FIGURE 4-4: ACKNOWLEDGE BITS**



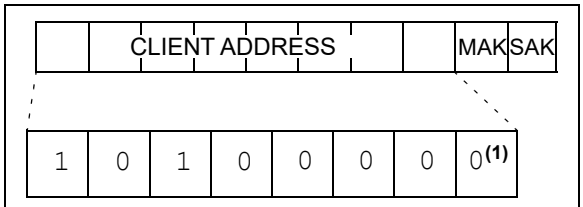

**Note 1:** A NoSAK is defined as any sequence that is not a valid SAK.

## 4.4 Device Addressing

A device address byte is the first byte received from the host device following the start header. The device address byte consists of a four-bit family code. For the 11AAXXX/11LCXXX, this is set as '1010'. The last four bits of the device address byte are the device code, which is hardwired to '0000' on the 11XXXX0 devices.

The device code on 11XXXX1 devices is hardwired to '0001'. This allows both 11XXXX0 and 11XXXX1 devices to be used on the same bus without address conflicts.

**FIGURE 4-5: DEVICE ADDRESS BYTE ALLOCATION**




**Note 1:** This bit is a '1' on the 11XXXX1.

## 4.5 Bus Conflict Protection

To help guard against high current conditions arising from bus conflicts, the 11AAXXX/11LCXXX features a current-limited output driver. The $I_{OL}$ and $I_{OH}$ specifications describe the maximum current that can be sunk or sourced, respectively, by the SCIO pin. The 11AAXXX/11LCXXX will vary the output driver impedance to ensure that the maximum current level is not exceeded.

## 4.6 Device Standby

The 11AAXXX/11LCXXX features a low-power Standby mode during which the device is waiting to begin a new command. A high-to-low transition on SCIO will exit low-power mode and prepare the device for receiving the start header.

Standby mode will be entered upon the following conditions:

- A NoMAK followed by a SAK (i.e., valid termination of a command)
- Reception of a standby pulse

**Note:** In the case of the WRITE, WRSR, SETAL or ERAL commands, the write cycle is initiated upon receipt of the NoMAK, assuming all other write requirements have been met.

## 4.7 Device Idle

The 11AAXXX/11LCXXX features an Idle mode during which all serial data is ignored until a standby pulse occurs. Idle mode will be entered upon the following conditions:

- Invalid device address
- Invalid command byte, including Read, CRRD, Write, WRSR, SETAL and ERAL during a write cycle.
- Missed edge transition
- Reception of a MAK following a WREN, WRDI, SETAL or ERAL command byte
- Reception of a MAK following the data byte of a WRSR command

An invalid start header will indirectly cause the device to enter Idle mode. Whether or not the start header is invalid cannot be detected by the client, but will prevent the client from synchronizing properly with the host. If the client is not synchronized with the host, an edge transition will be missed, thus causing the device to enter Idle mode.

## 4.8 Synchronization

At the beginning of every command, the 11AAXXX/11LCXXX utilizes the start header to determine the host's bus clock period. This period is then used as a reference for all subsequent communication within that command.

The 11AAXXX/11LCXXX features re-synchronization circuitry, which will monitor the position of the middle data edge during each MAK bit and will subsequently adjust the internal time reference to remain synchronized with the host.

There are two variables which can cause the 11AAXXX/11LCXXX to lose synchronization. The first is frequency drift, defined as a change in the bit period, $T_E$. The second is edge jitter, which is a single occurrence change in the position of an edge within a bit period, while the bit period itself remains constant.

### 4.8.1 FREQUENCY DRIFT

Within a system, there is a possibility that frequencies can drift due to changes in voltage, temperature, etc. The re-synchronization circuitry provides some tolerance for such frequency drift. The tolerance range is specified by two parameters, $F_{DRIFT}$ and $F_{DEV}$. $F_{DRIFT}$ specifies the maximum tolerable change in bus frequency per byte. $F_{DEV}$ specifies the overall limit in frequency deviation within an operation (i.e., from the end of the start header until communication is terminated for that operation). The start header at the beginning of the next operation will reset the re-synchronization circuitry and allow for another $F_{DEV}$ amount of frequency drift.

### 4.8.2 EDGE JITTER

Ensuring that edge transitions from the host always occur exactly in the middle or end of the bit period is not always possible. Therefore, the re-synchronization circuitry is designed to provide some tolerance for edge jitter.

The 11XX adjusts its phase every MAK bit, so $T_{IJIT}$ specifies the maximum allowable peak-to-peak jitter relative to the previous MAK bit. Since the position of the previous MAK bit would be difficult to measure by the host, the minimum and maximum jitter values for a system should be considered the worst-case. These values will be based on the execution time for different branch paths in software, jitter due to thermal noise, etc.

The difference between the minimum and maximum values, as a percentage of the bit period, should be calculated and then compared against $T_{IJIT}$ to determine jitter compliance.

**Note:** Because the 11AAXXX/11LCXXX only re-synchronizes during the MAK bit, the overall ability to remain synchronized depends on a combination of frequency drift and edge jitter (i.e., if the MAK bit edge is experiencing the maximum allowable edge jitter, then there is no room for frequency drift). Conversely, if the frequency has drifted to the maximum amount tolerable within a byte, then no edge jitter can be present.

## 5.0 DEVICE COMMANDS

After the device address byte, a command byte must be sent by the host to indicate the type of operation to be performed. The code for each instruction is listed in Table 5-1.

**TABLE 5-1: INSTRUCTION SET**

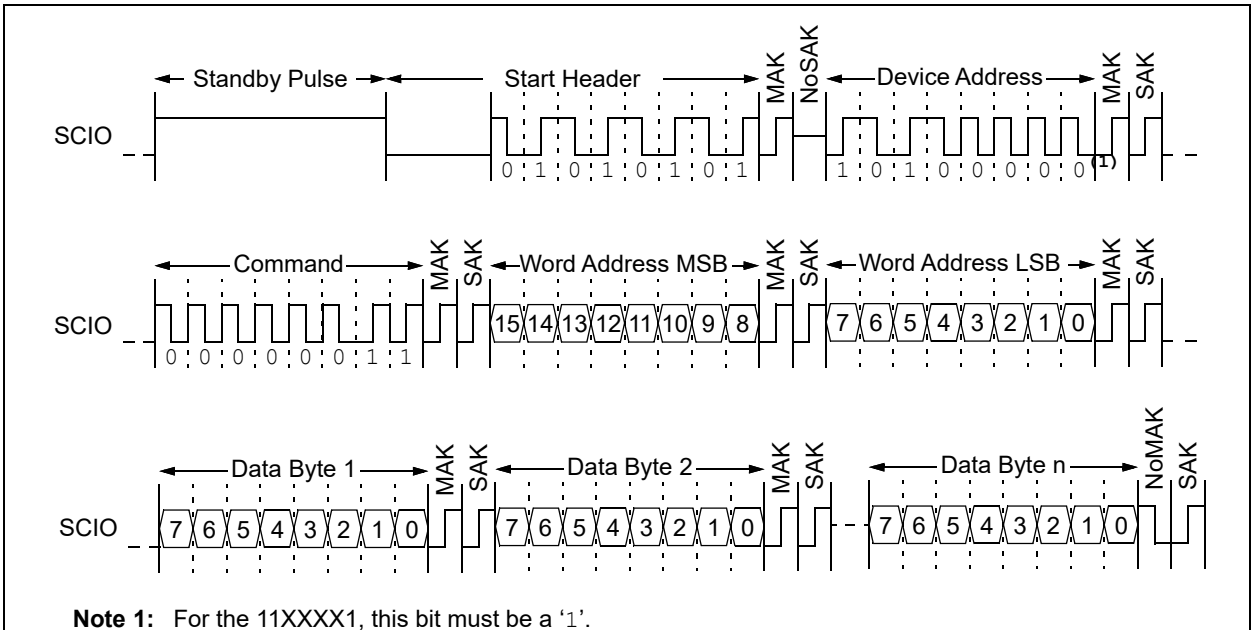
| Instruction Name | Instruction Code | Hex Code | Description |
|---|---|---|---|
| READ | 0000 0011 | 0x03 | Read data from memory array beginning at specified address |
| CRRD | 0000 0110 | 0x06 | Read data from current location in memory array |
| WRITE | 0110 1100 | 0x6C | Write data to memory array beginning at specified address |
| WREN | 1001 0110 | 0x96 | Set the write enable latch (enable write operations) |
| WRDI | 1001 0001 | 0x91 | Reset the write enable latch (disable write operations) |
| RDSR | 0000 0101 | 0x05 | Read STATUS register |
| WRSR | 0110 1110 | 0x6E | Write STATUS register |
| ERAL | 0110 1101 | 0x6D | Write '0x00' to entire array |
| SETAL | 0110 0111 | 0x67 | Write '0xFF' to entire array |

### 5.1 Read Instruction

The Read command allows the host to access any memory location in a random manner. After the READ instruction has been sent to the client, the two bytes of the Word Address are transmitted, with an Acknowledge sequence being performed after each byte. Then, the client sends the first data byte to the host. If more data is to be read, the host sends a MAK, indicating that the client should output the next data byte. This continues until the host sends a NoMAK, which ends the operation.

To provide sequential reads in this manner, the 11AAXXX/11LCXXX contains an internal Address Pointer which is incremented by one after the transmission of each byte. This Address Pointer allows the memory contents to be serially read during one operation. When the highest address is reached, the Address Pointer rolls over to address '0x000' if the host chooses to continue the operation by providing a MAK.

**FIGURE 5-1: READ COMMAND SEQUENCE**




**Note 1:** For the 11XXXX1, this bit must be a '1'.

## 5.2 Current Address Read (CRRD) Instruction

The internal address counter featured on the 11AAXXX/11LCXXX maintains the address of the last memory array location accessed. The CRRD instruction allows the host to read data back beginning from this current location. Consequently, no word address is provided upon issuing this command.

Note that, except for the initial word address, the READ and CRRD instructions are identical, including the ability to continue requesting data through the use of MAKs in order to sequentially read from the array.

As with the READ instruction, the CRRD instruction is terminated by transmitting a NoMAK.

Table 5-2 lists the events upon which the internal address counter is modified.

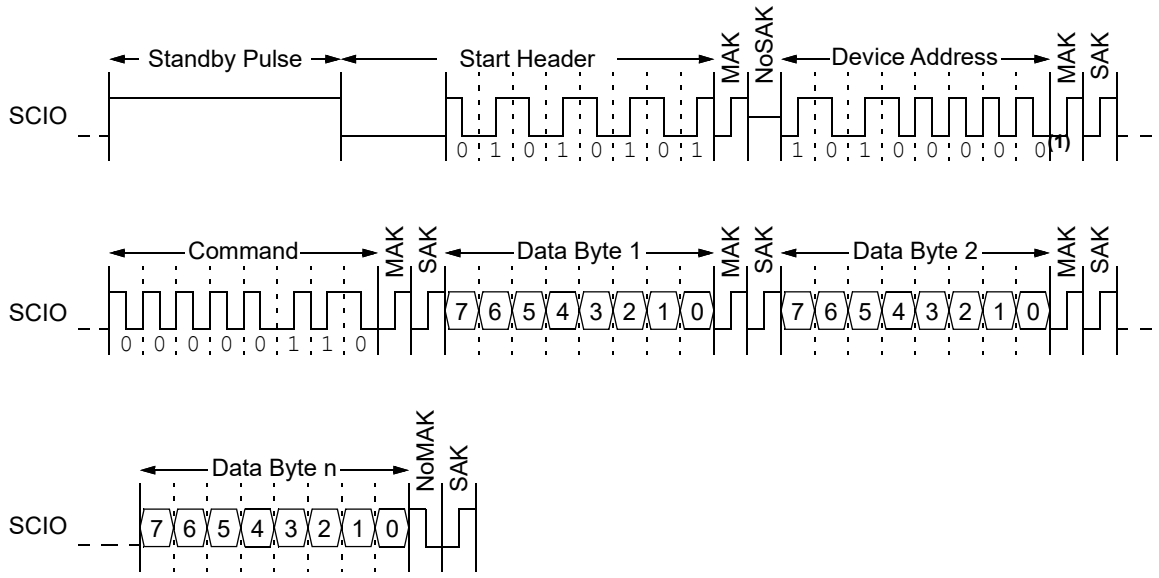
**TABLE 5-2: INTERNAL ADDRESS COUNTER**

| Command | Event | Action |
|---|---|---|
| — | Power-on Reset | Counter is undefined |
| READ or WRITE | MAK edge following each Address byte | Counter is updated with newly received value |
| READ, WRITE or CRRD | MAK/NoMAK edge following each data byte | Counter is incremented by 1 |

**Note 1:** If, following each data byte in a READ, WRITE or CRRD instruction, neither a MAK nor a NoMAK edge is received (i.e., if a standby pulse occurs instead), the internal address counter will not be incremented.

**2:** During a Write command, once the last data byte for a page has been loaded, the internal Address Pointer will rollover to the beginning of the selected page.

**FIGURE 5-2: CRRD COMMAND SEQUENCE**




**Note 1:** For the 11XXXX1, this bit must be a '1'.

## 5.3 Write Instruction

Prior to any attempt to write data to the 11AAXXX/11LCXXX, the write enable latch must be set by issuing the WREN instruction (see **Section 5.4 "Write Enable (WREN) and Write Disable (WRDI) Instructions"**).

Once the write enable latch is set, the user may proceed with issuing a WRITE instruction (including the header and device address bytes) followed by the MSB and LSB of the Word Address. Once the last Acknowledge sequence has been performed, the host transmits the data byte to be written.

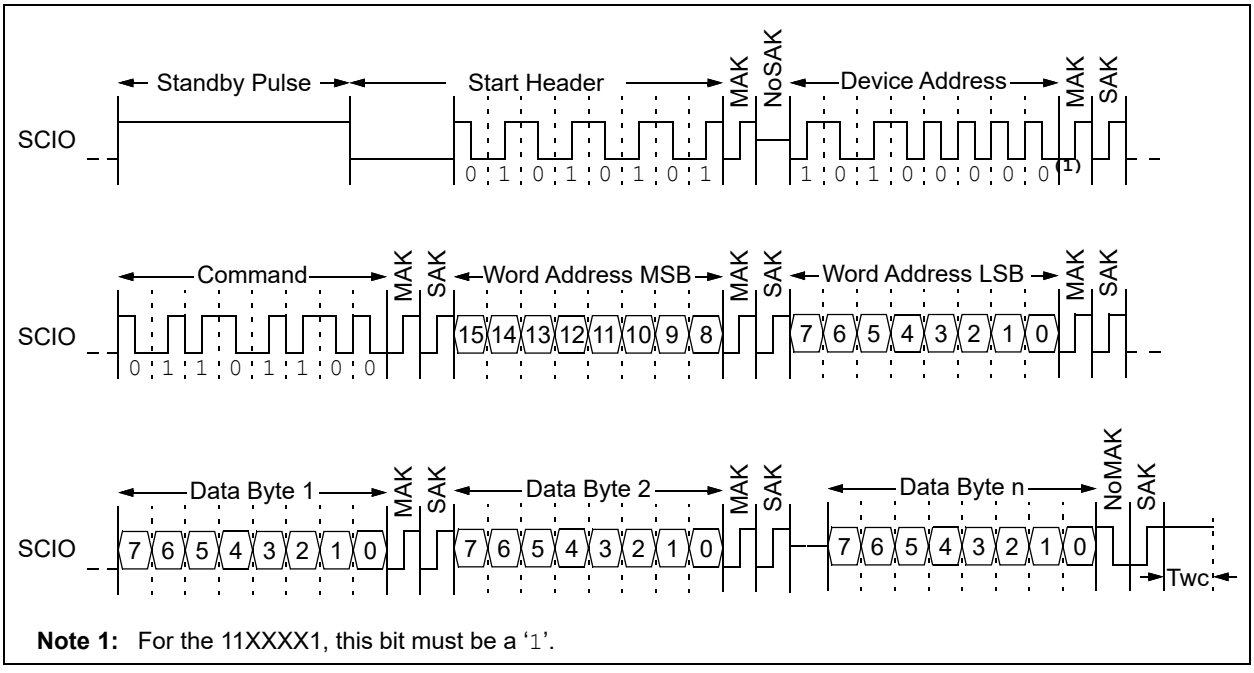
The 11AAXXX/11LCXXX features a 16-byte page buffer, meaning that up to 16 bytes can be written at one time. To utilize this feature, the host can transmit up to 16 data bytes to the 11AAXXX/11LCXXX, which are temporarily stored in the page buffer. After each data byte, the host sends a MAK, indicating whether or not another data byte is to follow. A NoMAK indicates that no more data is to follow, and as such will initiate the internal write cycle.

**Note:** If a NoMAK is generated before any data has been provided, or if a standby pulse occurs before the NoMAK is generated, the 11AAXXX/11LCXXX will be reset, and the write cycle will not be initiated.

Upon receipt of each word, the four lower-order Address Pointer bits are internally incremented by one. The higher-order bits of the word address remain constant. If the host should transmit data past the end of the page, the address counter will roll over to the beginning of the page, where further received data will be written.

**Note:** Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page size (16 bytes) and end at addresses that are integer multiples of the page size minus 1. As an example, the page that begins at address 0x30 ends at address 0x3F. If a page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is, therefore, necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

**FIGURE 5-3: WRITE COMMAND SEQUENCE**




**Note 1:** For the 11XXXX1, this bit must be a '1'.

## 5.4 Write Enable (WREN) and Write Disable (WRDI) Instructions

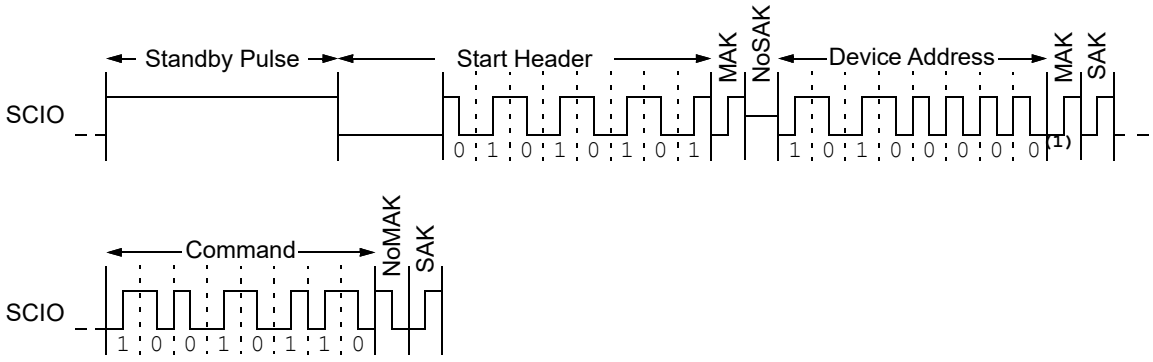
The 11XX contains a write enable latch. See Table 7-1 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI instruction will reset the latch.

**Note:** The WREN and WRDI instructions must be terminated with a NoMAK following the command byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

The following is a list of conditions under which the write enable latch will be reset:

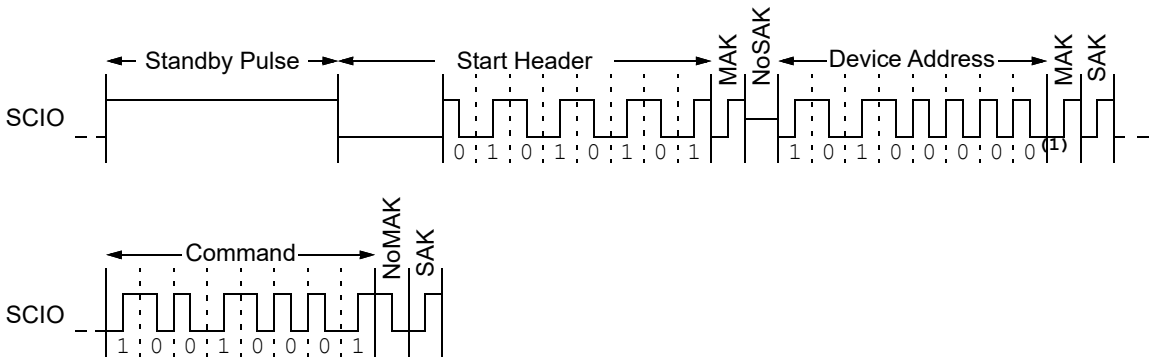
- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- ERAL instruction successfully executed
- SETAL instruction successfully executed

**FIGURE 5-4: WRITE ENABLE COMMAND SEQUENCE**




**Note 1:** For the 11XXXX1, this bit must be a '1'.

**FIGURE 5-5: WRITE DISABLE COMMAND SEQUENCE**




**Note 1:** For the 11XXXX1, this bit must be a '1'.

## 5.5 Read Status Register (RDSR) Instruction

The RDSR instruction provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | BP1 | BP0 | WEL | WIP |

**Note:** Bits 4-7 are don't cares, and will read as '0'.

The **Write-In-Process (WIP)** bit indicates whether the 11AAXXX/11LCXXX is busy with a write operation. When set to a '1', a write is in progress. When set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1', the latch allows writes to the array. When set to a '0', the latch prohibits writes to the array. This bit is set and cleared using the WREN and WRDI instructions, respectively. This bit is read-only for any other instruction.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user through the WRSR instruction. These bits are nonvolatile.

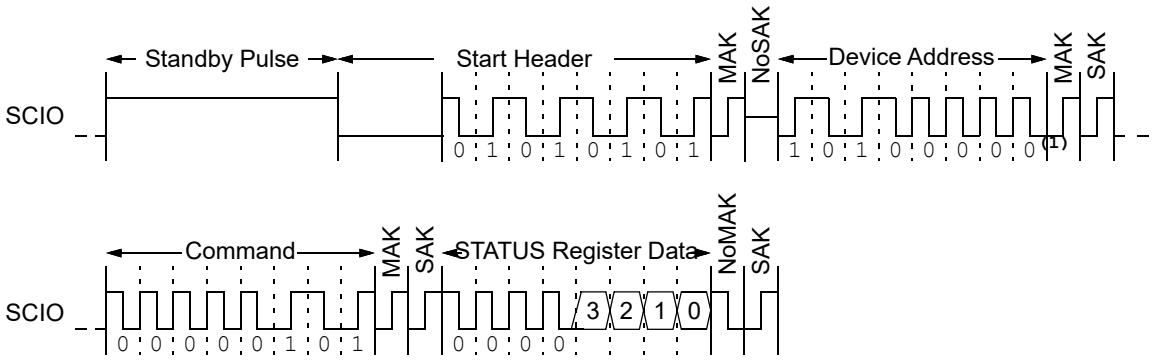
**Note:** If Read Status Register command is initiated while the 11XX is currently executing an internal write cycle on the STATUS register, the new Block Protection bit values will be read during the entire command.

The WIP and WEL bits will update dynamically (asynchronous to issuing the RDSR instruction). Furthermore, after the STATUS register data is received, the host can provide a MAK during the Acknowledge sequence to request that the data be transmitted again. This allows the host to continuously monitor the WIP and WEL bits without the need to issue another full command.

Once the host is finished, it provides a NoMAK to end the operation.

**Note:** The current drawn for a Read Status Register command during a write cycle is a combination of the ICC Read and ICC Write operating currents.

**FIGURE 5-6: READ STATUS REGISTER COMMAND SEQUENCE**




**Note 1:** For the 11XXXX1, this bit must be a '1'.

**Note 2:** The STATUS register data can continuously be read, or polled, by transmitting a MAK in place of the NoMAK.

## 5.6 Write Status Register (WRSR) Instruction

The WRSR instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 5-3.

After transmitting the STATUS register data, the host must transmit a NoMAK during the Acknowledge sequence in order to initiate the internal write cycle.

**Note:** The WRSR instruction must be terminated with a NoMAK following the data byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

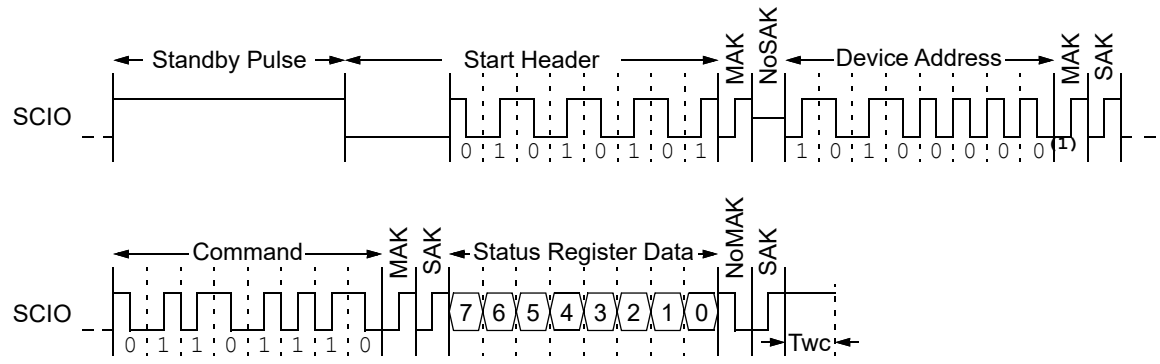
**TABLE 5-3: ARRAY PROTECTION**

| BP1 | BP0 | Address Ranges Write-Protected | Address Ranges Unprotected |
|---|---|---|---|
| 0 | 0 | None | All |
| 0 | 1 | Upper 1/4 | Lower 3/4 |
| 1 | 0 | Upper 1/2 | Lower 1/2 |
| 1 | 1 | All | None |

**TABLE 5-4: PROTECTED ARRAY ADDRESS LOCATIONS**

| Density | Upper 1/4 | Upper 1/2 | All Sectors |
|---|---|---|---|
| 1K | 60h-7Fh | 40h-7Fh | 00h-7Fh |
| 2K | C0h-FFh | 80h-FFh | 00h-FFh |
| 4K | 180h-1FFh | 100h-1FFh | 000h-1FFh |
| 8K | 300h-3FFh | 200h-3FFh | 000h-3FFh |
| 16K | 600h-7FFh | 400h-7FFh | 000h-7FFh |

**FIGURE 5-7: WRITE STATUS REGISTER COMMAND SEQUENCE**




**Note 1:** For the 11XXXX1, this bit must be a '1'.

## 5.7 Erase All (ERAL) Instruction

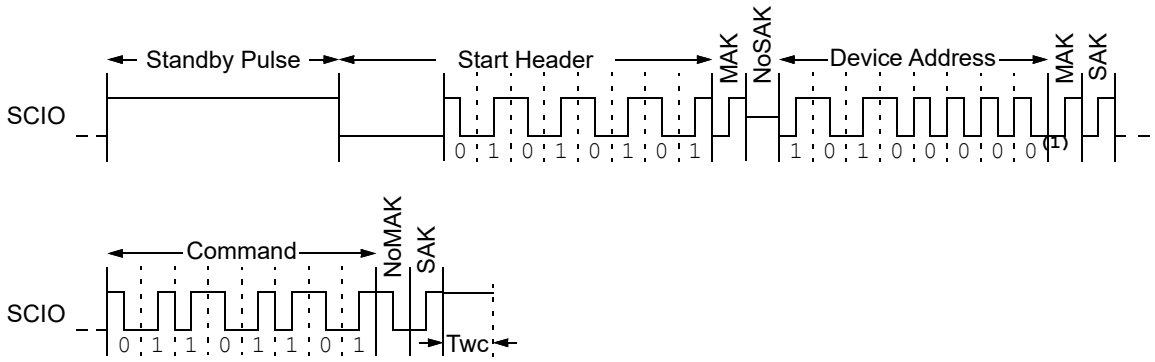
The ERAL instruction allows the user to write '0x00' to the entire memory array with one command. Note that the write enable latch (WEL) must first be set by issuing the WREN instruction.

Once the write enable latch is set, the user may proceed with issuing a ERAL instruction (including the header and device address bytes). Immediately after the NoMAK bit has been transmitted by the host, the internal write cycle is initiated, during which time all words of the memory array are written to '0x00'.

The ERAL instruction is ignored if either of the Block Protect bits (BP0, BP1) are not 0, meaning 1/4, 1/2, or all of the array is protected.

**Note:** The ERAL instruction must be terminated with a NoMAK following the command byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

**FIGURE 5-8: ERASE ALL COMMAND SEQUENCE**




**Note 1:** For the 11XXXX1, this bit must be a '1'.

## 5.8 Set All (SETAL) Instruction

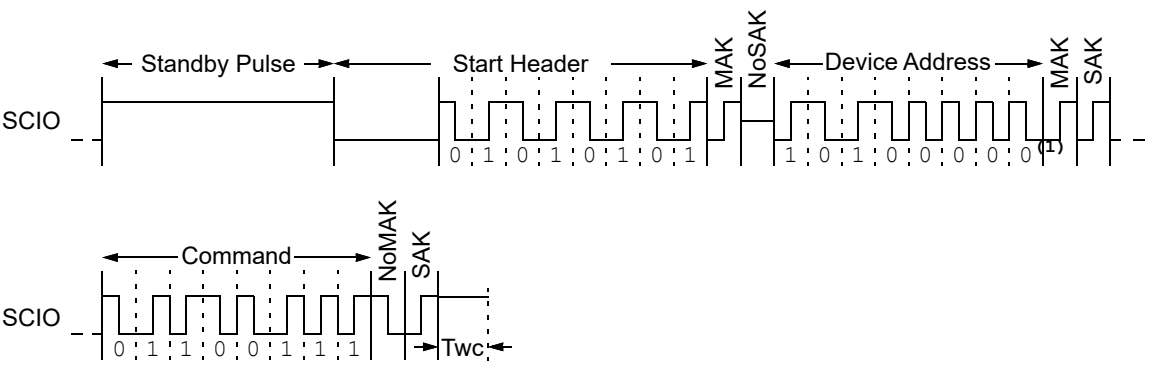
The SETAL instruction allows the user to write '0xFF' to the entire memory array with one command. Note that the write enable latch (WEL) must first be set by issuing the WREN instruction.

Once the write enable latch is set, the user may proceed with issuing a SETAL instruction (including the header and device address bytes). Immediately after the NoMAK bit has been transmitted by the host, the internal write cycle is initiated, during which time all words of the memory array are written to '0xFF'.

The SETAL instruction is ignored if either of the Block Protect bits (BP0, BP1) are not 0, meaning 1/4, 1/2, or all of the array is protected.

**Note:** The SETAL instruction must be terminated with a NoMAK following the command byte. If a NoMAK is not received at this point, the command will be considered invalid, and the device will go into Idle mode without responding with a SAK or executing the command.

**FIGURE 5-9: SET ALL COMMAND SEQUENCE**




**Note 1:** For the 11XXXX1, this bit must be a '1'.

## 6.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The Write Enable Latch (WEL) is reset on power-up
- A Write Enable (WREN) instruction must be issued to set the write enable latch
- After a write, ERAL, SETAL or WRSR command, the write enable latch is reset
- Commands to access the array or write to the STATUS register are ignored during an internal write cycle and programming is not affected

## 7.0 POWER-ON STATE

The 11AAXXX/11LCXXX powers on in the following state:

- The device is in low-power Shutdown mode, requiring a low-to-high transition on SCIO to enter Idle mode
- The Write Enable Latch (WEL) is reset
- The internal Address Pointer is undefined
- A low-to-high transition, standby pulse and subsequent high-to-low transition on SCIO (the first low pulse of the header) are required to enter the active state

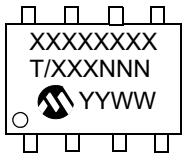
**TABLE 7-1: WRITE PROTECT FUNCTIONALITY MATRIX**

| WEL | Protected Blocks | Unprotected Blocks | Status Register |
|---|---|---|---|
| 0 | Protected | Protected | Protected |
| 1 | Protected | Writable | Writable |

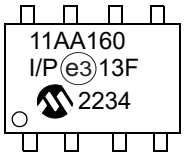
## 8.0 PACKAGING INFORMATION

### 8.1 Package Marking Information

8-Lead PDIP




Example:




| 8-Lead PDIP Package Marking (Pb-Free) | | | |
|---|---|---|---|
| **Device** | **Line 1 Marking** | **Device** | **Line 1 Marking** |
| 11AA010 | 11AA010 | 11LC010 | 11LC010 |
| 11AA020 | 11AA020 | 11LC020 | 11LC020 |
| 11AA040 | 11AA040 | 11LC040 | 11LC040 |
| 11AA080 | 11AA080 | 11LC080 | 11LC080 |
| 11AA160 | 11AA160 | 11LC160 | 11LC160 |
| 11AA161 | 11AA161 | 11LC161 | 11LC161 |
| **Note:** T = Temperature Grade (I, E) | | | |

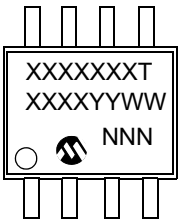
| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | RoHS-compliant JEDEC® designator for Matte Tin (Sn) |

**Note:** Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

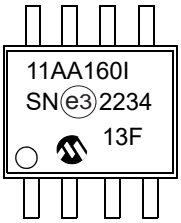
**Note:** For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead SOIC




Example:




| 8-Lead SOIC Package Marking (Pb-Free) | | | |
|---|---|---|---|
| **Device** | **Line 1 Marking** | **Device** | **Line 1 Marking** |
| 11AA010 | 11AA010T | 11LC010 | 11LC010T |
| 11AA020 | 11AA020T | 11LC020 | 11LC020T |
| 11AA040 | 11AA040T | 11LC040 | 11LC040T |
| 11AA080 | 11AA080T | 11LC080 | 11LC080T |
| 11AA160 | 11AA160T | 11LC160 | 11LC160T |
| 11AA161 | 11AA161T | 11LC161 | 11LC161T |
| **Note:** T = Temperature Grade (I, E) | | | |

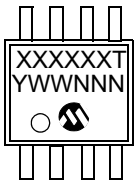
| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | RoHS-compliant JEDEC® designator for Matte Tin (Sn) |

**Note:** Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

**Note:** For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead MSOP (150 mil)




Example:


| 8-Lead MSOP Package Marking (Pb-Free) | | | |
|---|---|---|---|
| **Device** | **Line 1 Marking** | **Device** | **Line 1 Marking** |
| 11AA010 | 11A01T | 11LC010 | 11L01T |
| 11AA020 | 11A02T | 11LC020 | 11L02T |
| 11AA040 | 11A04T | 11LC040 | 11L04T |
| 11AA080 | 11A08T | 11LC080 | 11L08T |
| 11AA160 | 11AAT | 11LC160 | 11LAT |
| 11AA161 | 11AA1T | 11LC161 | 11LA1T |
| **Note:** T = Temperature Grade (I, E) | | | |

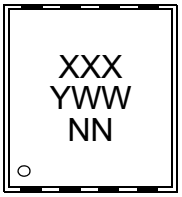
| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | RoHS-compliant JEDEC® designator for Matte Tin (Sn) |

**Note:** Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

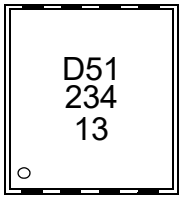
**Note:** For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead 2x3 TDFN




Example:




| 8-Lead 2x3 TDFN Package Marking (Pb-Free) | | | | |
|---|---|---|---|---|
| **Device** | **I-Temp Marking** | **Device** | **I-Temp Marking** | **E-Temp Marking** |
| 11AA010 | D11 | 11LC010 | D14 | D15 |
| 11AA020 | D21 | 11LC020 | D24 | D25 |
| 11AA040 | D31 | 11LC040 | D34 | D35 |
| 11AA080 | D41 | 11LC080 | D44 | D45 |
| 11AA160 | D51 | 11LC160 | D54 | D55 |
| 11AA161 | D5D | 11LC161 | D5G | D5H |

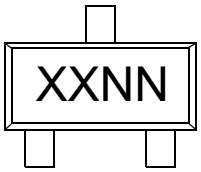
| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | RoHS-compliant JEDEC® designator for Matte Tin (Sn) |

**Note:** Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

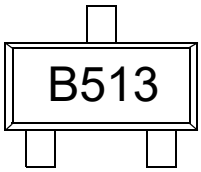
**Note:** For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3-Lead SOT-23




Example:




| 3-Lead SOT-23 Package Marking (Pb-Free) | | | | |
|---|---|---|---|---|
| **Device** | **I-Temp Marking** | **Device** | **I-Temp Marking** | **E-Temp Marking** |
| 11AA010 | B1NN | 11LC010 | M1NN | N1NN |
| 11AA020 | B2NN | 11LC020 | M2NN | N2NN |
| 11AA040 | B3NN | 11LC040 | M3NN | N3NN |
| 11AA080 | B4NN | 11LC080 | M4NN | N4NN |
| 11AA160 | B5NN | 11LC160 | M5NN | N5NN |
| 11AA161 | B0NN | 11LC161 | M0NN | N0NN |

**Legend:**

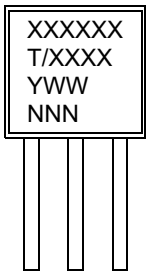
| | |
|---|---|
| XX...X | Part number or part number code |
| T | Temperature (I, E) |
| Y | Year code (last digit of calendar year) |
| YY | Year code (last 2 digits of calendar year) |
| WW | Week code (week of January 1 is week ‘01’) |
| NNN | Alphanumeric traceability code (2 characters for small packages) |
| (e3) | RoHS-compliant JEDEC® designator for Matte Tin (Sn) |

**Note:** Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

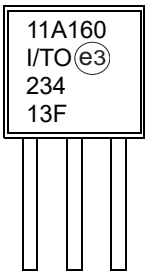
**Note:** For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3-Lead TO-92




Example:




| 3-Lead TO-92 Package Marking (Pb-Free) | | | |
|---|---|---|---|
| **Device** | **Line 1 Marking** | **Device** | **Line 1 Marking** |
| 11AA010 | 11A010 | 11LC010 | 11L010 |
| 11AA020 | 11A020 | 11LC020 | 11L020 |
| 11AA040 | 11A040 | 11LC040 | 11L040 |
| 11AA080 | 11A080 | 11LC080 | 11L080 |
| 11AA160 | 11A160 | 11LC160 | 11L160 |
| 11AA161 | 11A161 | 11LC161 | 11L161 |
| **Note:** T = Temperature Grade (I, E) | | | |

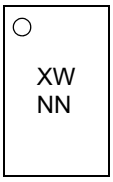
| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | RoHS-compliant JEDEC® designator for Matte Tin (Sn) |

**Note:** Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

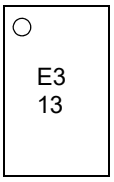
**Note:** For very small packages with no room for the JEDEC® designator (e3) , the marking will only appear on the outer carton or reel label.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

4-Lead Chip Scale




Example:




| 4-Lead Chip Scale Package Marking (Pb-Free) | |
|---|---|
| **Device** | **Line 1 Marking** |
| 11AA010 | AW |
| 11AA020 | BW |
| 11AA040 | CW |
| 11AA080 | DW |
| 11AA160 | EW |
| 11AA161 | HW |

| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | RoHS-compliant JEDEC® designator for Matte Tin (Sn) |

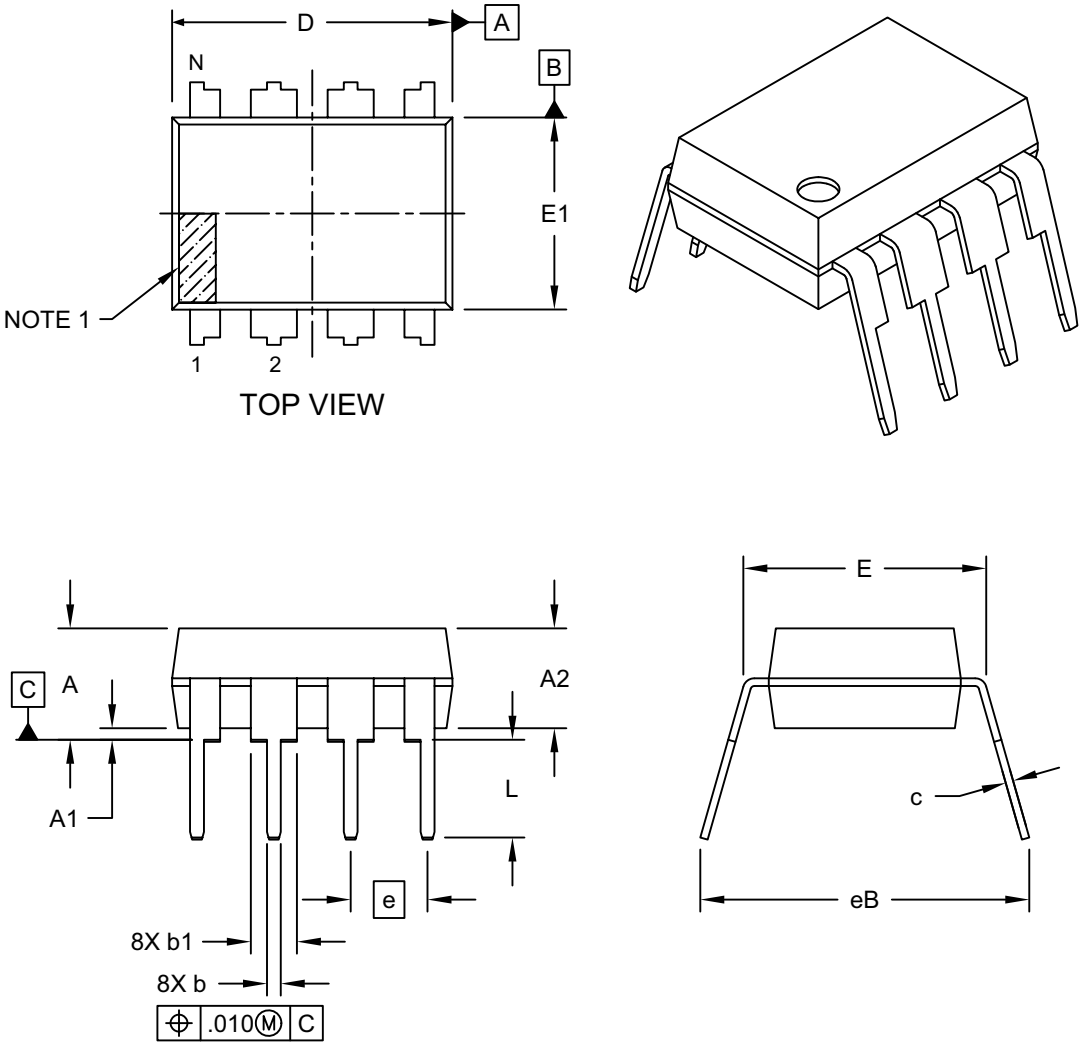
**Note:** Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

**Note:** For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

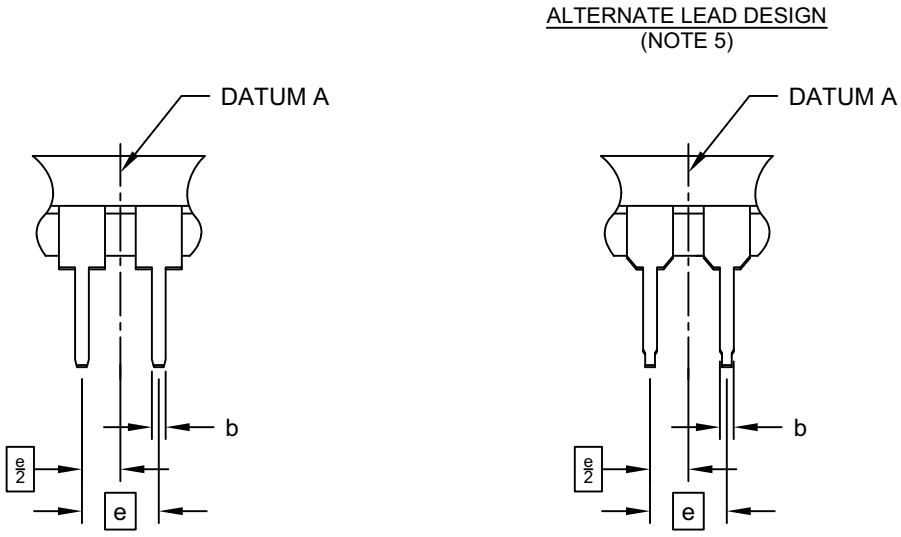
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-018-P Rev F Sheet 1 of 2

## 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | - | - | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | - | - |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | - | - | .430 |

Notes:

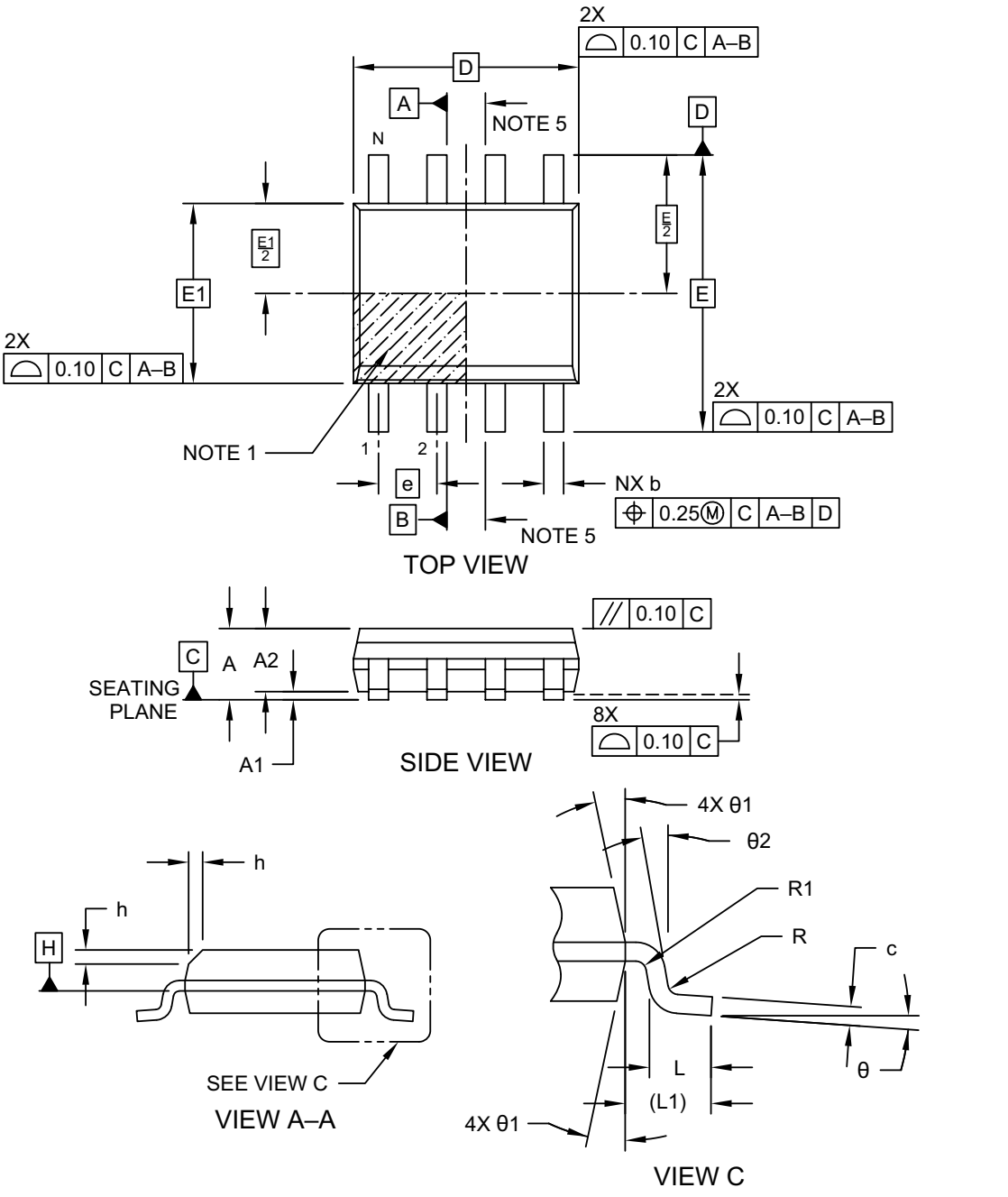
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev F Sheet 2 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

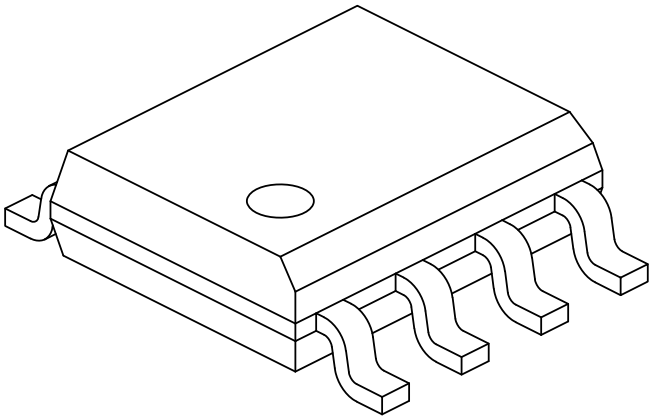
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | - |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Lead Bend Radius | R | 0.07 | – | – |
| Lead Bend Radius | R1 | 0.07 | – | – |
| Foot Angle | θ | 0° | – | 8° |
| Mold Draft Angle | θ1 | 5° | – | 15° |
| Lead Angle | θ2 | 0° | – | – |

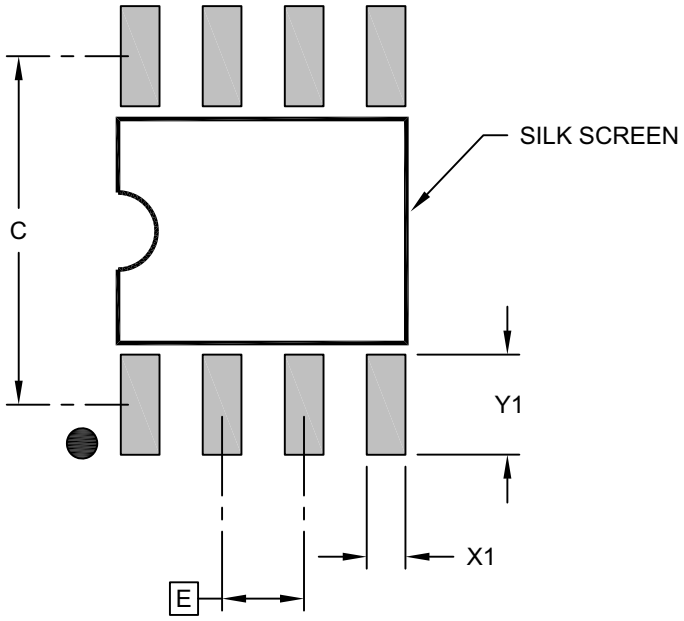
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

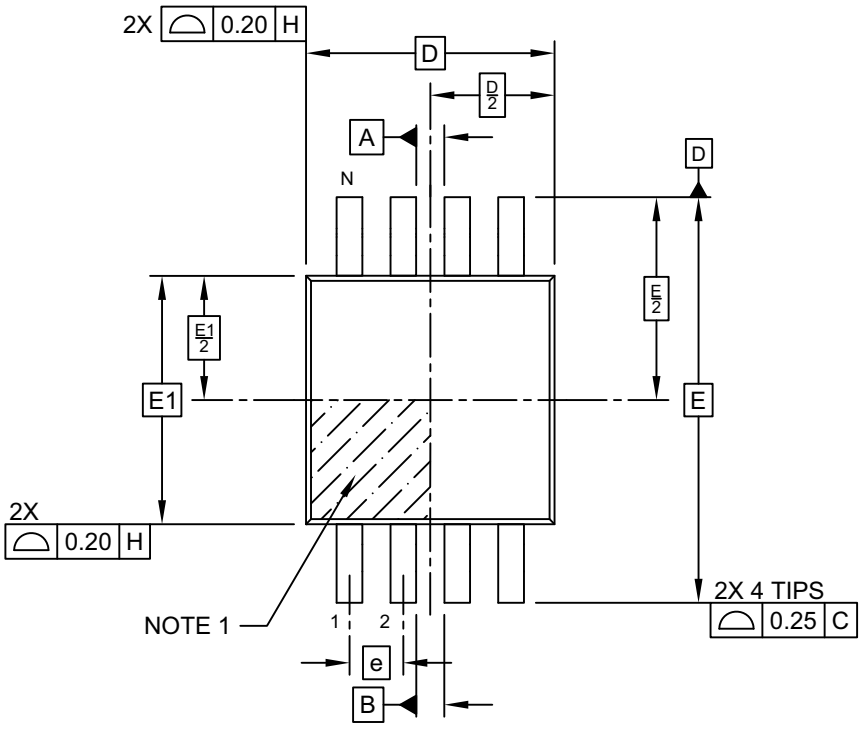
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

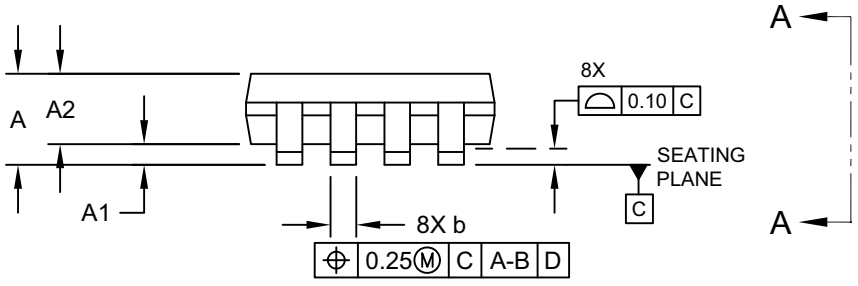
Microchip Technology Drawing C04-2057-SN Rev K

### 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

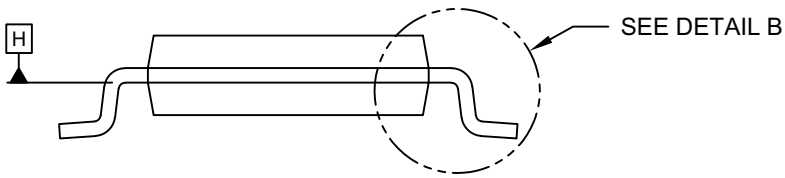
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

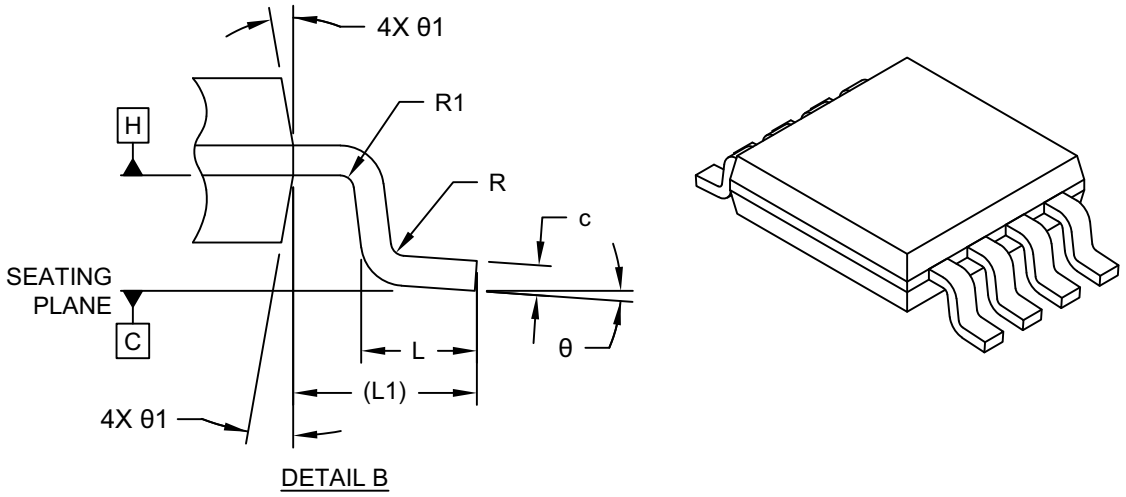



VIEW A–A

Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

## 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.10 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Overall Length | D | | 3.00 BSC | |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Terminal Width | b | 0.22 | – | 0.40 |
| Terminal Thickness | c | 0.08 | – | 0.23 |
| Terminal Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Lead Bend Radius | R | 0.07 | – | – |
| Lead Bend Radius | R1 | 0.07 | – | – |
| Foot Angle | θ | 0° | – | 8° |
| Mold Draft Angle | θ1 | 5° | – | 15° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

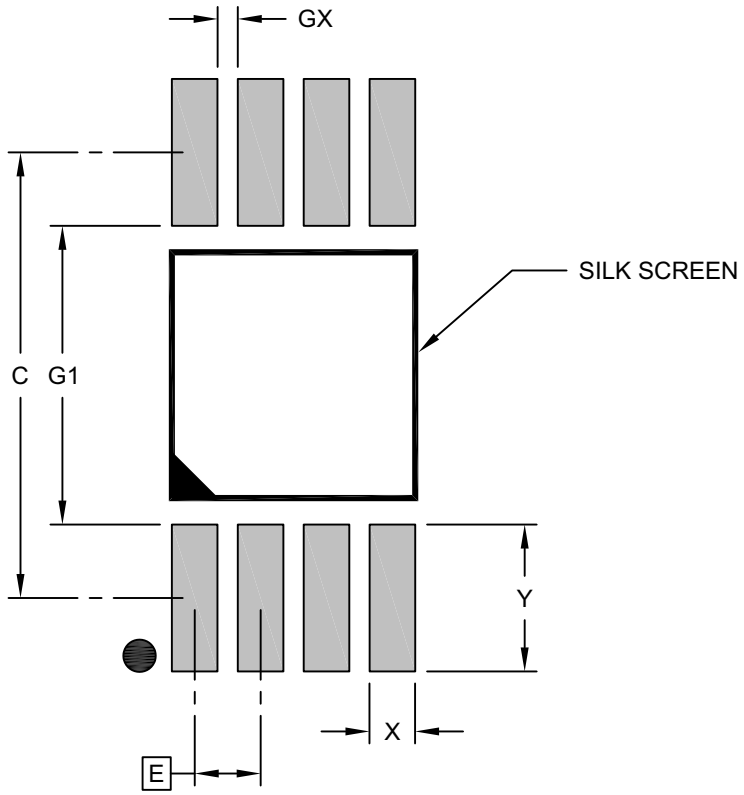
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

## 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 4.40 | |
| Contact Pad Width (X8) | X | | | 0.45 |
| Contact Pad Length (X8) | Y | | | 1.45 |
| Contact Pad to Contact Pad (X4) | G1 | 2.95 | | |
| Contact Pad to Contact Pad (X6) | GX | 0.20 | | |

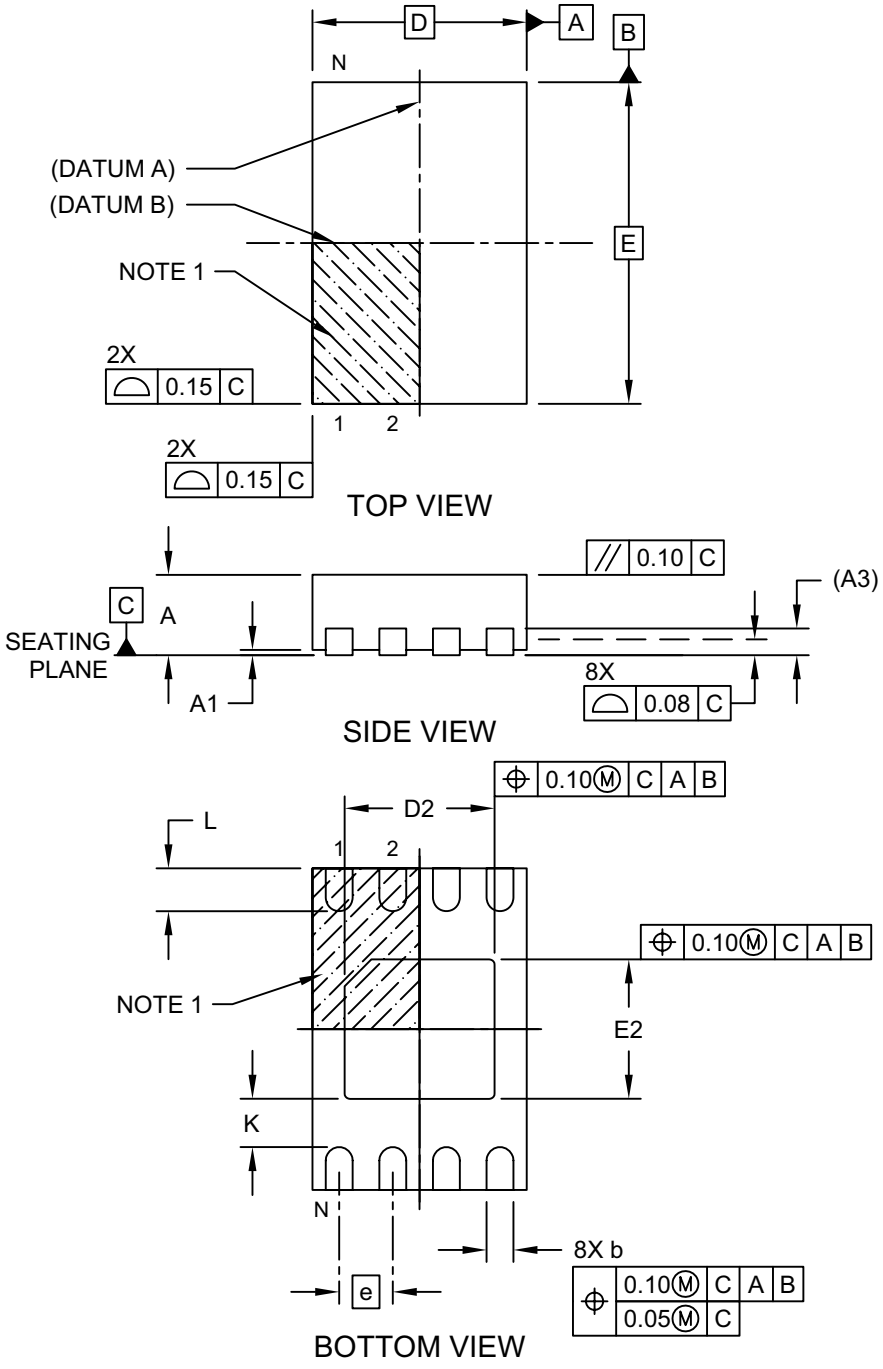
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-MS Rev F

**8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN]**
**With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)**

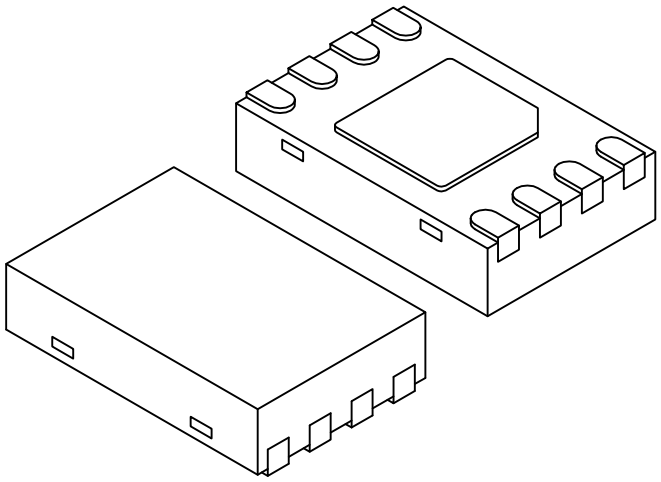
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

## 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.70 | 0.75 | 0.80 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.35 | 1.40 | 1.45 |
| Exposed Pad Width | E2 | 1.25 | 1.30 | 1.35 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.30 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

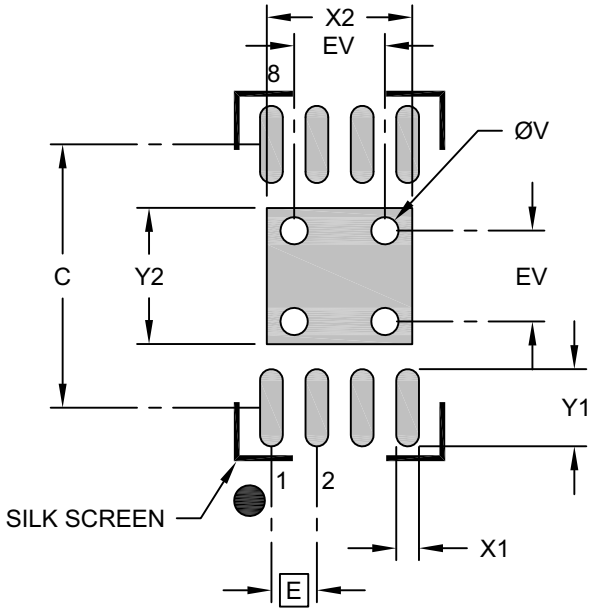
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

### 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.60 |
| Optional Center Pad Length | Y2 | | | 1.50 |
| Contact Pad Spacing | C | | 2.90 | |
| Contact Pad Width (X8) | X1 | | | 0.25 |
| Contact Pad Length (X8) | Y1 | | | 0.85 |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

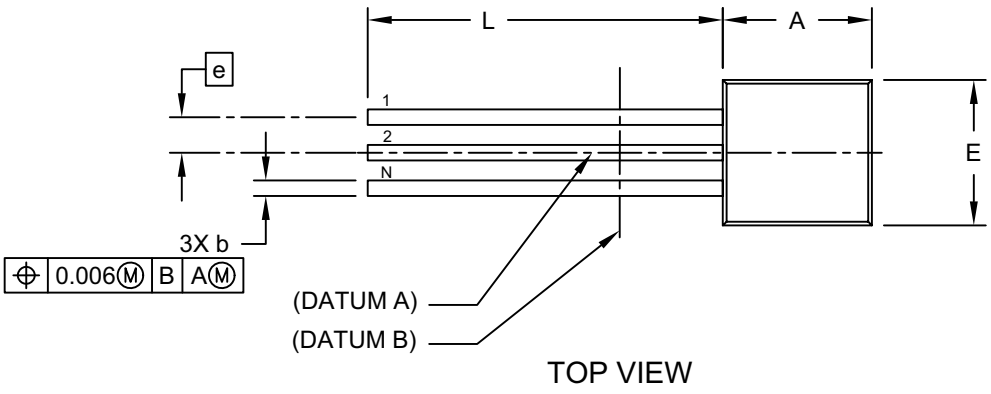
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MN Rev. B

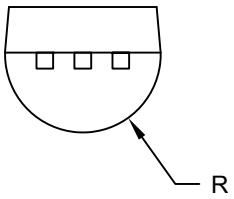
### 3-Lead Plastic Transistor Outline (TO) [TO-92]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW


SIDE VIEW

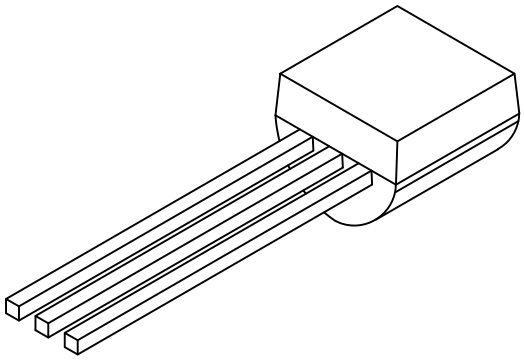



VIEW A-A

Microchip Technology Drawing C04-101-TO Rev D Sheet 1 of 2

### 3-Lead Plastic Transistor Outline (TO) [TO-92]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 3 | |
| Pitch | e | | .050 BSC | |
| Bottom to Package Flat | D | .125 | - | .165 |
| Overall Width | E | .175 | - | .205 |
| Overall Length | A | .170 | - | .210 |
| Molded Package Radius | R | .080 | - | .105 |
| Tip to Seating Plane | L | .500 | - | - |
| Lead Thickness | c | .014 | - | .021 |
| Lead Width | b | .014 | - | .022 |

Notes:

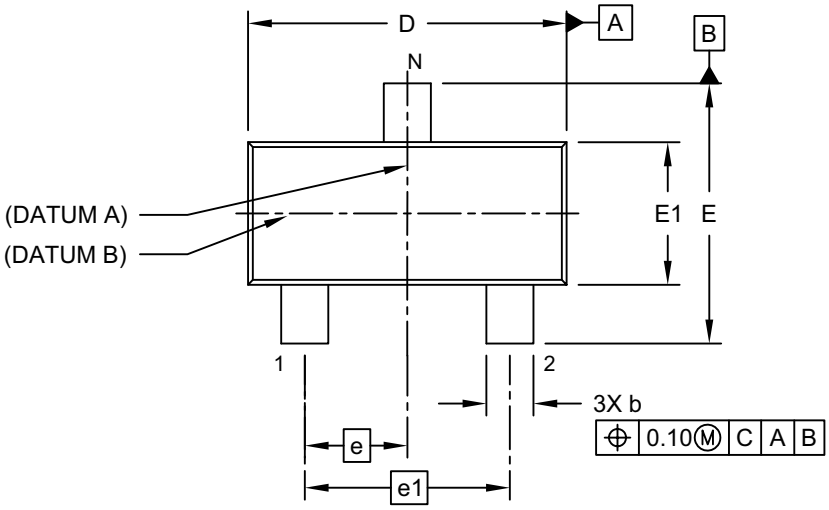
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

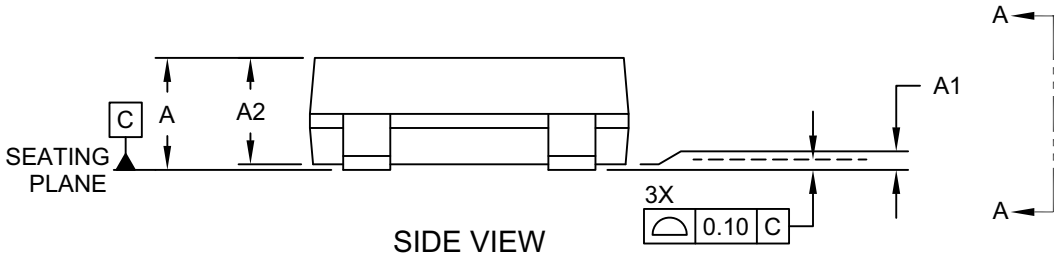
Microchip Technology Drawing C04-101-TO Rev D Sheet 2 of 2

### 3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

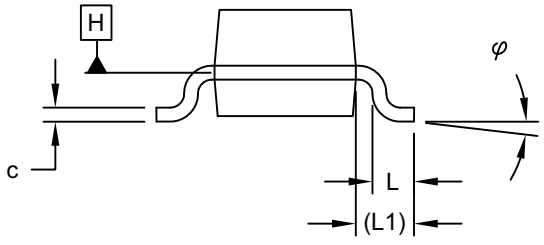
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

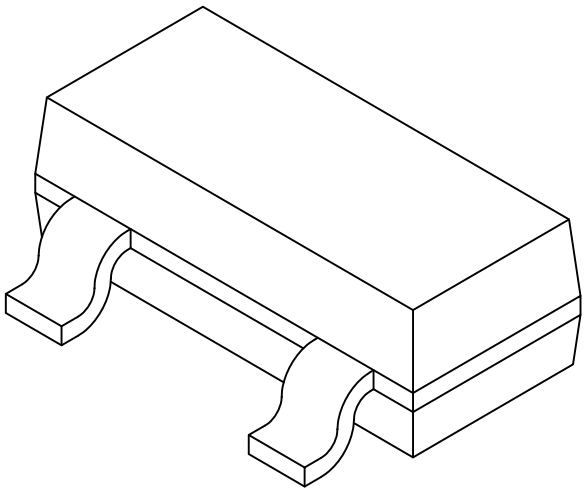



VIEW A-A

Microchip Technology Drawing C04-104 (TT) Rev C Sheet 1 of 2

### 3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 3 | |
| Lead Pitch | e | | 0.95 BSC | |
| Outside Lead Pitch | e1 | | 1.90 BSC | |
| Overall Height | A | 0.89 | - | 1.12 |
| Molded Package Thickness | A2 | 0.79 | 0.95 | 1.02 |
| Standoff | A1 | 0.01 | - | 0.10 |
| Overall Width | E | 2.10 | - | 2.64 |
| Molded Package Width | E1 | 1.16 | 1.30 | 1.40 |
| Overall Length | D | 2.67 | 2.90 | 3.05 |
| Foot Length | L | 0.13 | 0.50 | 0.60 |
| Footprint | (L1) | | 0.42 REF | |
| Foot Angle | φ | 0° | - | 10° |
| Lead Thickness | c | 0.08 | - | 0.20 |
| Lead Width | b | 0.30 | - | 0.54 |

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M

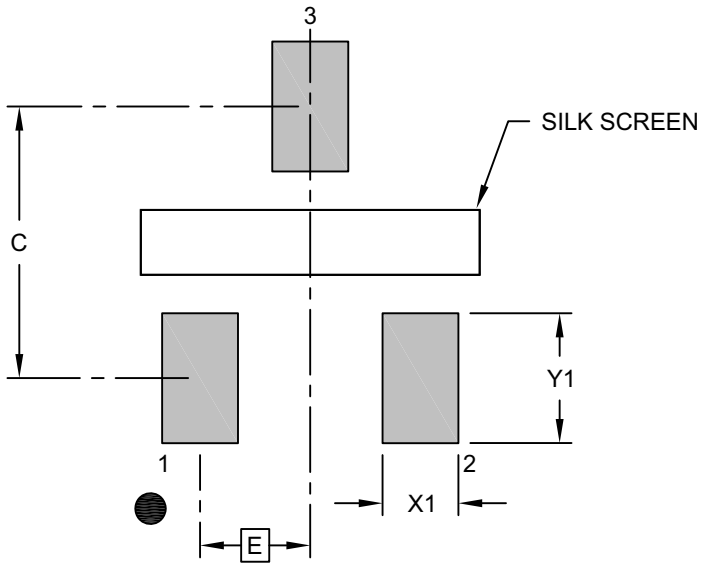
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-104 (TT) Rev C Sheet 2 of 2

### 3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.95 BSC | |
| Contact Pad Spacing | C | | 2.30 | |
| Contact Pad Width (X3) | X1 | | | 0.65 |
| Contact Pad Length (X3) | Y1 | | | 1.10 |

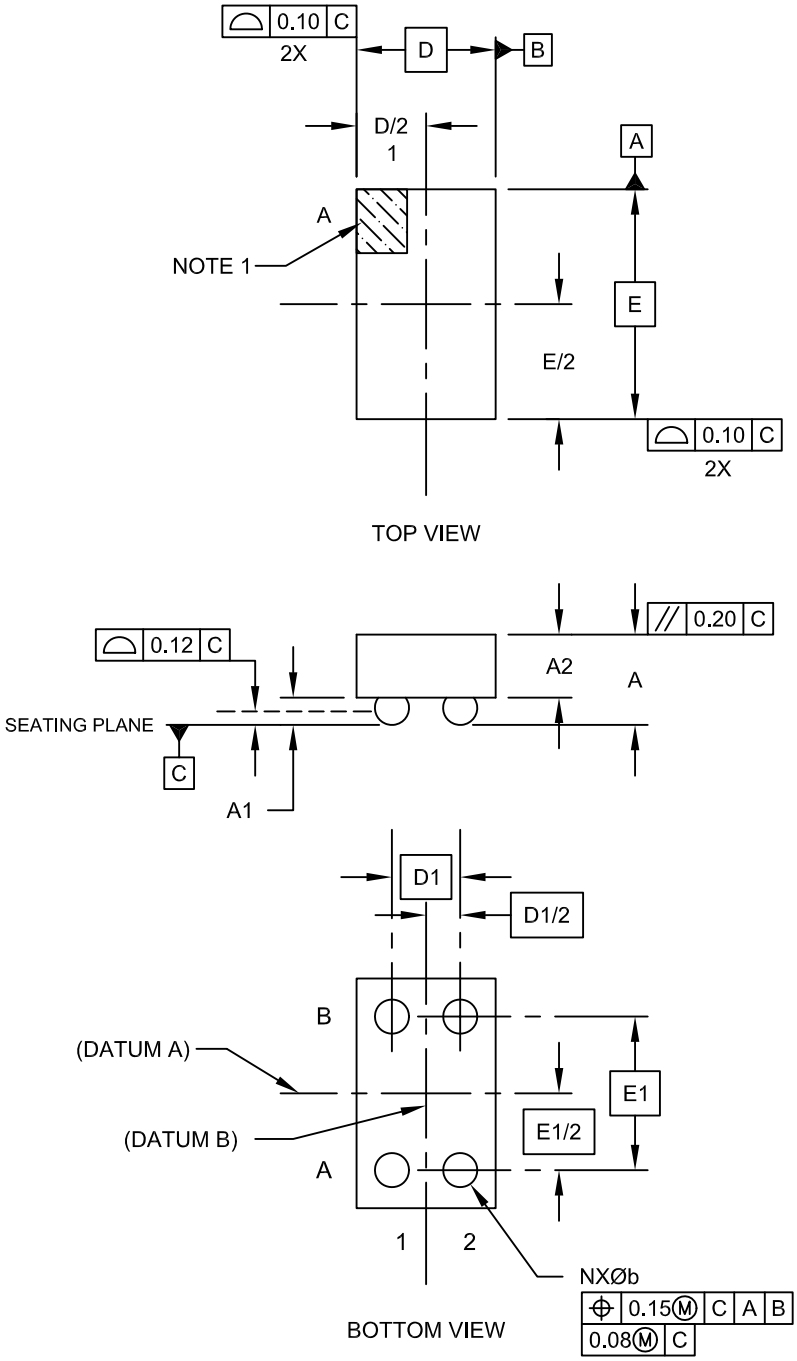
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2104 (TT) Rev B

4-Lead Chip Scale Package (CS) - [CSP]

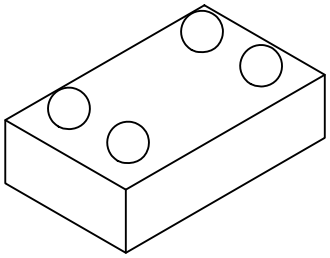
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-6008A Sheet 1 of 2

4-Lead Chip Scale Package (CS) - [CSP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Contacts | N | | 4 | |
| Adjacent Column X-Pitch | D1 | | 0.400 BSC | |
| Adjacent Row Y-Pitch | E1 | | 0.900 BSC | |
| Overall Height | A | 0.47 | 0.51 | 0.55 |
| Die Height | A2 | 0.33 | 0.35 | 0.37 |
| Bump Height | A1 | 0.14 | 0.16 | 0.18 |
| Overall Width | D | | NOTE 4 | |
| Overall Length | E | | NOTE 4 | |
| Ball Diameter | b | 0.18 | 0.20 | 0.22 |

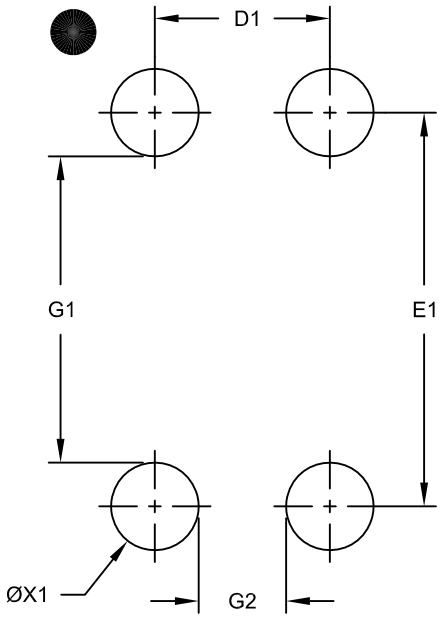
Notes:

1. Orientation reference feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
4. Package size varies with specific devices. Please see the specific Product Data Sheet.

Microchip Technology Drawing C04-6008A Sheet 2 of 2

### 4-Lead Chip Scale Package (CS) - [CSP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Contacts | N | | 4 | |
| Contact Pad Spacing | D1 | | 0.40 | |
| Contact Pad Spacing | E1 | | 0.90 | |
| Contact Pad Diameter (X4) | ØX1 | | 0.20 | |
| Distance Between Pads | G1 | | 0.70 | |
| Distance Between Pads | G2 | | 0.20 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-8008A

## APPENDIX A: REVISION HISTORY

### Revision K (03/23)

Updated formatting to current template; Replaced terminology “Master” and “Slave” with “Host” and “Client” respectively; Added Automotive PIS.

### Revision J (04/11)

Added new Patent No.; Revised Table 1-2, Param Nos 3 and 4.

### Revision H (03/10)

Added 4-lead Chip Scale package.

### Revision G (12/09)

Added 11AA161/11LC161 device.

### Revision F (10/09)

Added 3-lead TO-92 Package.

### Revision E (09/08)

Updated UNI/O trademark; Revised Table 1-2, parameters 3 and 5; Updated package drawings.

### Revision D (04/08)

Revised document status to Preliminary; General updates.

### Revision C (03/08)

Removed patent pending notice; Revised Tables 1-1 and 1-2; Section 3.3 (bullet 3) and 3.7 (bullet 2); Product ID System.

### Revision B (01/08)

Revised SOT-23 Package Type; Revised DFN package to TDFN; Section 3.3 (added new bullet item); Section 4.5 note; Table 7-1.

### Revision A (10/07)

Original release of this document.

**NOTES:**

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**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | X[1] | — | X | /XXX |
|---|---|---|---|---|---|
| Device | Device Address | Tape & Reel | | Temperature Range | Package |

| | | |
|---|---|---|
| **Device:** | 11AA01 = | 1-Kbit, 1.8V UNI/O Serial EEPROM |
| | 11LC01 = | 1-Kbit, 2.5V UNI/O Serial EEPROM |
| | 11AA02 = | 2-Kbit, 1.8V UNI/O Serial EEPROM |
| | 11LC02 = | 2-Kbit, 2.5V UNI/O Serial EEPROM |
| | 11AA04 = | 4-Kbit, 1.8V UNI/O Serial EEPROM |
| | 11LC04 = | 4-Kbit, 2.5V UNI/O Serial EEPROM |
| | 11AA08 = | 8-Kbit, 1.8V UNI/O Serial EEPROM |
| | 11LC08 = | 8-Kbit, 2.5V UNI/O Serial EEPROM |
| | 11AA16 = | 16-Kbit, 1.8V UNI/O Serial EEPROM |
| | 11LC16 = | 16-Kbit, 2.5V UNI/O Serial EEPROM |
| **Device Address:** | 0 = | Standard Address – 0xA0 |
| | 1 = | Alternate Address – 0xA1 (11XX161 only) |
| **Tape & Reel:** | T = | Tape and Reel[1] |
| | Blank = | Tube |
| **Temperature Range:** | I = | -40°C to +85°C (Industrial) |
| | E = | -40°C to +125°C (Extended) |
| **Package:** | P = | 8-lead Plastic DIP (300 mil body) |
| | SN = | 8-lead Plastic SOIC (3.90 mm body) |
| | MS = | 8-lead Plastic Micro Small Outline (MSOP) |
| | MNY[2] = | 8-lead 2x3 mm TDFN |
| | TO = | 3-lead Plastic TO-92 |
| | TT = | 3-lead SOT-23 (Tape and Reel only) |
| | CS16K[3] = | Chip Scale (CS), 4-lead (I-temp, “AA”, Tape and Reel only) |

**Examples:**

a) 11AA010-I/P: 1-Kbit, 1.8V Serial EEPROM, Industrial temp., Standard address, PDIP package

b) 11LC160T-E/TT: 16-Kbit, 2.5V Serial EEPROM, Extended temp., Tape & Reel, SOT-23 package

c) 11AA080-I/MS: 8-Kbit, 1.8V Serial EEPROM, Industrial temp., Standard address, MSOP package

d) 11LC020T-I/SN: 2-Kbit, 2.5V Serial EEPROM, Industrial temp., Tape & Reel, Standard Address, SOIC package

e) 11AA040T-I/MNY: 4-Kbit, 1.8V Serial EEPROM, Industrial temp., Tape and Reel, Standard Address, 2 x 3 mm TDFN package, Nickel Palladium Gold finish

f) 11LC161-I/SN: 16-Kbit, 2.5V Serial EEPROM, Industrial temp., Alternate address, SOIC package

g) 11AA020T-I/CS16K: 2-Kbit, 1.8V Serial EEPROM, Industrial temp., Standard address, Chip Scale package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** “Y” indicates a Nickel Palladium Gold (NiPdAu) finish.

**3:** “16K” indicates 160K technology.

## PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | X (1) | — | X | /XXX | XXX (2,3) |
|---|---|---|---|---|---|---|
| Device | Device Address | Tape & Reel | | Temperature Range | Package | Variant |

| | | |
|---|---|---|
| **Device:** | 11LC08 = | 8-Kbit, 2.5V UNI/O Serial EEPROM |
| **Device Address:** | 0 = | Standard Address – 0xA0 |
| **Tape & Reel:** | T = | Tape and Reel(1) |
| | Blank = | Tube |
| **Temperature Range:** | I = | -40°C to +85°C AEC-Q100 Grade 3 |
| | E = | -40°C to +125°C AEC-Q100 Grade 1 |
| **Package:** | TT = | 3-lead SOT-23 (Tape and Reel only) |
| **Variant(2,3):** | 16KVAO = | Standard Automotive, 16K Process |
| | 16KVXX = | Customer-Specific Automotive, 16K Process |

**Examples:**

a) 11LC080T-E/TT16KVAO: 8-Kbit, 2.5V Serial EEPROM, Tape and Reel, Automotive Grade 1, Standard address, SOT-23 package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

**3:** For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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