

Processor Power Management Subsystem

DESCRIPTION

WM8321 is an integrated power-management subsystem which provides a cost-effective, flexible, single-chip solution for power management, specifically targeted at the requirements of a range of low-power portable applications. WM8321 is specifically designed to operate as a system PMIC supporting the ARM9™, ARM11™ and ARM Cortex-A™ series processors at the heart of a range of low-power applications.

The start-up behaviour and configuration is fully programmable in an integrated OTP non-volatile memory. This highly flexible solution helps reduce time-to-market, as changing application requirements can be very easily accommodated in the OTP contents. An external EEPROM can be used to configure the WM8321 for development purposes.

The WM8321 power management subsystem comprises four programmable DC-DC converters and eleven LDO regulators (four of which are low-noise for supplying sensitive analogue subsystems). The integrated OTP bootstrap circuitry controls the start-up sequencing and voltages of the converters and regulators as well as the sequencing of system clocks.

The DC-DC converters deliver high performance and high efficiency across a wide range of operating conditions. They are optimised to support the high load current transients seen in modern processor core domains. DC-DC3 / DC-DC4 can be connected together and operated in 'dual' mode to support an increased current load of up to 1.6A.

An on-chip regulator provides power for always-on PMIC functions such as register map and the RTC. The device provides autonomous backup battery switchover. A low-power LDO is included to support 'Alive' processor power domains external to the WM8321.

A 12-bit Auxiliary ADC supports a wide range of applications for internal as well as external analogue sampling, such as voltage detection and temperature measurement.

WM8321 includes a crystal oscillator and an internal RC oscillator to generate all clock signals for autonomous system start-up and processor clocking. A Secure Real-time Clock (S-RTC) and alarm function is included, capable of waking up the system from low-power modes. A watchdog function is provided to ensure system integrity.

To maximise battery life, highly-granular power management enables each function in the WM8321 subsystem to be independently powered down through a control interface or alternatively through register and OTP-configurable GPIOs. The device offers a standby power consumption of <10uA, making it particularly suitable for portable applications.

The WM8321 is supplied in an 8x8mm 81-lead QFN package, ideal for use in portable systems. The WM8321 forms part of the Wolfson series of audio and power management solutions, and is widely register compatible with the WM831X family of PMIC devices.

FEATURES

Power Management

- 2 x DC-DC buck converter (0.6V - 1.8V, up to 1.25A, DVS)
- 2 x DC-DC buck converter (0.85V - 3.4V, up to 1A)
- 1 x LDO regulator (0.9V - 3.3V, 300mA, 1Ω)
- 2 x LDO regulators (0.9V - 3.3V, 200mA, 1Ω)
- 3 x LDO regulators (0.9V - 3.3V, 100mA, 2Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 200mA, 1Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 150mA, 2Ω)
- 1 x 'Alive' regulator (0.8V - 1.55V, up to 10mA)

System Control

- I²C or SPI compatible primary control interface
- Comprehensive interrupt scheme
- Watchdog timer and system reset control
- Autonomous power sequencing and fault detection
- OTP memory bootstrap configuration function

Additional Features

- Auxiliary ADC for multi-function analogue measurement
- 128-bit pseudo-random unique ID
- Secure Real-Time Clock with wake-up alarm
- 12 x configurable multi-function (GPIO) pins
- Comprehensive clocking scheme: low-power 32kHz RTC crystal oscillator, GPIO clock output and 4MHz RC clock for power management
- System LED outputs indicating device power state, and fault status

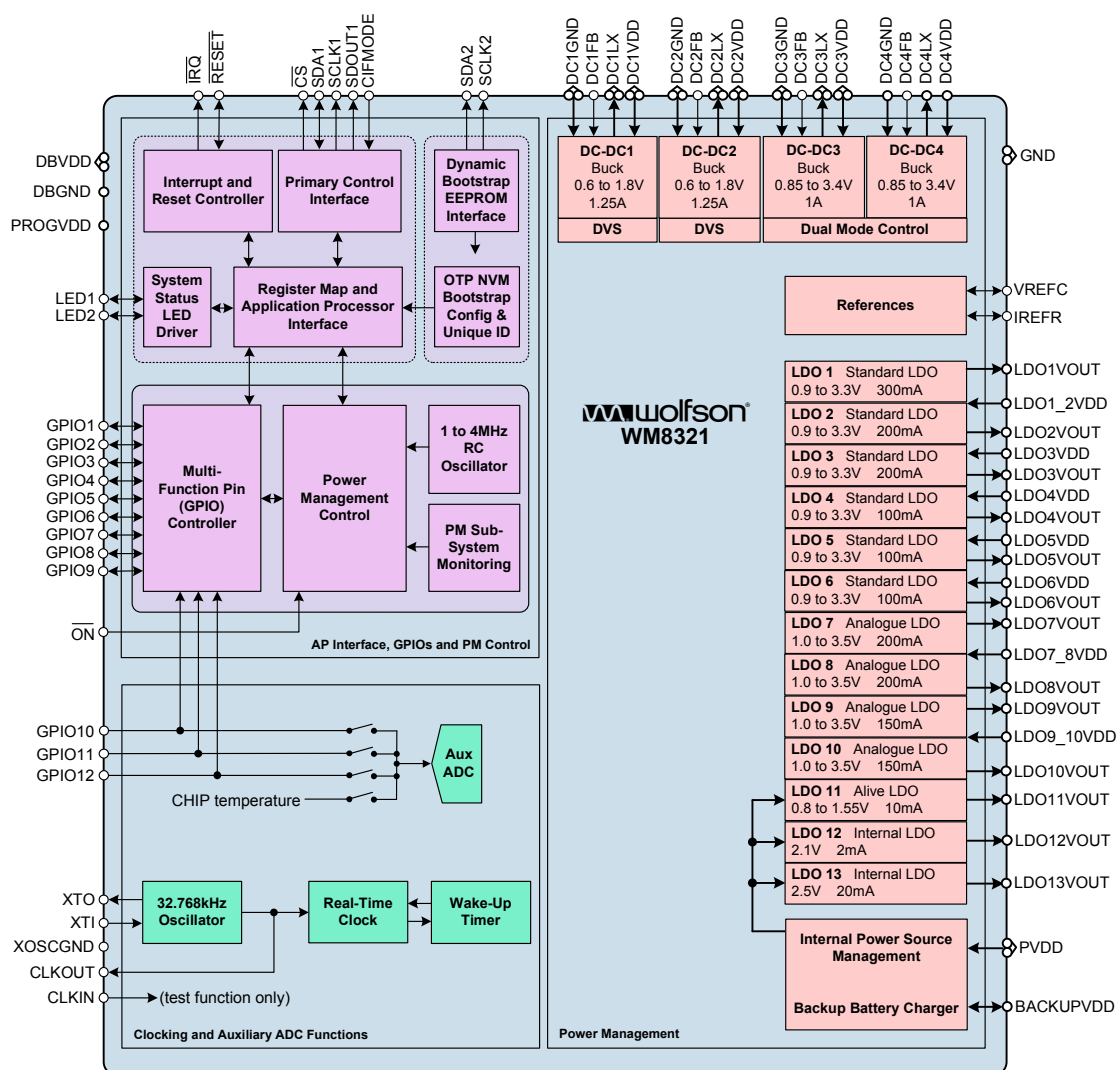
Package Options

- 8x8mm, 0.85mm thick, 81-lead QFN package

APPLICATIONS

- Cellular Handsets
- Smartphones
- Electronic Books
- Portable Media Players
- Mobile Internet Devices
- Electronic Gaming Devices
- Netbooks
- Set Top Box

BLOCK DIAGRAM



TYPICAL APPLICATIONS

The WM8321 is designed as a system PMIC device that generates configurable DC supplies to power processors and associated peripherals within a system. The WM8321 provides four step-down DC-DC converters. Two of these can operate in dual mode, providing an increased current capability. Eleven LDO regulators provide a high degree of flexibility to provide power to multiple devices, with the capability to power-up and power-down different circuits independently.

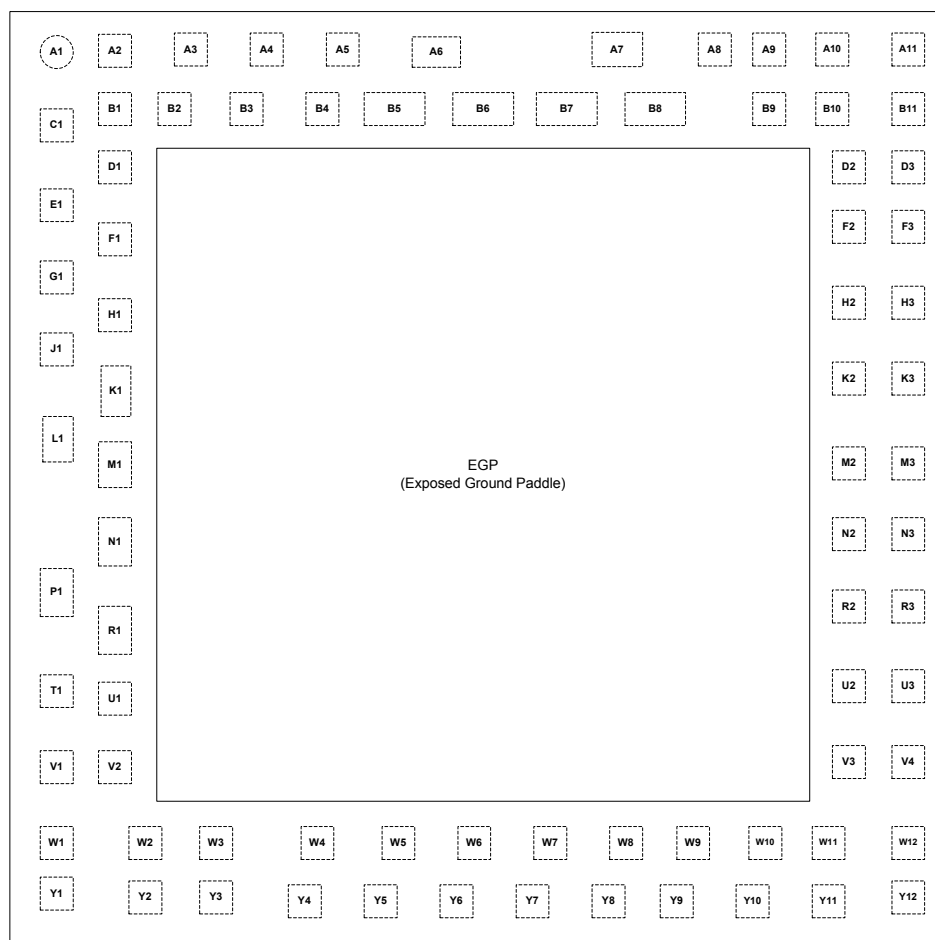
Two of the DC-DC step-down converters are specifically designed to handle rapid changes in load current, as required by modern application processors; selectable operating modes allow the converters to be optimally configured for light, heavy or transient load conditions; they can also be tailored for minimum PCB area, maximum performance, or for maximum efficiency. The analogue LDOs provide low-noise outputs suitable for powering sensitive circuits such as RF / Wi-Fi / cellular handset applications.

The WM8321 powers up the converters and LDOs according to a programmable sequence. A configurable 'SLEEP' state is also available, providing support for an alternate configuration, typically for low-power / standby operation. The power control sequences and many other parameters can be stored in an integrated user-programmable OTP memory or may be loaded from an external memory. The WM8321 supports the programming and verification of the integrated OTP memory.

A backup battery supply can be connected to the WM8321 in order to maintain the Real Time Clock (RTC) in the absence of the primary supply. The WM8321 provides a battery charger for the backup battery.

Programmable GPIO pins may be configured as hardware inputs for general use or for selecting different power management configurations. As outputs, the GPIOs can provide indications of the device status, or may be used as control signals for other power management circuits. The WM8321 also provides two LED drivers, which can be controlled manually or configured as status indicators for the OTP memory programmer or operating power state.

PIN CONFIGURATION



Top View - WM8321

ORDERING INFORMATION

| ORDER CODE | TEMPERATURE RANGE (T _A) | PACKAGE | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|---------------|-------------------------------------|---|----------------------------|----------------------------|
| WM8321GEFL/V | -40°C to +85°C | 81-lead QFN (8 x 8mm) (Pb-free) | MSL3 | 260°C |
| WM8321GEFL/RV | -40°C to +85°C | 81-lead QFN (8 x 8mm) (Pb-free, tape and reel) | MSL3 | 260°C |

Note:

Reel quantity = 2,200

PIN DESCRIPTION

Notes:

1. Pins are sorted by functional groups.
2. The power domain associated with each pin is noted; VPMIC is the domain powered by LDO12 for the 'always-on' functions internal to the WM8321.

| PIN | NAME | TYPE | POWER DOMAIN | DESCRIPTION | |
|--|---------|-----------------|-----------------|---|--|
| Clocking and Real Time Clock | | | | | |
| Y12 | XTO | Analogue Output | VPMIC | Crystal Drive Output | |
| Y11 | XTI | Analogue Input | | Crystal Drive Input or 32.768kHz CMOS Clock Input | |
| W11 | XOSCGND | Supply | | Crystal Oscillator Ground | |
| H1 | CLKOUT | Digital Output | DBVDD2 | CMOS Clock Output | |
| G1 | CLKIN | Digital Input | | CMOS Clock Input (test function only; this pin should be connected to GND) | |
| General Purpose Input / Output and Auxiliary ADC | | | | | |
| D3 | GPIO1 | Digital I/O | DBVDD1 or VPMIC | GPIO Pin 1 | |
| F2 | GPIO2 | Digital I/O | | GPIO Pin 2 | |
| F3 | GPIO3 | Digital I/O | | GPIO Pin 3 | |
| W4 | GPIO4 | Digital I/O | DBVDD1 or PVDD | GPIO Pin 4 | |
| Y4 | GPIO5 | Digital I/O | | GPIO Pin 5 | |
| W5 | GPIO6 | Digital I/O | | GPIO Pin 6 | |
| H2 | GPIO7 | Digital I/O | DBVDD1 or VPMIC | GPIO Pin 7 | |
| H3 | GPIO8 | Digital I/O | | GPIO Pin 8 | |
| K3 | GPIO9 | Digital I/O | | GPIO Pin 9 | |
| Y5 | GPIO10 | Digital I/O | DBVDD1 or PVDD | GPIO Pin 10 / Auxiliary ADC input | |
| Y6 | GPIO11 | Digital I/O | | GPIO Pin 11 / Auxiliary ADC input | |
| W6 | GPIO12 | Digital I/O | | GPIO Pin 12 / Auxiliary ADC input | |
| Processor Interface and IC Control | | | | | |
| W9 | ON | Digital Input | VPMIC | ON Request Pin (Internal pull-up) | |
| B10 | RESET | Digital I/O | DBVDD1 | System Reset Input and Open Drain Output. (Internal pull-up) | |
| A11 | IRQ | Digital Output | DBVDD1 | PMIC Interrupt Flag Output. Configurable Open Drain / CMOS mode. (Internal pull-up in Open Drain mode.) | |
| E1 | CIFMODE | Digital Input | DBVDD2 | Primary Control Interface Mode Select: 0 = I ² C Compatible Control Interface Mode 1 = SPI Compatible Control Interface Mode | |
| | | | | SPI Compatible Control Interface Mode | I ² C Compatible Control Interface Mode |
| D2 | SDOUT1 | Digital Output | DBVDD1 | Control Interface Serial Data Out | No Function |
| B9 | SCLK1 | Digital Input | | Control Interface Serial Clock | Control Interface Serial Clock |
| A9 | SDA1 | Digital I/O | | Control Interface Serial Data In | Control Interface Serial Data Input and Open Drain Output. (Output can extend above DBVDD1 domain.) |
| A10 | CS | Digital Input | | Control Interface Chip Select | I ² C Address Select: 0 = 68h 1 = 6Ch |

| PIN | NAME | TYPE | POWER DOMAIN | DESCRIPTION |
|-------------------------------------|-----------------------|-----------------|--------------|---|
| Y10 | SCLK2 | Digital I/O | VPMIC | Control Interface Serial Clock for external DBE EEPROM (Internal pull-down) |
| W10 | SDA2 | Digital I/O | | Control Interface Serial Data to/from external DBE EEPROM (Internal pull-down) |
| B11 | DBVDD1 | Supply | | Digital Buffer Supply |
| F1 | DBVDD2 | Supply | | Digital Buffer Supply |
| OTP Memory | | | | |
| Y3 | PROGVDD | Supply | | High-voltage input for OTP programming. |
| DC-DC Converters and LDO Regulators | | | | |
| EGP | Exposed Ground Paddle | Analogue Ground | | Ground |
| B7 | DC1GND | Supply | DC1VDD | DC-DC1 Power Ground |
| A8 | DC1FB | Analogue Input | | DC-DC1 Feedback Pin |
| A7 | DC1LX | Analogue I/O | | DC-DC1 Inductor Connection |
| B8 | DC1VDD | Supply | | DC-DC1 Power Input (System VDD Supply) |
| B6 | DC2GND | Supply | DC2VDD | DC-DC2 Power Ground |
| A5 | DC2FB | Analogue Input | | DC-DC2 Feedback Pin |
| A6 | DC2LX | Analogue I/O | | DC-DC2 Inductor Connection |
| B5 | DC2VDD | Supply | | DC-DC2 Power Input (System VDD Supply) |
| M1 | DC3GND | Supply | DC3VDD | DC-DC3 Power Ground |
| J1 | DC3FB | Analogue Input | | DC-DC3 Feedback Pin |
| L1 | DC3LX | Analogue I/O | | DC-DC3 Inductor Connection |
| K1 | DC3VDD | Supply | | DC-DC3 Power Input (System VDD Supply) |
| N1 | DC4GND | Supply | DC4VDD | DC-DC4 Power Ground |
| T1 | DC4FB | Analogue Input | | DC-DC4 Feedback Pin |
| P1 | DC4LX | Analogue I/O | | DC-DC4 Inductor Connection |
| R1 | DC4VDD | Supply | | DC-DC4 Power Input (System VDD Supply) |
| A3 | LDO1_2VDD | Supply | | LDO1 & LDO2 Power Input |
| B2 | LDO1VOUT | Analogue Output | LDO1VDD | LDO1 Power Output |
| B3 | LDO2VOUT | Analogue Output | LDO2VDD | LDO2 Power Output |
| B4 | LDO3VDD | Supply | | LDO3 Power Input |
| A4 | LDO3VOUT | Analogue Output | LDO3VDD | LDO3 Power Output |
| W3 | LDO4VDD | Supply | | LDO4 Power Input |
| Y2 | LDO4VOUT | Analogue Output | LDO4VDD | LDO4 Power Output |
| Y1 | LDO5VDD | Supply | | LDO5 Power Input |
| W2 | LDO5VOUT | Analogue Output | LDO5VDD | LDO5 Power Output |
| W1 | LDO6VDD | Supply | | LDO6 Power Input |
| V1 | LDO6VOUT | Analogue Output | LDO6VDD | LDO6 Power Output |
| R3 | LDO7_8VDD | Supply | | LDO7 & LDO8 Power Input |
| N2 | LDO7VOUT | Analogue Output | LDO7VDD | LDO7 Power Output |
| R2 | LDO8VOUT | Analogue Output | LDO8VDD | LDO8 Power Output |
| M2 | LDO9_10VDD | Supply | | LDO9 Power Input |
| M3 | LDO9VOUT | Analogue Output | LDO9VDD | LDO9 Power Output |
| N3 | LDO10VOUT | Analogue Output | LDO10VDD | LDO10 Power Output |
| V3 | LDO11VOUT | Analogue Output | PVDD2 | LDO11 (Alive) Power Output |
| Y8 | LDO12VOUT | Analogue I/O | PVDD2 | LDO12 (Internal VPMIC) Output; not for general use |
| W7 | LDO13VOUT1 | Analogue I/O | PVDD2 | LDO13 (Internal INTVDD) Output; not for general use |
| K2 | LDO13VOUT2 | Analogue I/O | PVDD2 | LDO13 - Connect to LDO13VOUT1 (W7) |

| PIN | NAME | TYPE | POWER DOMAIN | DESCRIPTION |
|--------------------------------|-----------|----------------|--------------|--|
| Voltage and Current References | | | | |
| W8 | VREFC | Analogue I/O | VPMIC | Voltage Reference capacitor connection point |
| Y9 | IREFR | Analogue I/O | | Current Reference resistor connection point |
| System Power | | | | |
| U1 | PVDD1 | Supply | | System VDD Supply |
| Y7 | PVDD2 | Supply | | System VDD Supply |
| V4 | PVDD3 | Supply | | System VDD Supply |
| W12 | BACKUPVDD | Supply | | Secondary (Backup) Battery Supply |
| System LED Drivers | | | | |
| U3 | LED1 | Digital Output | PVDD3 | Status LED Driver 1. Open Drain Output |
| U2 | LED2 | Digital Output | | Status LED Driver 2. Open Drain Output |
| Do Not Connect | | | | |
| A1, A2, B1, C1, D1, V2 | DNC | | | Do Not Connect |

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8321 has been classified as MSL3.

| CONDITION | MIN | MAX |
|---|-----------------------|--------------|
| OTP Programming Supply (PROGVDD) | -0.3V | 7.0V |
| System supply (PVDD) | -0.3V | 7.0V |
| Input voltage for LDO regulators | -0.3V | 7.0V |
| Input voltage for DC-DC converters | -0.3V | 7.0V |
| Digital buffer supply (DBVDD) | -0.3V | 4.5V |
| Voltage range for digital inputs | -0.3V | DBVDD + 0.3V |
| Operating Temperature Range, T _A | -40°C | +85°C |
| Junction Temperature, T _J | -40°C | +125°C |
| Thermal Impedance Junction to Ambient, θ _{JA} | | TBC |
| Storage temperature prior to soldering | 30°C max / 60% RH max | |
| Storage temperature after soldering | -65°C | +150°C |
| Soldering temperature (10 seconds) | | +260°C |
| Note: These ratings assume that all ground pins are at 0V. | | |

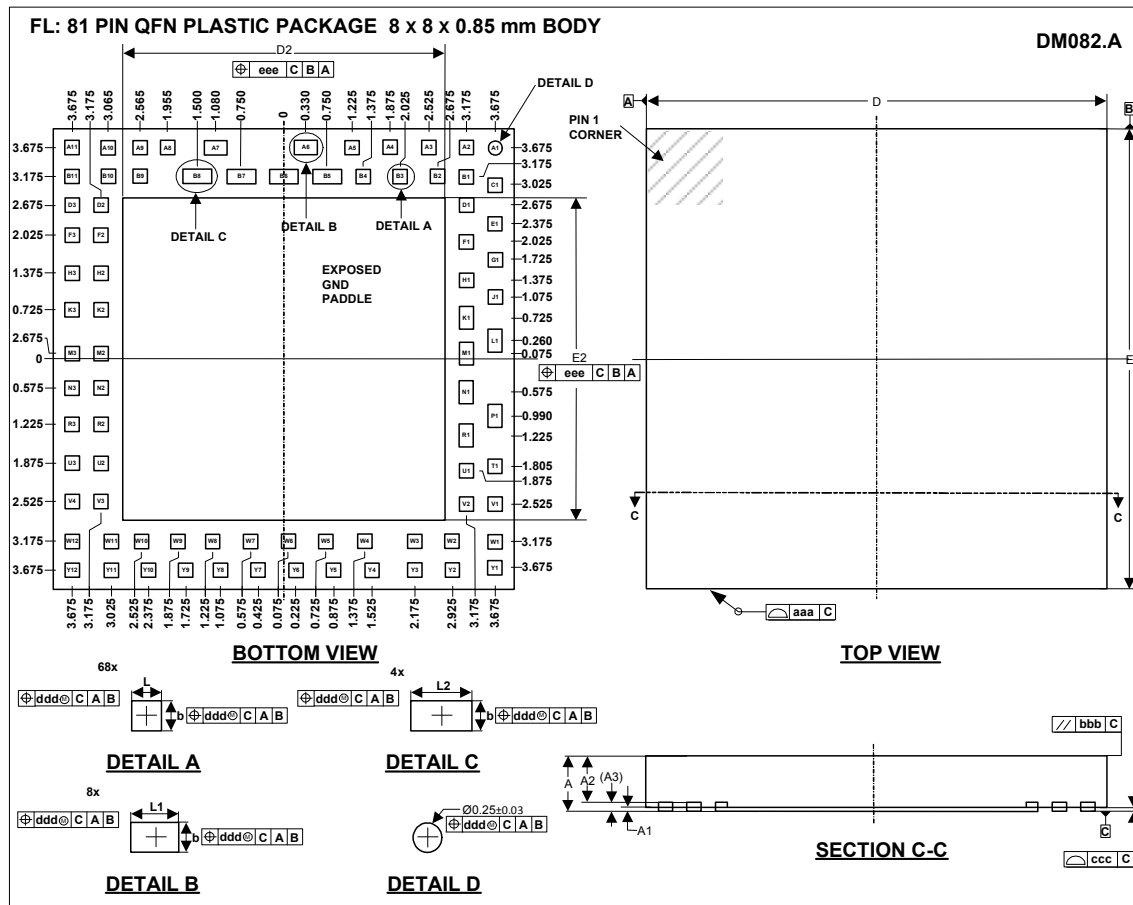
RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|-----------------------------------|-----------|------|-----|------|-------|
| System power source | PVDD | 2.7 | | 5.5 | V |
| Backup Battery power source | BACKUPVDD | | | 3.6 | V |
| Digital buffer supply | DBVDD | 1.71 | | 3.6 | V |
| OTP Programming Supply (see note) | PROGVDD | 6.25 | 6.5 | 6.75 | V |
| | LDO12VOUT | | 3.3 | | V |
| Ground | GND | | 0 | | V |

Note:

The OTP Programming Supply PROGVDD should only be present when programming the OTP. At other times, this pin should be left unconnected. The LDO12VOUT must be overdriven by an external supply when programming the OTP. At other times, the voltage at this pin is driven by the internal circuits of the WM8321.

PACKAGE DIAGRAM



| Symbols | Dimensions (mm) | | | NOTE |
|--|-----------------|---------------|------|------|
| | MIN | NOM | MAX | |
| A | --- | --- | 0.85 | |
| A1 | 0.02 | 0.05 | 0.08 | |
| A2 | 0.64 | 0.675 | 0.71 | |
| A3 | 0.12 | 0.13 | 0.14 | |
| b | 0.22 | 0.25 | 0.28 | |
| D | | 8 BSC | | |
| D2 | 5.55 | 5.60 | 5.65 | |
| E | | 8 BSC | | |
| E2 | 5.55 | 5.60 | 5.65 | |
| L | 0.22 | 0.25 | 0.28 | |
| L1 | 0.37 | 0.4 | 0.43 | |
| L2 | 0.47 | 0.5 | 0.53 | |
| Tolerances of Form and Position | | | | |
| aaa | | 0.10 | | |
| bbb | | 0.20 | | |
| ccc | | 0.05 | | |
| ddd | | 0.08 | | |
| eee | | 0.10 | | |
| REF | | JEDEC, MO-220 | | |

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETRES
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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