



PMV48XP

20 V, 3.5 A P-channel Trench MOSFET

Rev. 1 — 21 December 2010

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- Very fast switching

1.3 Applications

- High-side loadswitch
- High-speed line driver
- Relay driver
- Switching circuits

1.4 Quick reference data

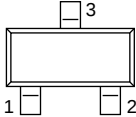
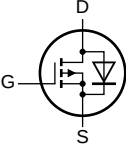
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_{amb} = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-12	-	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}$; $T_{amb} = 25\text{ °C}$	[1]	-	-3.5	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}$; $I_D = -2.4\text{ A}$; pulsed; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.01$; $T_j = 25\text{ °C}$	-	48	55	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT23 (TO-236AB)	 017aaa094
2	S	source		
3	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV48XP	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PMV48XP	KN%

[1] % = placeholder for manufacturing site code

5. Limiting values

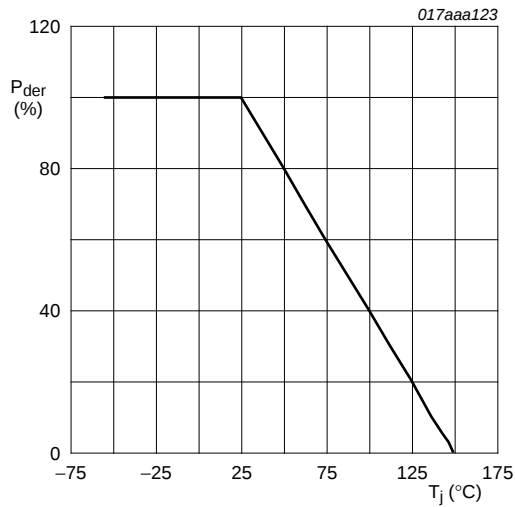
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _{amb} = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-3.5	A
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-2.2	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-14	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	510	mW
			[1]	-	930	mW
		T _{sp} = 25 °C		-	4150	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-1	A

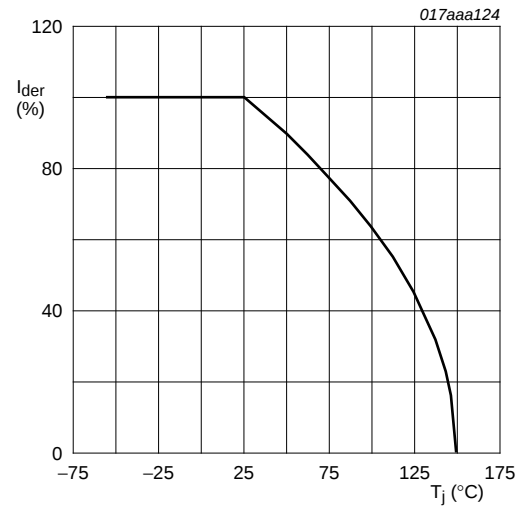
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



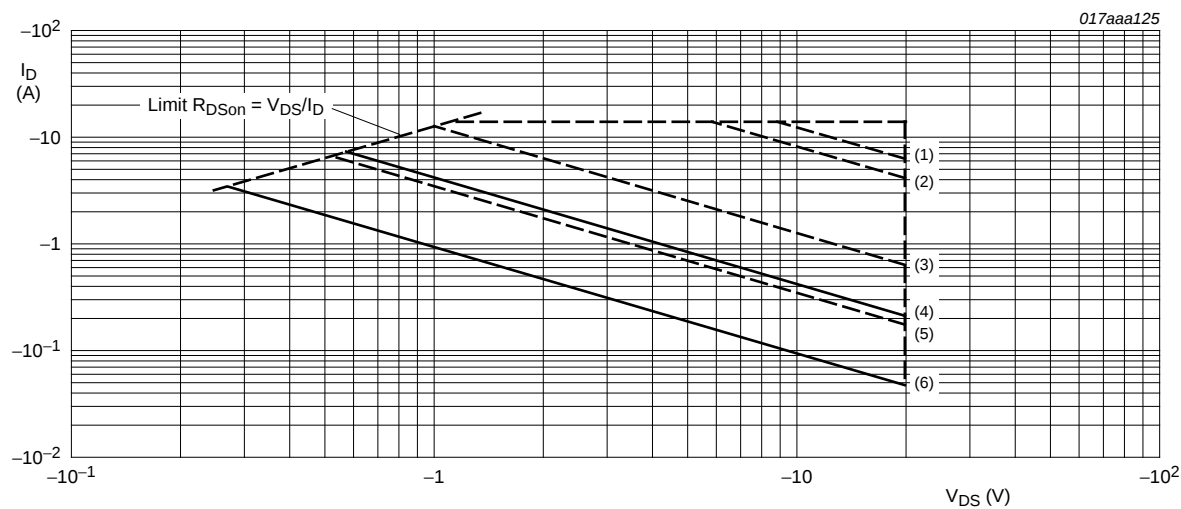
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse
(1) $t_p = 100\ \mu s$
(2) $t_p = 1\ ms$
(3) $t_p = 10\ ms$
(4) DC; $T_{sp} = 25\ ^\circ C$
(5) $t_p = 100\ ms$
(6) DC; $T_{amb} = 25\ ^\circ C$; drain mounting pad $6\ cm^2$

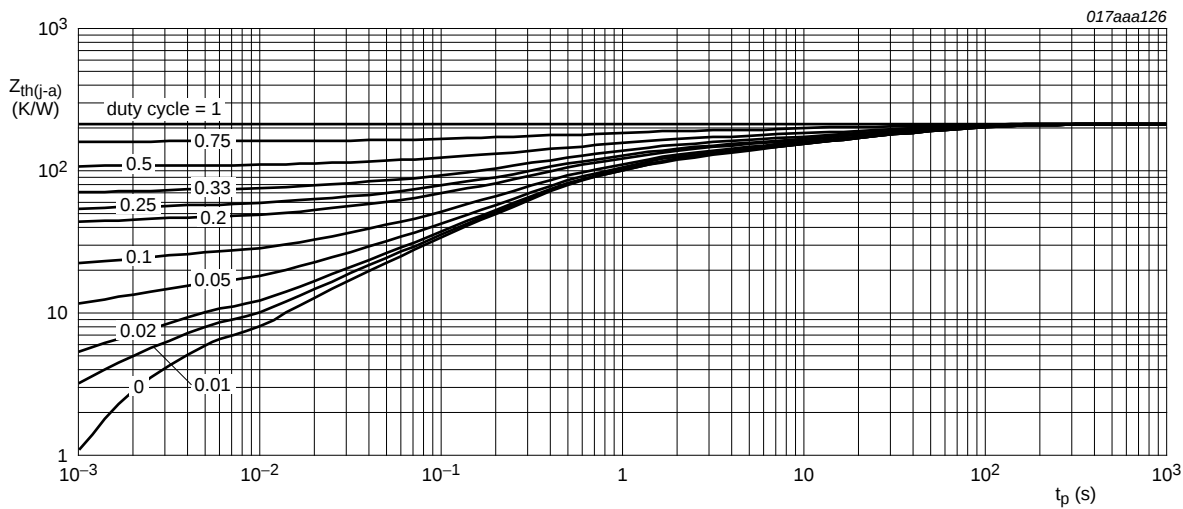
Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

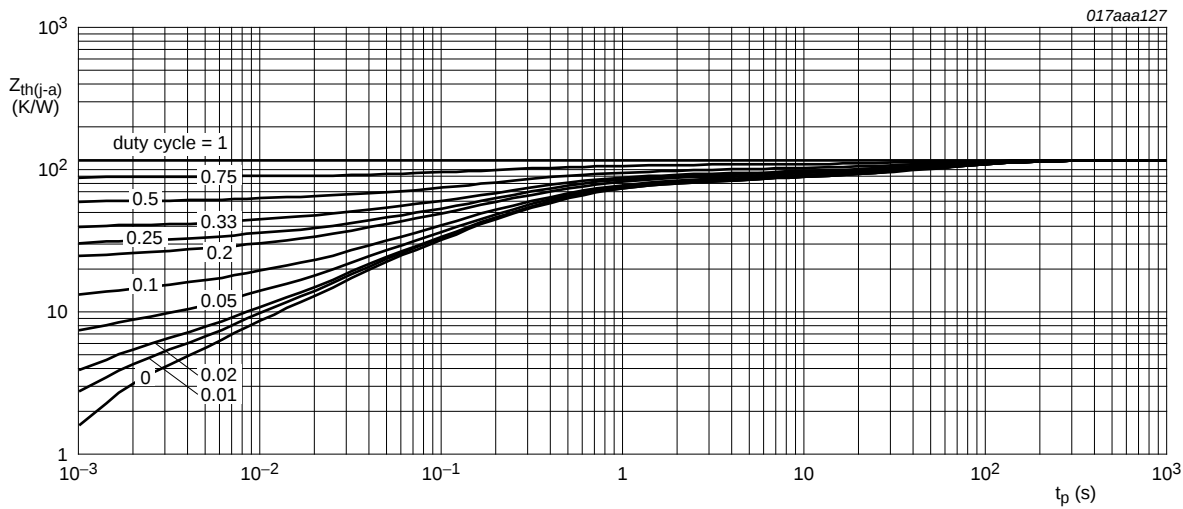
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	213	245 K/W
			[2]	-	117	135 K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	25	30	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain $6\ cm^2$.



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C	-20	-	-	V
V _{GSt}	gate-source threshold voltage	I _D = -250 μA; V _{DS} = V _{GS} ; T _j = 25 °C	-0.75	-1	-1.25	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _{amb} = 25 °C	-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -2.4 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.01 ; T _j = 25 °C	-	48	55	mΩ
		V _{GS} = -4.5 V; I _D = -2.4 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.01 ; T _j = 150 °C	-	70	80	mΩ
		V _{GS} = -2.5 V; I _D = -2 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.01 ; T _j = 25 °C	-	71	81	mΩ
g _{fs}	forward transconductance	V _{DS} = -12 V; I _D = -2 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.01 ; T _j = 25 °C	-	12	-	S
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = -1 A; V _{DS} = -10 V; V _{GS} = -4.5 V; T _j = 25 °C	-	8.5	11	nC
Q _{GS}	gate-source charge		-	1.8	-	nC
Q _{GD}	gate-drain charge		-	1.8	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = -10 V; f = 1 MHz; T _j = 25 °C	-	1000	-	pF
C _{oss}	output capacitance		-	130	-	pF
C _{rss}	reverse transfer capacitance		-	90	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; V _{GS} = -4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C; I _D = -1 A	-	11	-	ns
t _r	rise time		-	13	-	ns
t _{d(off)}	turn-off delay time		-	61	-	ns
t _f	fall time		-	23	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = -2.4 A; V _{GS} = 0 V; T _j = 25 °C; t _p ≤ 300 μs; δ ≤ 0.01	-	-0.82	-1.2	V

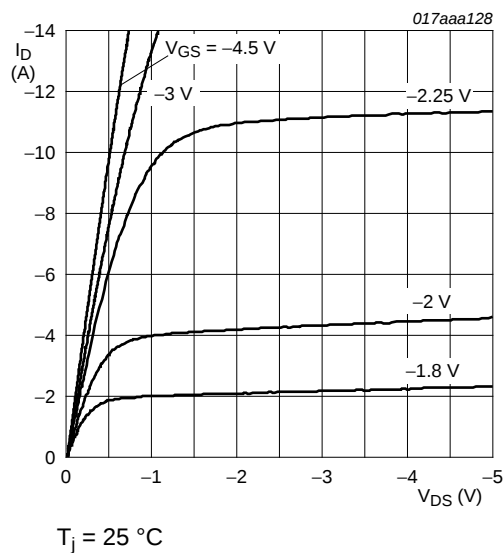


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

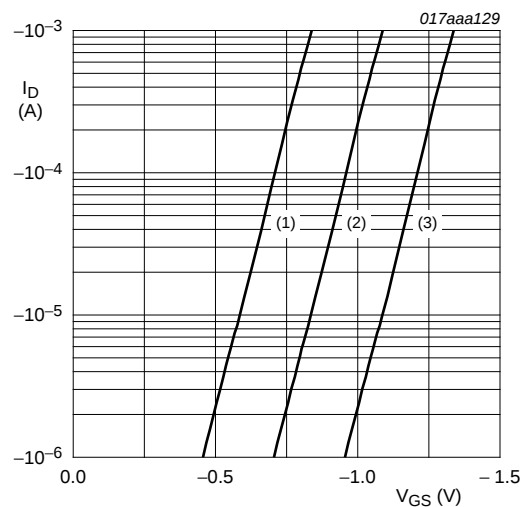


Fig 7. Sub-threshold drain current as a function of gate-source voltage

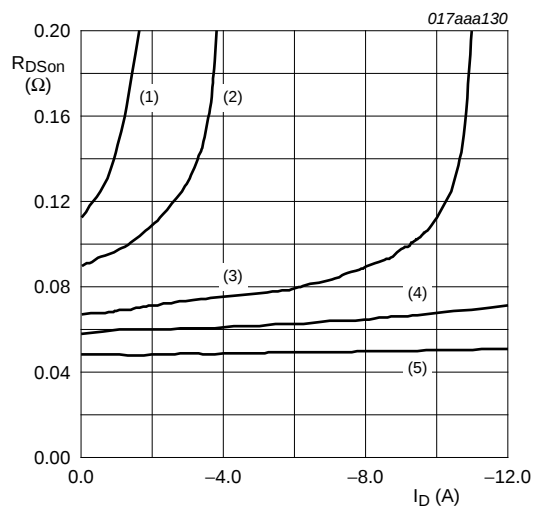


Fig 8. Drain-source on-state resistance as a function of drain current; typical values

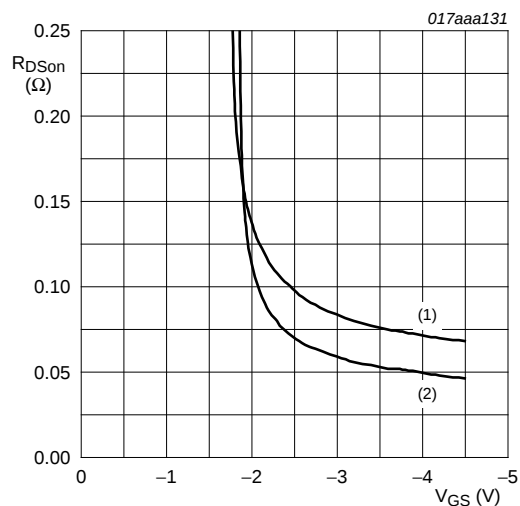
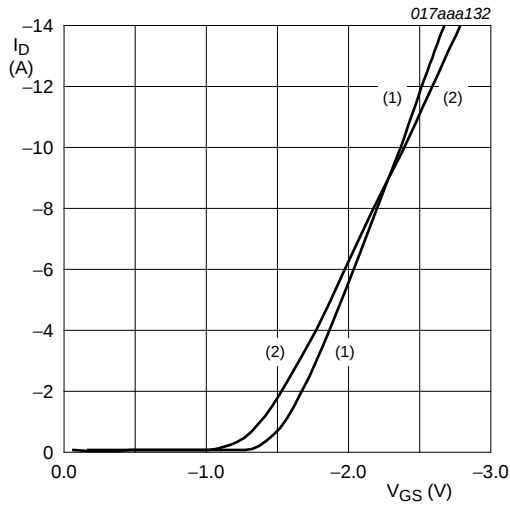


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

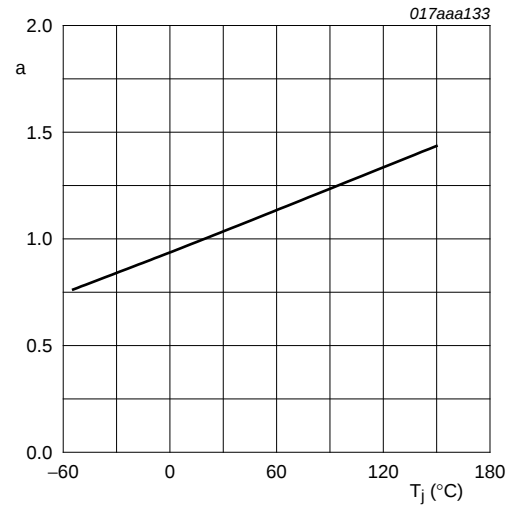


$$V_{DS} > I_D \times R_{DSon}$$

(1) $T_j = 25\text{ }^{\circ}\text{C}$

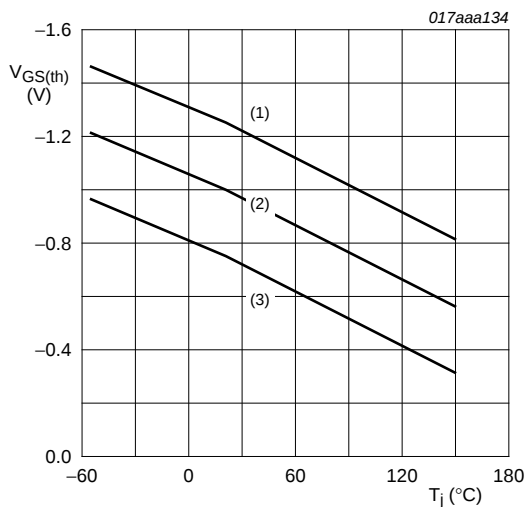
(2) $T_j = 150\text{ }^{\circ}\text{C}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



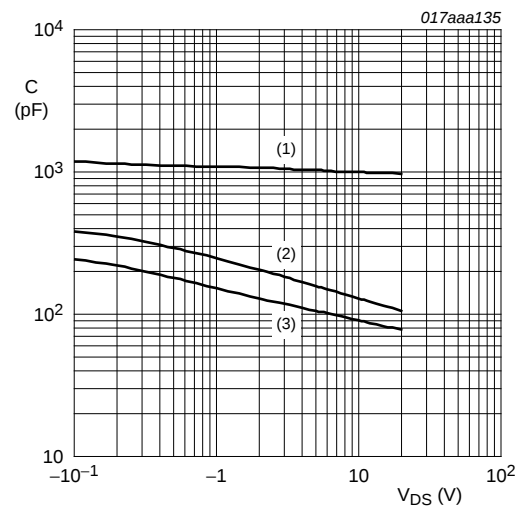
$$I_D = -0.25\text{ mA}; V_{DS} = V_{GS}$$

(1) maximum values

(2) typical values

(3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$$

(1) C_{iss}

(2) C_{oss}

(3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

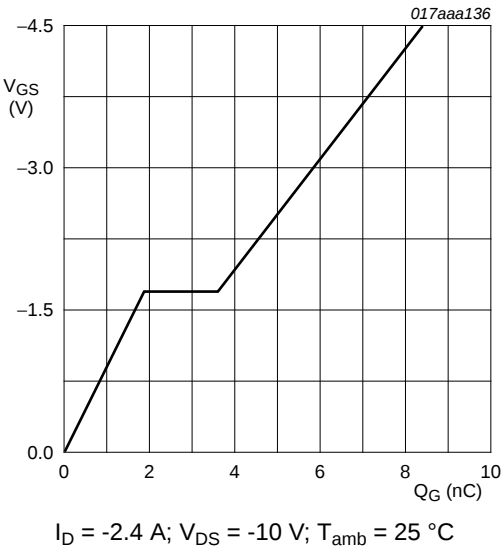


Fig 14. Gate-source voltage as a function of gate charge; typical values

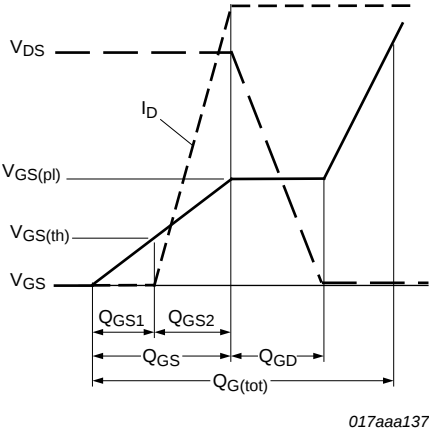


Fig 15. Gate charge waveform definitions

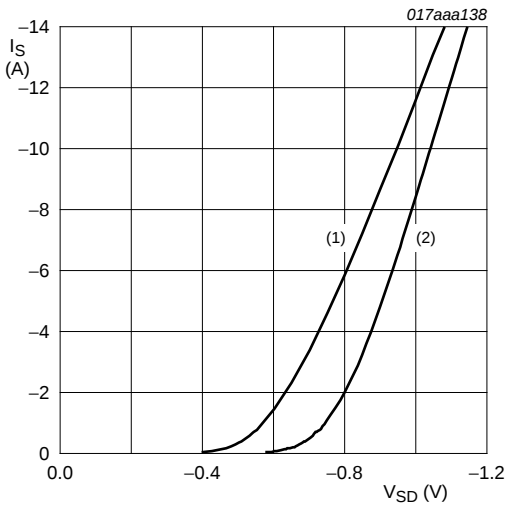


Fig 16. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic surface-mounted package; 3 leads

SOT23

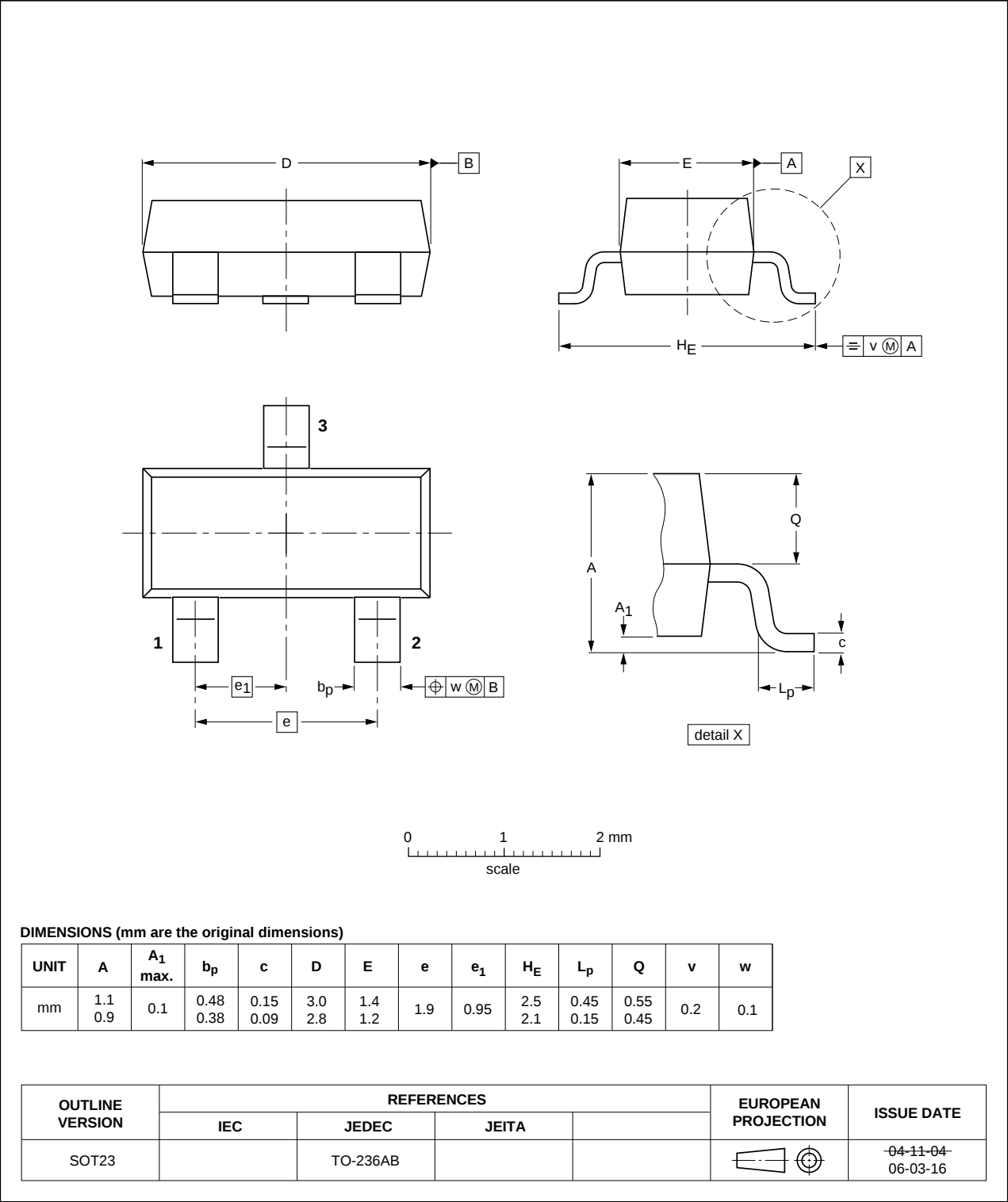


Fig 17. Package outline SOT23 (TO-236AB)

9. Soldering

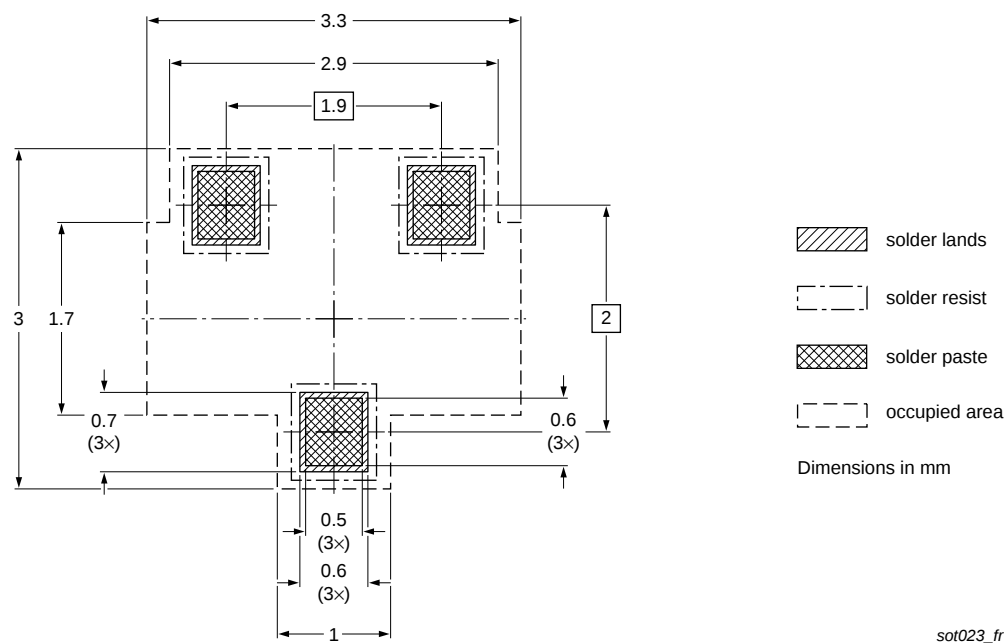


Fig 18. Reflow soldering footprint for SOT23 (TO-236AB)

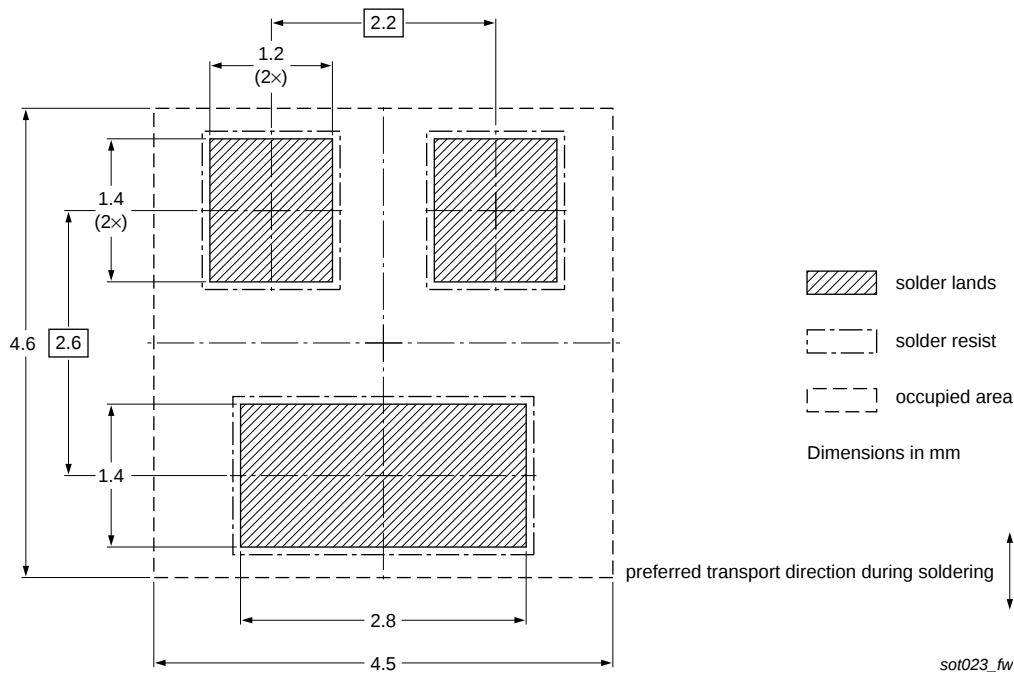


Fig 19. Wave soldering footprint for SOT23 (TO-236AB)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMV48XP v.1	20101221	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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