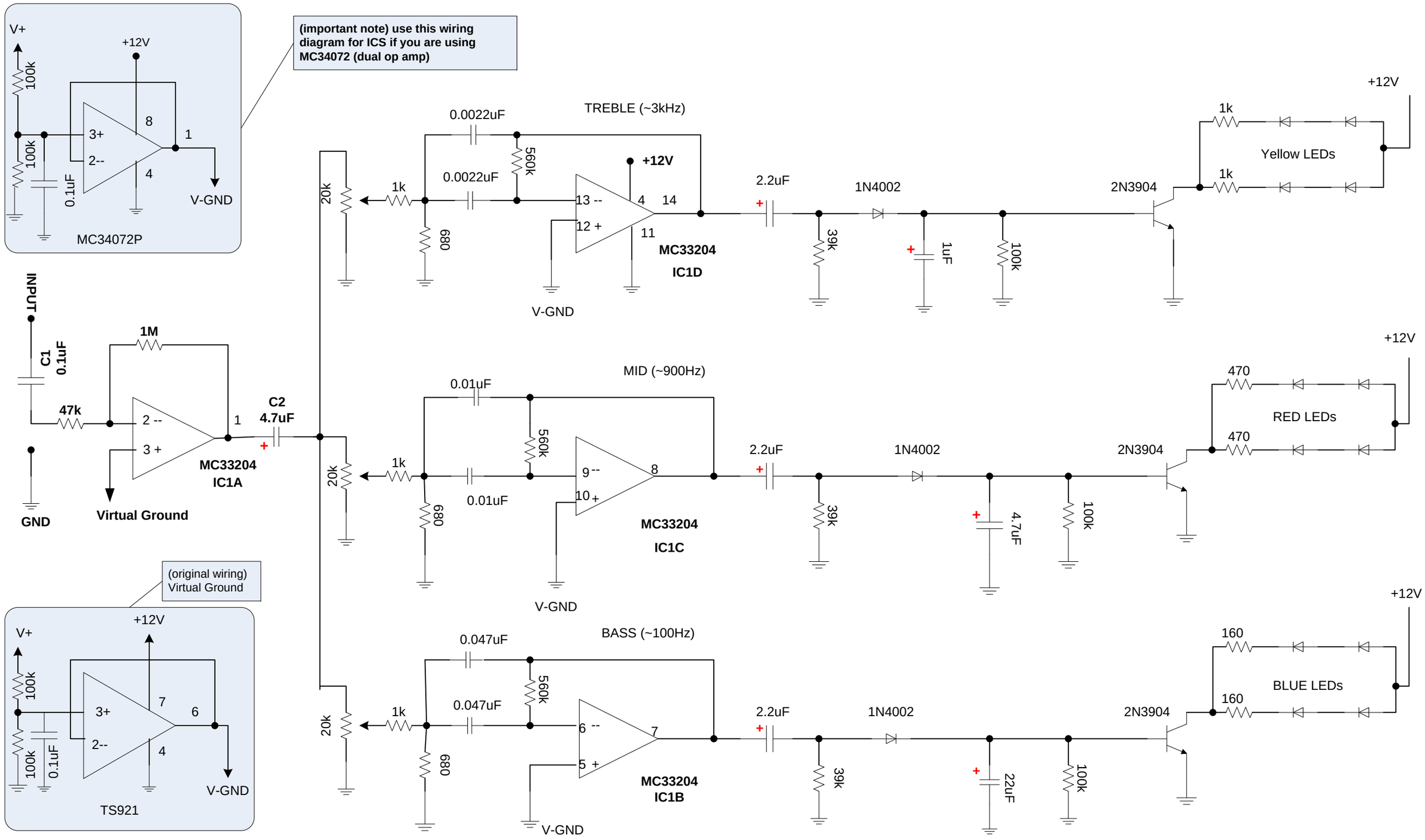

(important note) use this wiring diagram for ICS if you are using MC34072 (dual op amp)
V+
+12V
100k
100k
0.1uF
3+
2--
8
1
4
V-GND
MC34072P
INPUT
C1
0.1uF
1M
47k
2 --
3 +
1
MC33204
IC1A
Virtual Ground
GND
C2
4.7uF
20k
TREBLE (~3kHz)
0.0022uF
0.0022uF
560k
1k
680
+12V
13 --
12 +
4
14
11
MC33204
IC1D
V-GND
2.2uF
39k
1N4002
1uF
100k
2N3904
+12V
1k
Yellow LEDs
1k
MID (~900Hz)
0.01uF
0.01uF
560k
1k
680
9 --
10 +
8
MC33204
IC1C
V-GND
2.2uF
39k
1N4002
4.7uF
100k
2N3904
+12V
470
RED LEDs
470
(original wiring)
Virtual Ground
V+
+12V
100k
100k
0.1uF
3+
2--
7
6
4
V-GND
TS921
BASS (~100Hz)
0.047uF
0.047uF
560k
1k
680
6 --
5 +
7
MC33204
IC1B
V-GND
2.2uF
39k
1N4002
22uF
100k
2N3904
+12V
160
BLUE LEDs
160

TS921

RAIL TO RAIL HIGH OUTPUT CURRENT SINGLE OPERATIONAL AMPLIFIER

- RAIL TO RAIL INPUT AND OUTPUT
- LOW NOISE : **9nV/√(Hz)**
- LOW DISTORTION
- HIGH OUTPUT CURRENT : **80mA** (able to drive 32Ω loads)
- HIGH SPEED : **4MHz, 1V/µs**
- OPERATING FROM **2.7V to 12V**
- ESD INTERNAL PROTECTION : 1.5KV
- LATCH-UP IMMUNITY
- MACROMODEL INCLUDED IN THIS SPECIFICATION

DESCRIPTION

The TS921 is a RAIL TO RAIL single BiCMOS operational amplifier optimized and fully specified for 3V and 5V operation.

High output current allows low load impedances to be driven.

The TS921 exhibits a very low noise, low distortion, low offset and high ouput current capability making this device an excellent choice for high quality, low voltage or battery operated audio systems.

The device is stable for capacitive loads up to 500pF.

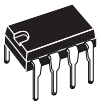
APPLICATIONS

- headphone amplifier
- piezoelectric speaker driver
- sound cards, multimedia systems
- line driver, actuator driver
- servo amplifier
- mobile phone and portable communication sets
- instrumentation with low noise as key factor

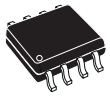
ORDER CODE

Part Number	Temperature Range	Package		
		N	D	P
TS921I	-40°C, +125°C	•	•	•

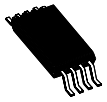
N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)
P = Thin Shrink Small Outline Package (TSSOP) - only available in Tape & Reel (PT)



N
DIP8
(Plastic Package)

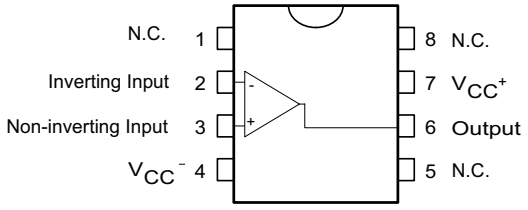


D
SO8
(Plastic Micropackage)



P
TSSOP8
(Thin Shrink Small Outline Package)

PIN CONNECTIONS (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	14	V
V_{id}	Differential Input Voltage [2]	±1	V
V_i	Input Voltage [3]	-0.3 to 14	V
T_{oper}	Operating Free Air Temperature Range	-40 to +125	°C
I_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
	Output Short Circuit Duration	see note [4]	°C

1. All voltages values, except differential voltage are with respect to network ground terminal.
2. Differential voltagesare the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuit on all amplifiers

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 12	V
V_{icm}	Common Mode Input Voltage Range	V_{CC}^- -0.2 to V_{CC}^+ +0.2	V

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = 3V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage Tmin. ≤ Tamb ≤ Tmax.			3 5	mV
DV_{io}	Input Offset Voltage Drift		2		µV/°C
I_{io}	Input Offset Current V_{out} = 1.5V			30	nA
I_{ib}	Input Bias Current V_{out} = 1.5V		15	100	nA
V_{OH}	High Level Output Voltage RL = 600Ω RL = 32Ω	2.87	2.63		V
V_{OL}	Low Level Output Voltage RL = 600Ω RL = 32Ω		180	100	mV
A_{vd}	Large Signal Voltage Gain (V_{out} = 2Vpk-pk) RL = 600Ω RL = 32Ω		35 16		V/mV
I_{CC}	Supply Current no load, V_{out} = Vcc/2		1	1.5	mA
GBP	Gain Bandwith Product RL = 600Ω		4		MHz
CMR	Common Mode Rejection Ratio	60	80		dB
SVR	Supply Voltage Rejection Ratio Vcc = 2.7 to 3.3 V	60	80		dB
I_o	Output Short Circuit Current	50	80		mA
SR	Slew Rate	0.7	1.3		V/µs
ϕm	Phase Margin at Unit Gain RL = 600Ω, C_L =100pF		68		Degrees
G_m	Gain Margin RL = 600Ω, C_L =100pF		12		dB
e_n	Equivalent Input Noise Voltage f = 1kHz		9		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion V_{out} = 2Vpk-pk, F = 1kHz, A_V = 1, R_L =600Ω		0.005		%

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = 5V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $T_{min.} \le T_{amb} \le T_{max.}$			3 5	mV
DV_{io}	Input Offset Voltage Drift		2		µV/°C
I_{io}	Input Offset Current V_{out} = 1.5V			30	nA
I_{ib}	Input Bias Current V_{out} = 1.5V		15	100	nA
V_{OH}	High Level Output Voltage R_L = 600Ω R_L = 32Ω	4.85	4.4		V
V_{OL}	Low Level Output Voltage R_L = 600Ω R_L = 32Ω		300	120	mV
A_{vd}	Large Signal Voltage Gain (V_{out} = $2V_{pk}$-V_{pk}) R_L = 600Ω R_L = 32Ω		35 16		V/mV
I_{cc}	Supply Current no load, V_{out} = $V_{cc/2}$		1	1.5	mA
GBP	Gain Bandwith Product R_L = 600Ω		4		MHz
CMR	Common Mode Rejection Ratio	60	80		dB
SVR	Supply Voltage Rejection Ratio V_{cc} = 4.5 to 5.5V	60	80		dB
I_o	Output Short Circuit Current	50	80		mA
SR	Slew Rate	0.7	1.3		V/µs
ϕm	Phase Margin at Unit Gain R_L = 600Ω, C_L =100pF		68		Degrees
G_m	Gain Margin R_L = 600Ω, C_L =100pF		12		dB
e_n	Equivalent Input Noise Voltage f = 1kHz		9		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion V_{out} = 2Vpk-pk, F = 1kHz, A_v = 1, R_L =600Ω		0.005		%

MACROMODELS

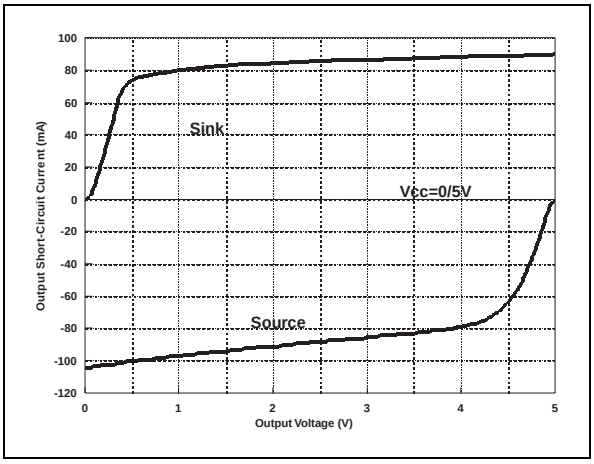
```
** Standard Linear Ics Macromodels, 1996.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT TS921 1 3 2 4 5 (analog)
************************************************************
.MODEL MDTH D IS=1E-8 KF=2.664234E-16 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 8.125000E+00
RIN 15 16 8.125000E+00
RIS 11 15 2.238465E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 153.5u
VOFN 13 14 DC 0
IPOL 13 5 3.200000E-05
CPS 11 15 1e-9
DINN 17 13 MDTH 400E-12
VIN 17 5 -0.100000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 0.400000E+00
FCP 4 5 VOFP 1.865000E+02
FCN 5 4 VOFN 1.865000E+02
FIBP 2 5 VOFP 6.250000E-03
FIBN 5 1 VOFN 6.250000E-03
* GM1 STAGE ***************
FGM1P 119 5 VOFP 1.1
FGM1N 119 5 VOFN 1.1
RAP 119 4 2.6E+06
RAN 119 5 2.6E+06
* GM2 STAGE ***************
G2P 19 5 119 5 1.92E-02
G2N 19 5 119 4 1.92E-02
R2P 19 4 1E+07
R2N 19 5 1E+07
**************************
VINT1 500 0 5
GCONVP 500 501 119 4 19.38 !envoie ds VP,
I(VP)=(V119-V4)/2/Ut VP 501 0 0
GCONVN 500 502 119 5 19.38 !envoie ds VN,
I(VN)=(V119-V5)/2/Ut VN 502 0 0
********* orientation isink isource *******
VINT2 503 0 5
FCOPY 503 504 VOUT 1
DCOPYP 504 505 MDTH 400E-9
VCOPYP 505 0 0
DCOPYN 506 504 MDTH 400E-9
VCOPYN 0 506 0
**************************
F2PP 19 5 poly(2) VCOPYP VP 0 0 0 0 0.5 !multiplie
I(vout)*I(VP)=Iout*(V119-V4)/2/Ut
F2PN 19 5 poly(2) VCOPYP VN 0 0 0 0 0.5 !multiplie
I(vout)*I(VN)=Iout*(V119-V5)/2/Ut
F2NP 19 5 poly(2) VCOPYN VP 0 0 0 0 1.75 !multiplie
I(vout)*I(VP)=Iout*(V119-V4)/2/Ut
F2NN 19 5 poly(2) VCOPYN VN 0 0 0 0 1.75 !multiplie
I(vout)*I(VN)=Iout*(V119-V5)/2/Ut
* COMPENSATION ************
CC 19 119 25p
* OUTPUT***********
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 6.250000E+02
VIPM 28 4 5.000000E+01
HONM 21 27 VOUT 6.250000E+02
VINM 5 27 5.000000E+01
VOUT 3 23 0
ROUT 23 19 6
COUT 3 5 1.300000E-10
DOP 19 25 MDTH 400E-12
VOP 4 25 1.052
DON 24 19 MDTH 400E-12
VON 24 5 1.052
.ENDS
```

ELECTRICAL CHARACTERISTICS

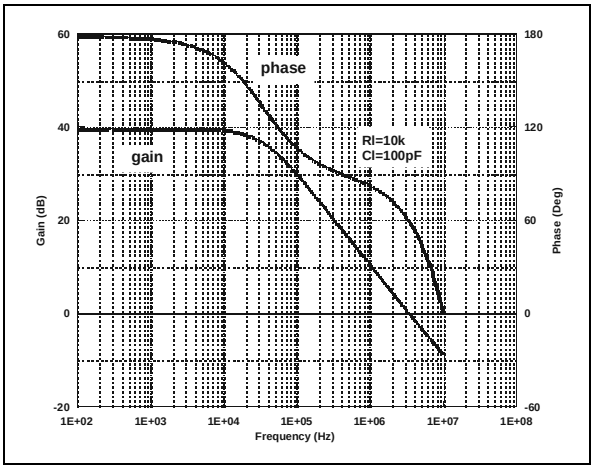
V_{CC}^+ = 3V, V_{CC}- = 0V, R_L, C_L connected to $V_{CC/2}$, T_{amb} = 25°C (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 10kΩ	200	V/mV
I_{CC}	No load, per operator	1.2	mA
V_{icm}		-0.2 to 3.2	V
V_{OH}	R_L = 10kΩ	2.95	V
V_{OL}	R_L = 10kΩ	25	mV
I_{sink}	V_O = 3V	80	mA
I_{source}	V_O = 0V	80	mA
GBP	R_L = 600kΩ	4	MHz
SR	R_L = 10kΩ, C_L = 100pF	1.3	V/µs
ϕm	R_L = 600kΩ	68	Degrees

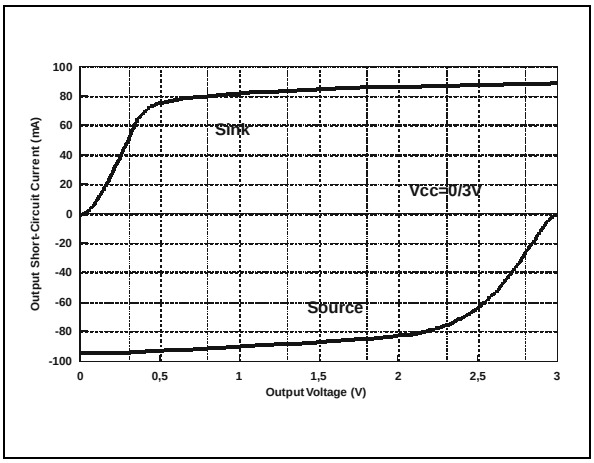
OUTPUT SHORT CIRCUIT CURRENT vs OUTPUT VOLTAGE



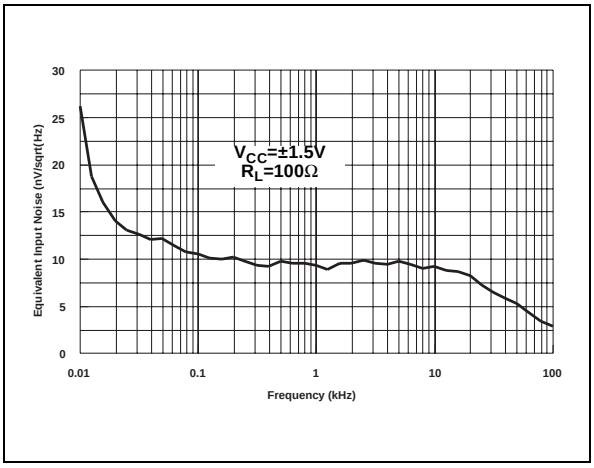
VOLTAGE GAIN AND PHASE vs FREQUENCY



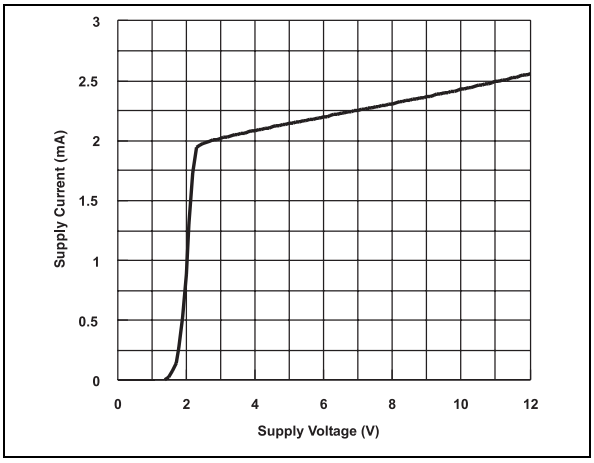
OUTPUT SHORT CIRCUIT CURRENT vs OUTPUT VOLTAGE



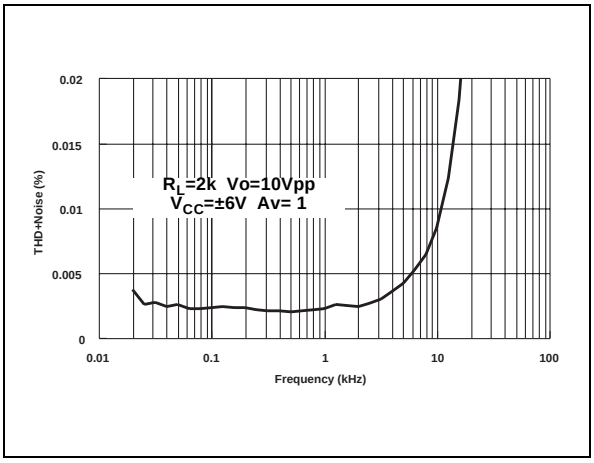
EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY



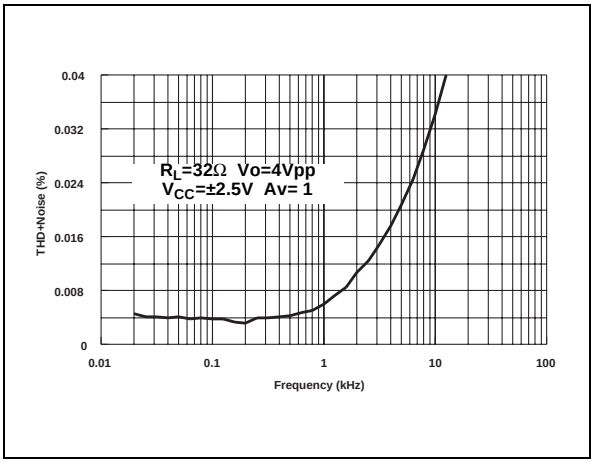
OUTPUT SUPPLY CURRENT vs SUPPLY VOLTAGE



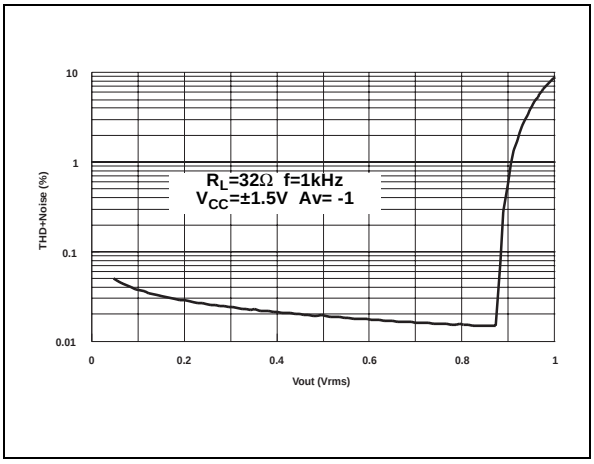
THD + NOISE vs FREQUENCY



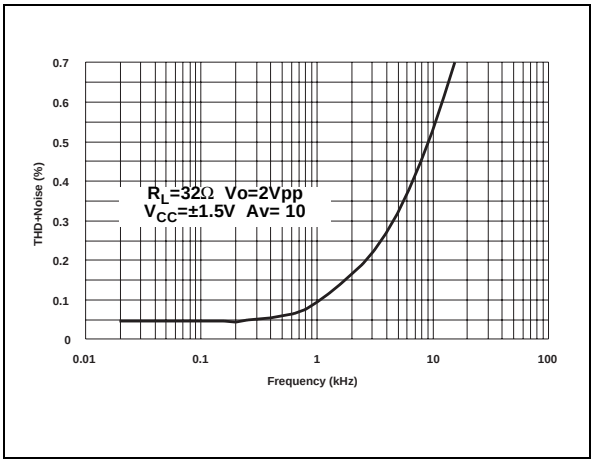
THD + NOISE vs FREQUENCY



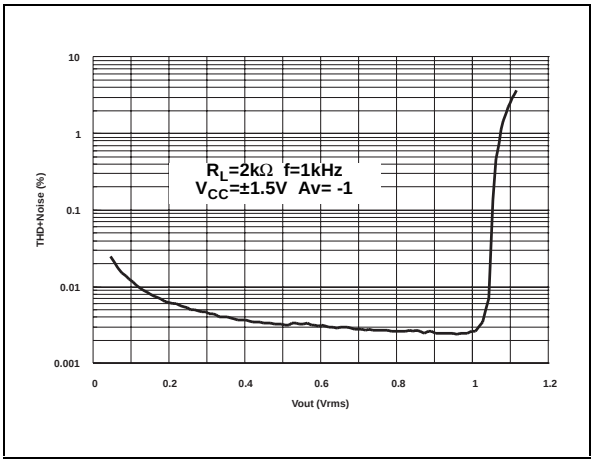
THD + NOISE vs OUTPUT VOLTAGE



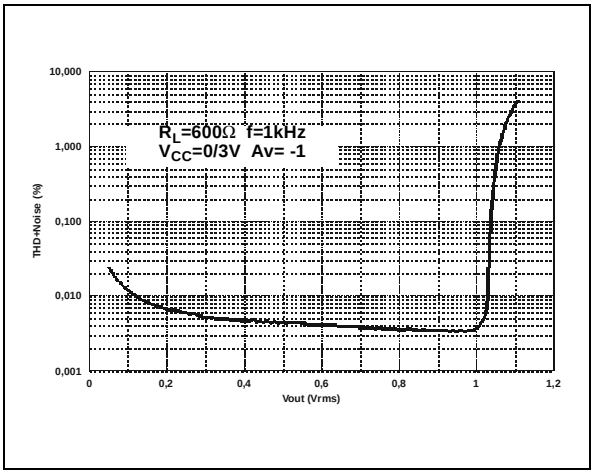
THD + NOISE vs FREQUENCY



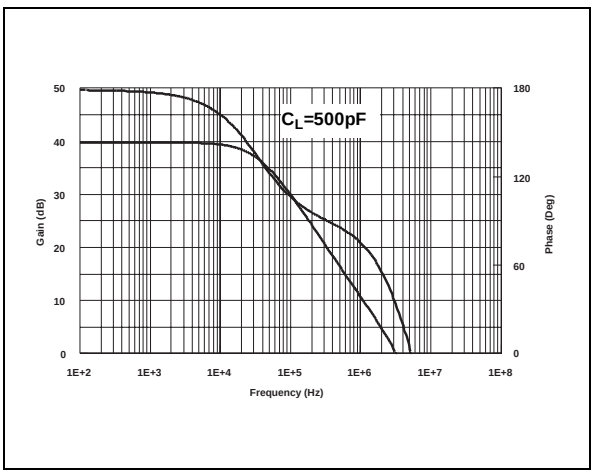
THD + NOISE vs OUTPUT VOLTAGE



THD + NOISE vs OUTPUT VOLTAGE

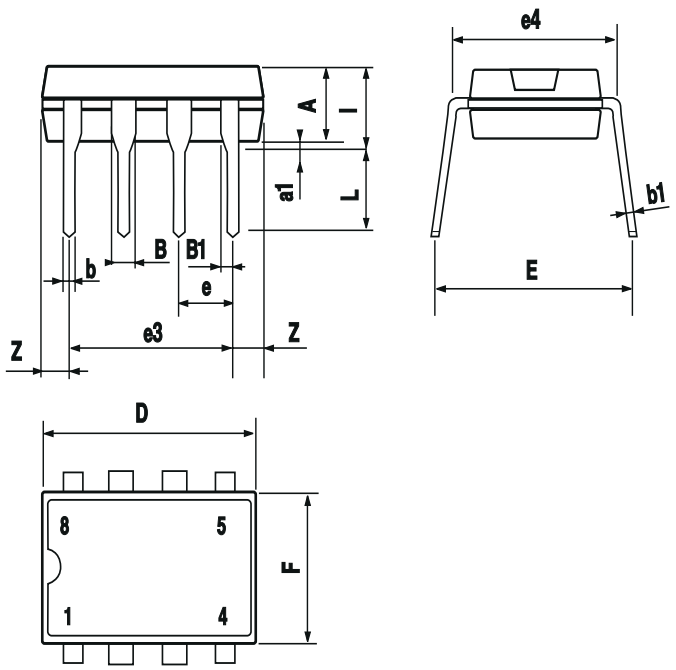


OPEN LOOP GAIN AND PHASE vs FREQUENCY



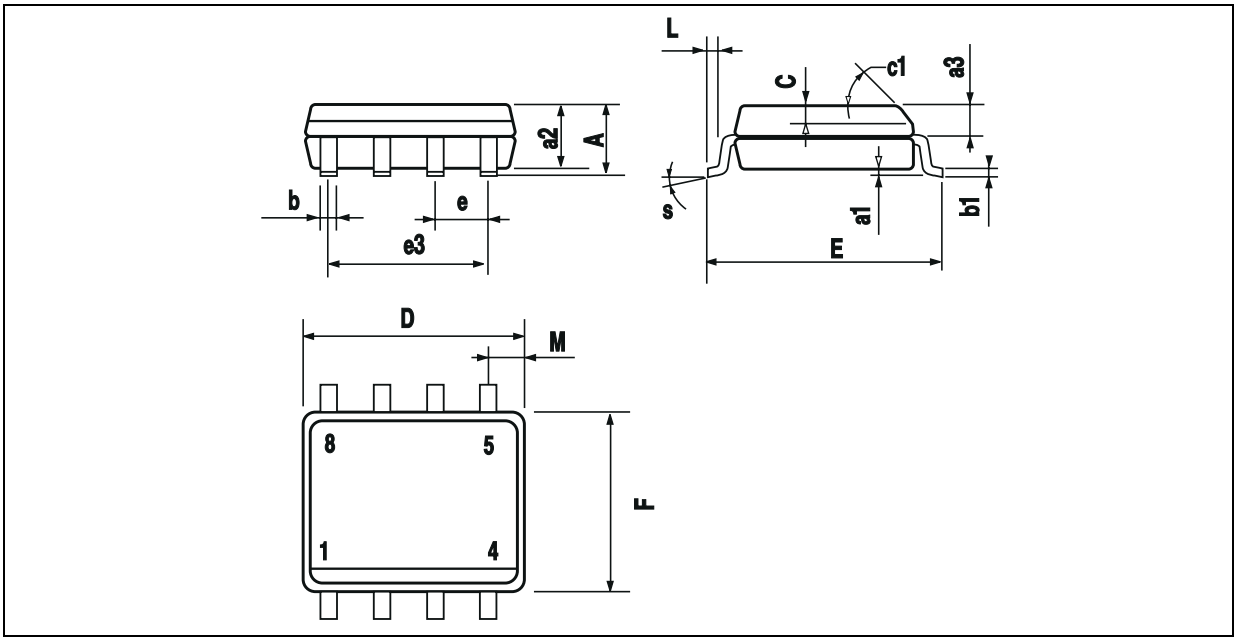
PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

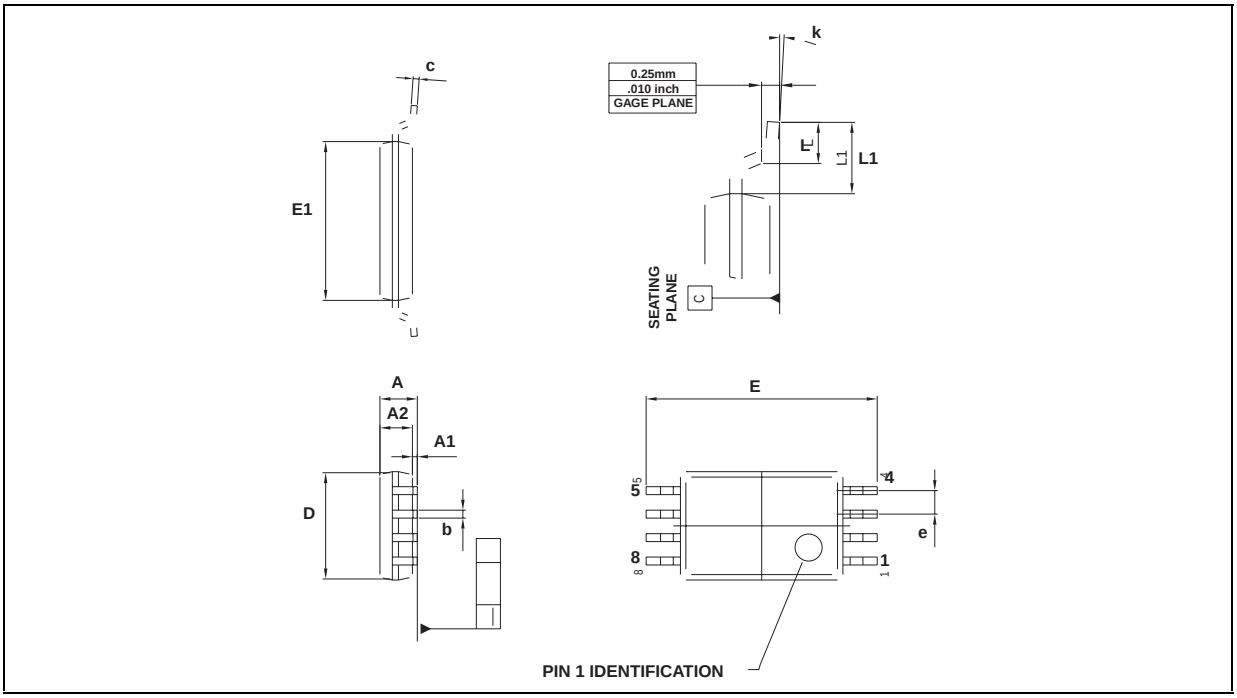
PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

PACKAGE MECHANICAL DATA

8 PINS - THIN SHRINK SMALL OUTLINE PACKAGE



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.05
A1	0.05		0.15	0.01		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.15
c	0.09		0.20	0.003		0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E		6.40			0.252	
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.025	
k	0°		8°	0°		8°
l	0.50	0.60	0.75	0.09	0.0236	0.030
L	0.45	0.600	0.75	0.018	0.024	0.030
L1		1.000			0.039	

MC34071,2,4,A
MC33071,2,4,A

Single Supply 3.0 V to 44 V Operational Amplifiers

Quality bipolar fabrication with innovative design concepts are employed for the MC33071/72/74, MC34071/72/74 series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33071/72/74, MC34071/72/74 series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic DIP, SOIC and TSSOP surface mount packages.

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.1%
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground (V_{EE})
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection
- ESD Diodes/Clamps Provide Input Protection for Dual and Quad
- Pb−Free Package May be Available. The G−Suffix Denotes a Pb−Free Lead Finish

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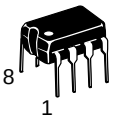
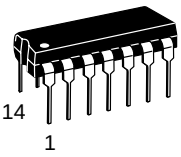
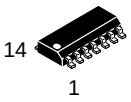


PDIP−8
P SUFFIX
CASE 626

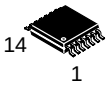
SO−8
D SUFFIX
CASE 751



PDIP−14
P SUFFIX
CASE 646



SO−14
D SUFFIX
CASE 751A



TSSOP−14
DTB SUFFIX
CASE 948G

ORDERING INFORMATION

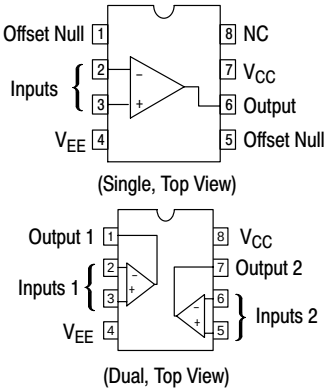
See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

DEVICE MARKING INFORMATION

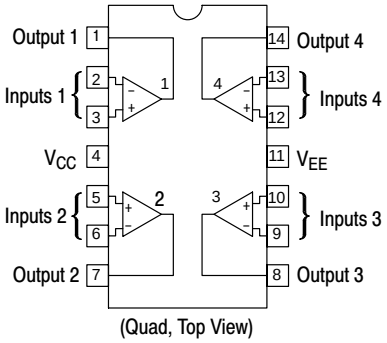
See general marking information in the device marking section on page 18 of this data sheet.

PIN CONNECTIONS

CASE 626/CASE 751



CASE 646/CASE 751A/CASE 948G



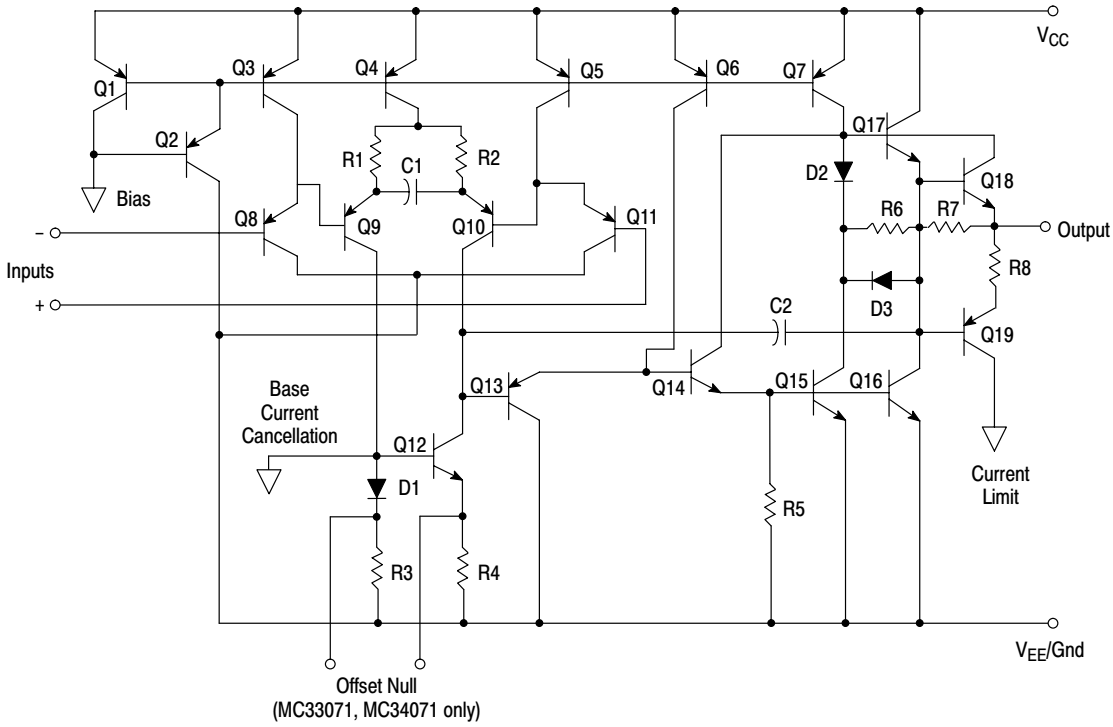


Figure 1. Representative Schematic Diagram
(Each Amplifier)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{EE} to V_{CC})	V_S	+44	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C

1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground, unless otherwise noted. See Note 3 for $T_A = T_{low}$ to T_{high})

Characteristics	Symbol	A Suffix			Non−Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V) V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, $T_A = T_{low}$ to T_{high}	V_{IO}	– – –	0.5 0.5 –	3.0 3.0 5.0	– – –	1.0 1.5 –	5.0 5.0 7.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, $T_A = T_{low}$ to T_{high}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IB}	– –	100 –	500 700	– –	100 –	500 700	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0V) T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IO}	– –	6.0 –	50 300	– –	6.0 –	75 300	nA
Input Common Mode Voltage Range T_A = +25°C $T_A = T_{low}$ to T_{high}	V_{ICR}	V_{EE} to (V_{CC} −1.8) V_{EE} to (V_{CC} −2.2)			V_{EE} to (V_{CC} −1.8) V_{EE} to (V_{CC} −2.2)			V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) T_A = +25°C $T_A = T_{low}$ to T_{high}	A_{VOL}	50 25	100 –	– –	25 20	100 –	– –	V/mV
Output Voltage Swing (V_{ID} = ±1.0 V) V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, $T_A = T_{low}$ to T_{high}	V_{OH}	3.7 13.6 13.4	4.0 14 –	– – –	3.7 13.6 13.4	4.0 14 –	– – –	V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, $T_A = T_{low}$ to T_{high}	V_{OL}	– – –	0.1 −14.7 –	0.3 −14.3 −13.5	– – –	0.1 −14.7 –	0.3 −14.3 −13.5	V
Output Short Circuit Current (V_{ID} = 1.0 V, V_O = 0 V, T_A = 25°C) Source Sink	I_{SC}	10 20	30 30	– –	10 20	30 30	– –	mA
Common Mode Rejection $R_S \le$ 10 kΩ, $V_{CM} = V_{ICR}$, T_A = 25°C	CMR	80	97	–	70	97	–	dB
Power Supply Rejection (R_S = 100 Ω) V_{CC}/V_{EE} = +16.5 V/−16.5 V to +13.5 V/−13.5 V, T_A = 25°C	PSR	80	97	–	70	97	–	dB
Power Supply Current (Per Amplifier, No Load) V_{CC} = +5.0 V, V_{EE} = 0 V, V_O = +2.5 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, $T_A = T_{low}$ to T_{high}	I_D	– – –	1.6 1.9 –	2.0 2.5 2.8	– – –	1.6 1.9 –	2.0 2.5 2.8	mA

3. T_{low} = −40°C for MC33071, 2, 4, /A
= 0°C for MC34071, 2, 4, /A
= −40°C for MC34072, 4/V
T_{high} = +85°C for MC33071, 2, 4, /A
= +70°C for MC34071, 2, 4, /A
= +125°C for MC34072, 4/V

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground. T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	A Suffix			Non−Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 500 pF) A_V = +1.0 A_V = −1.0	SR	 8.0 −	 10 13	 − −	 8.0 −	 10 13	 − −	V/μs
Setting Time (10 V Step, A_V = −1.0) To 0.1% (+1/2 LSB of 9−Bits) To 0.01% (+1/2 LSB of 12−Bits)	t_s	 − −	 1.1 2.2	 − −	 − −	 1.1 2.2	 − −	μs
Gain Bandwidth Product (f = 100 kHz)	GBW	3.5	4.5	−	3.5	4.5	−	MHz
Power Bandwidth A_V = +1.0, R_L = 2.0 kΩ, V_O = 20 V_{pp}, THD = 5.0%	BW	−	160	−	−	160	−	kHz
Phase margin R_L = 2.0 kΩ R_L = 2.0 kΩ, C_L = 300 pF	f_m	 − −	 60 40	 − −	 − −	 60 40	 − −	Deg
Gain Margin R_L = 2.0 kΩ R_L = 2.0 kΩ, C_L = 300 pF	A_m	 − −	 12 4.0	 − −	 − −	 12 4.0	 − −	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	−	32	−	−	32	−	nV/$\sqrt{Hz}$
Equivalent Input Noise Current f = 1.0 kHz	i_n	−	0.22	−	−	0.22	−	pA/$\sqrt{Hz}$
Differential Input Resistance V_{CM} = 0 V	R_{in}	−	150	−	−	150	−	MΩ
Differential Input Capacitance V_{CM} = 0 V	C_{in}	−	2.5	−	−	2.5	−	pF
Total Harmonic Distortion A_V = +10, R_L = 2.0 kΩ, 2.0 $V_{pp} \le V_O \le$ 20 V_{pp}, f = 10 kHz	THD	−	0.02	−	−	0.02	−	%
Channel Separation (f = 10 kHz)	−	−	120	−	−	120	−	dB
Open Loop Output Impedance (f = 1.0 MHz)	$\|Z_O\|$	−	30	−	−	30	−	W

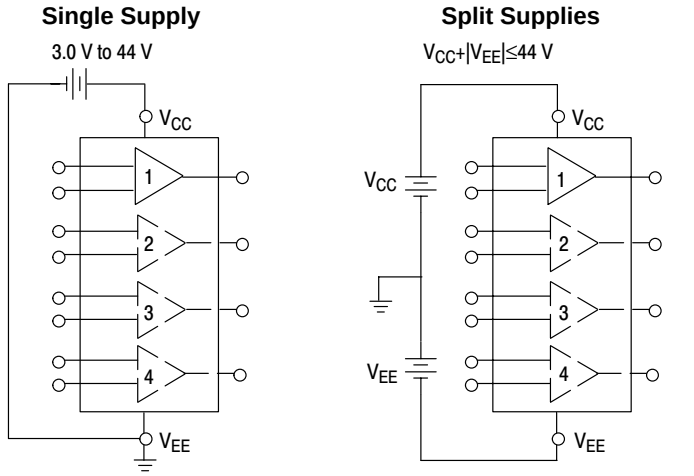
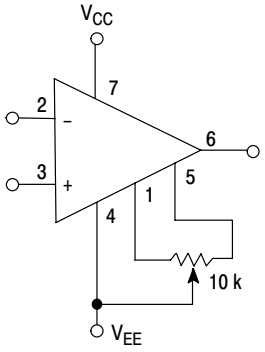


Figure 2. Power Supply Configurations



Offset nulling range is approximately ±80 mV with a 10 k potentiometer (MC33071, MC34071 only).

Figure 3. Offset Null Circuit

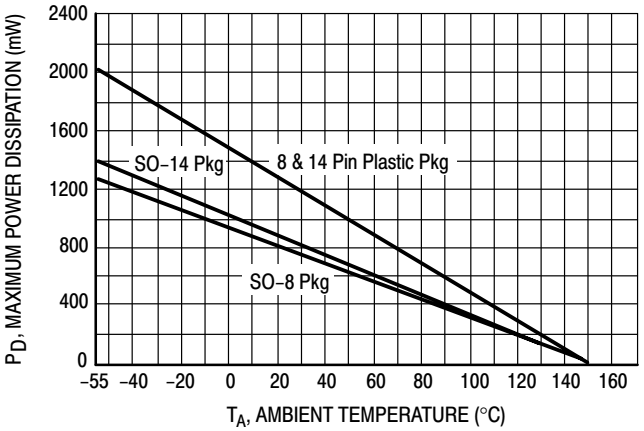


Figure 4. Maximum Power Dissipation versus Temperature for Package Types

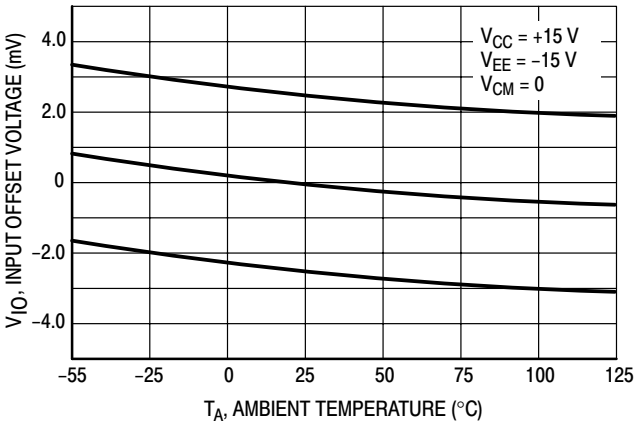


Figure 5. Input Offset Voltage versus Temperature for Representative Units

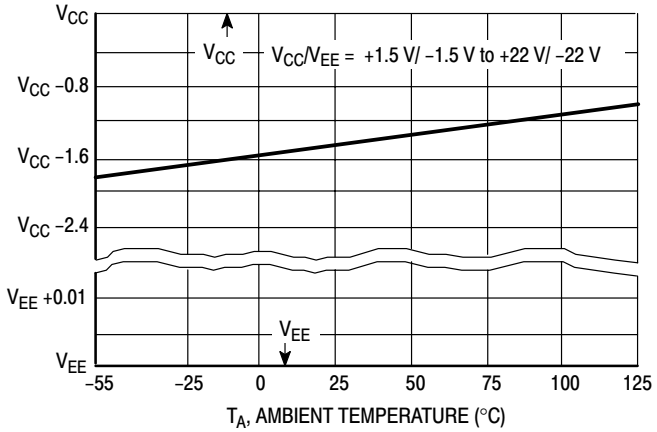


Figure 6. Input Common Mode Voltage Range versus Temperature

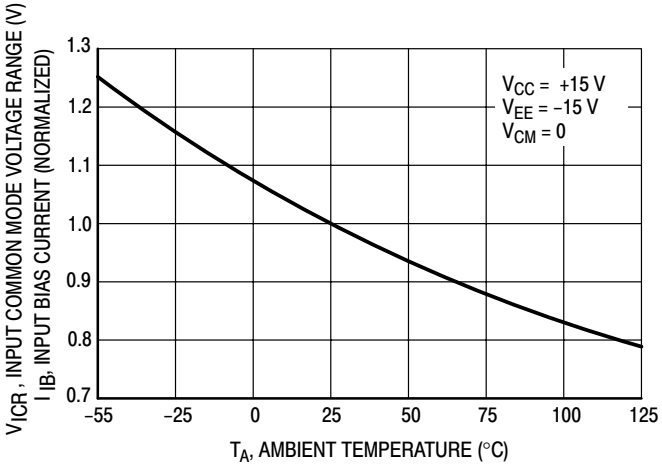


Figure 7. Normalized Input Bias Current versus Temperature

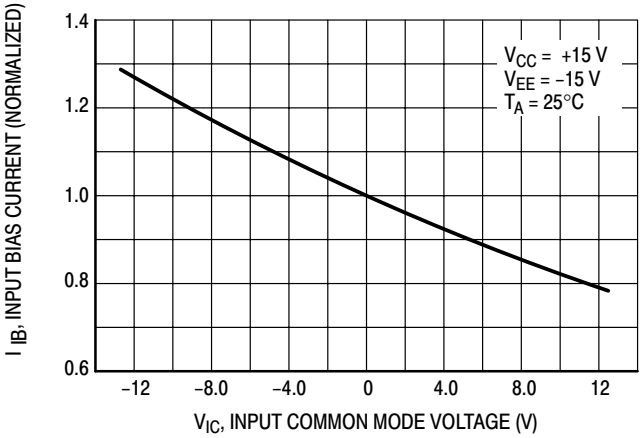


Figure 8. Normalized Input Bias Current versus Input Common Mode Voltage

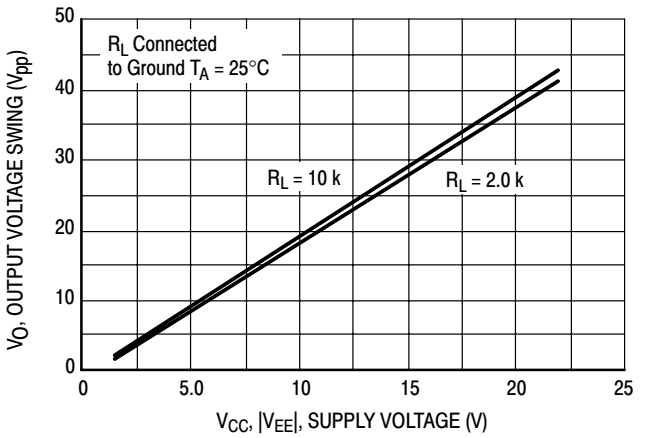


Figure 9. Split Supply Output Voltage Swing versus Supply Voltage

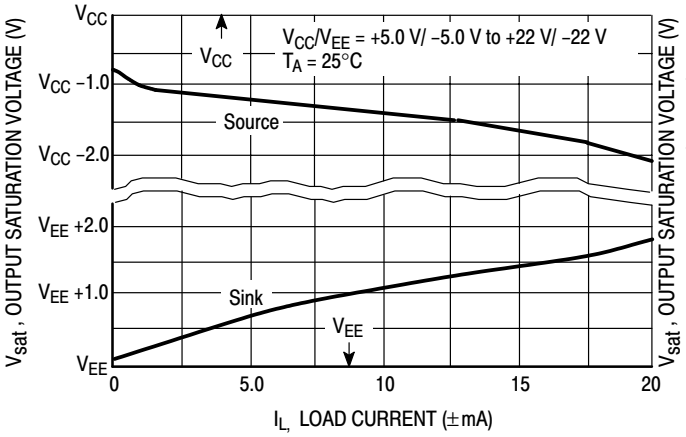


Figure 10. Single Supply Output Saturation versus Load Resistance to V_{CC}

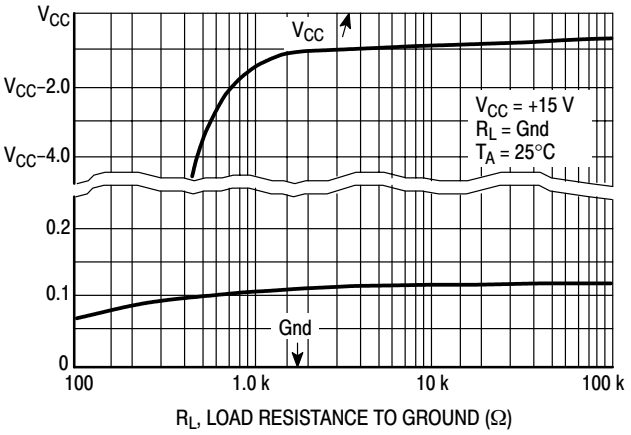


Figure 11. Split Supply Output Saturation versus Load Current

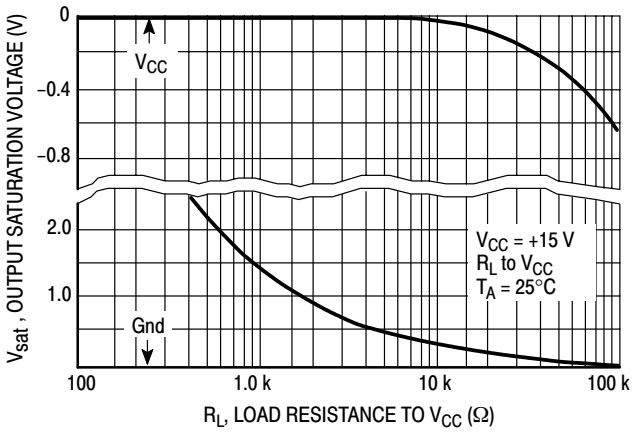


Figure 12. Single Supply Output Saturation versus Load Resistance to Ground

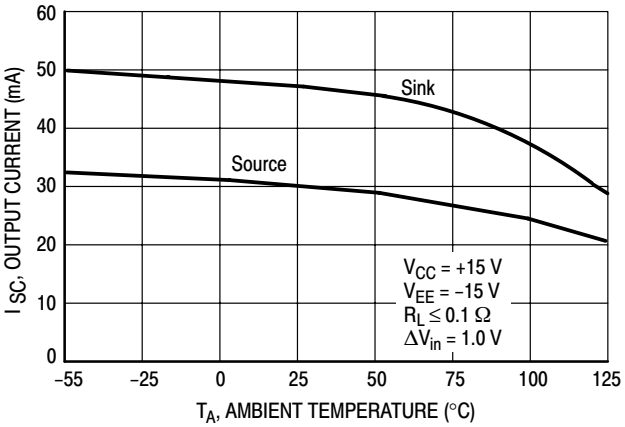


Figure 13. Output Short Circuit Current versus Temperature

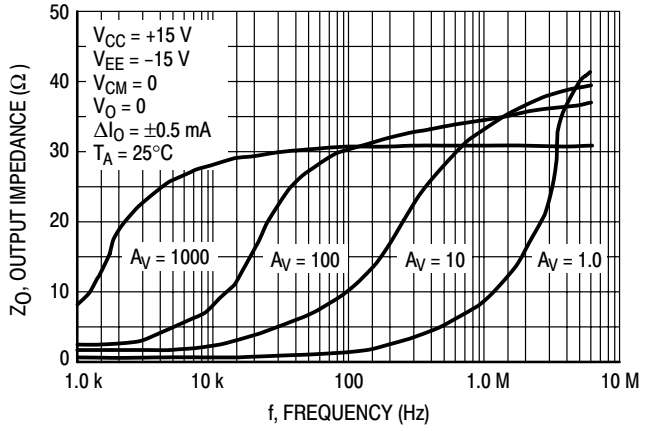


Figure 14. Output Impedance versus Frequency

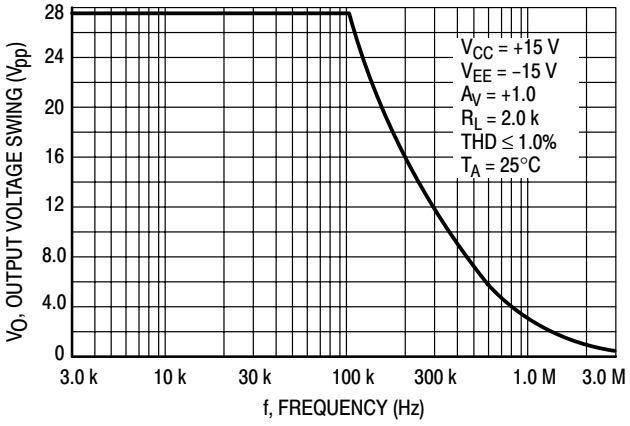


Figure 15. Output Voltage Swing versus Frequency

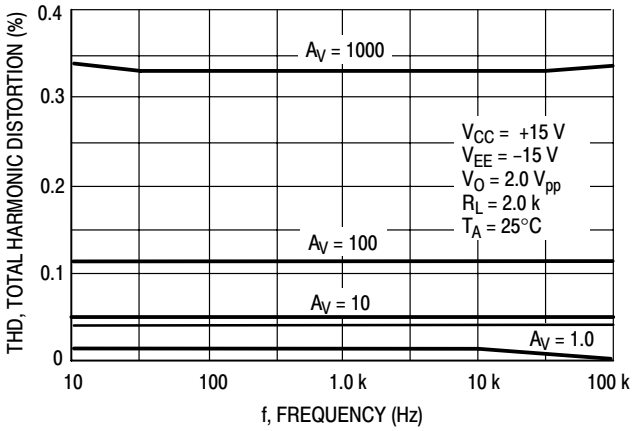


Figure 16. Total Harmonic Distortion versus Frequency

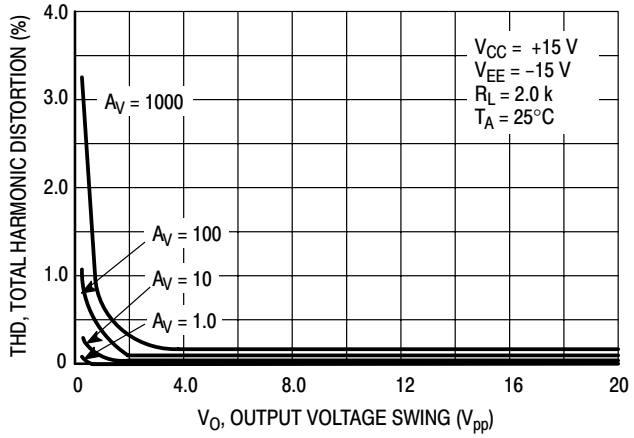


Figure 17. Total Harmonic Distortion versus Output Voltage Swing

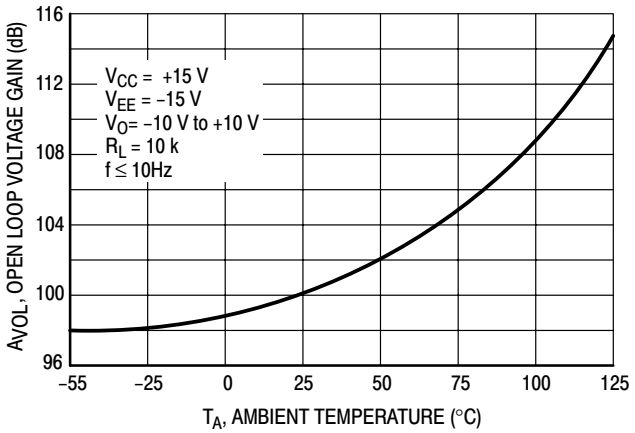


Figure 18. Open Loop Voltage Gain versus Temperature

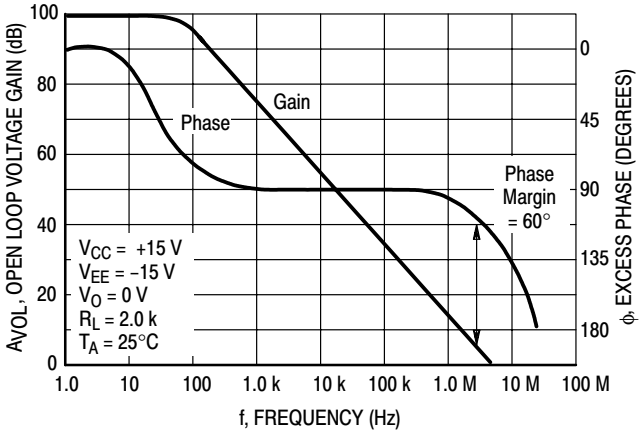


Figure 19. Open Loop Voltage Gain and Phase versus Frequency

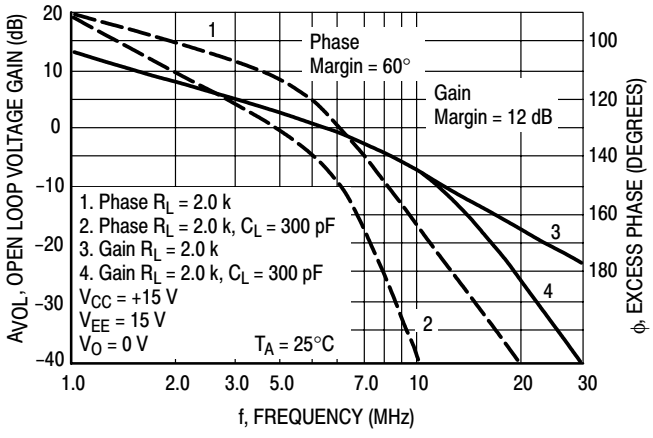


Figure 20. Open Loop Voltage Gain and Phase versus Frequency

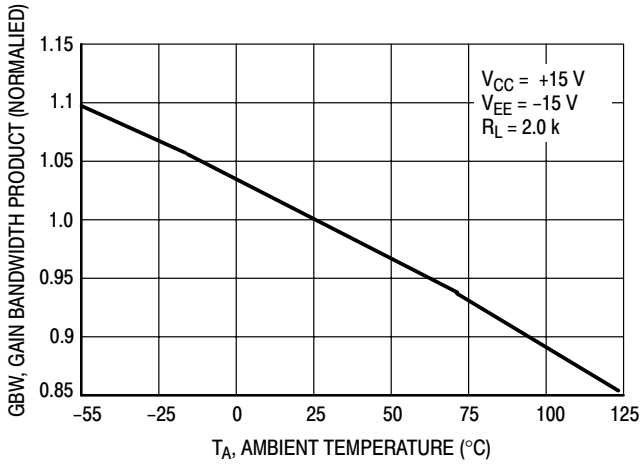


Figure 21. Normalized Gain Bandwidth Product versus Temperature

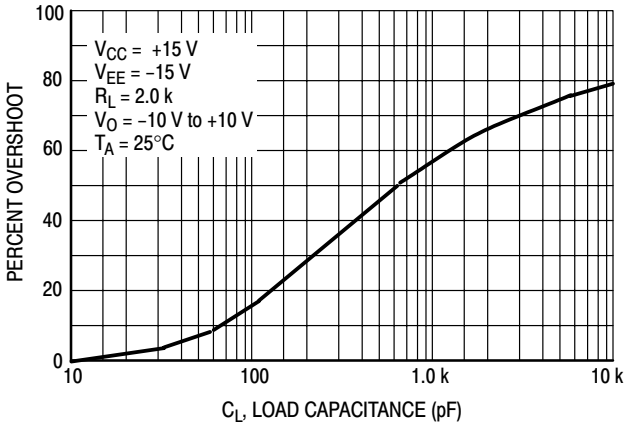


Figure 22. Percent Overshoot versus Load Capacitance

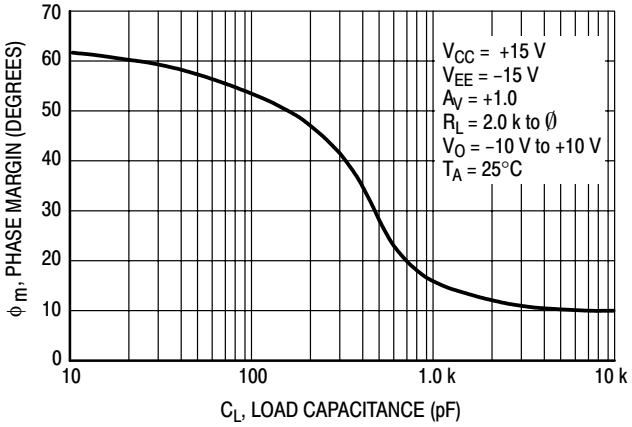


Figure 23. Phase Margin versus Load Capacitance

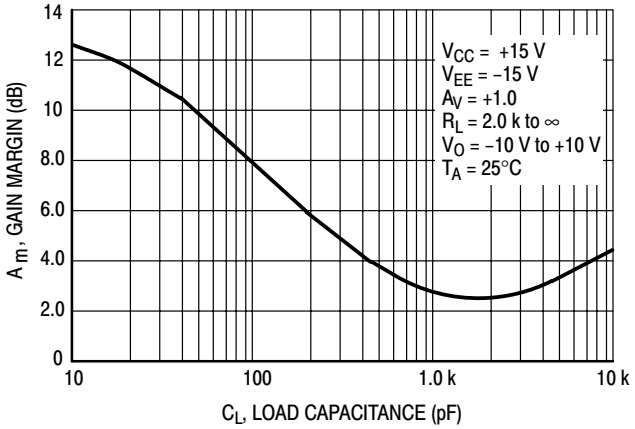


Figure 24. Gain Margin versus Load Capacitance

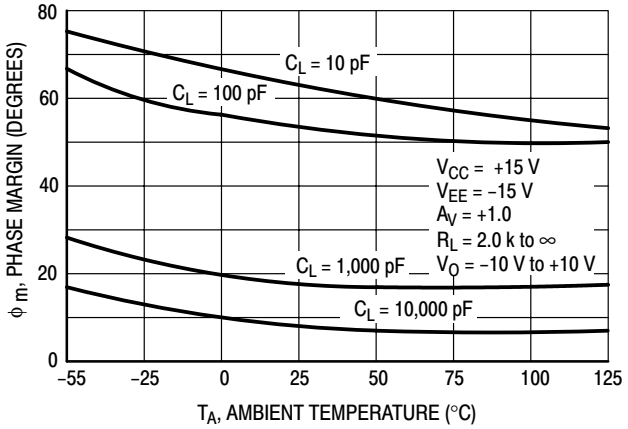


Figure 25. Phase Margin versus Temperature

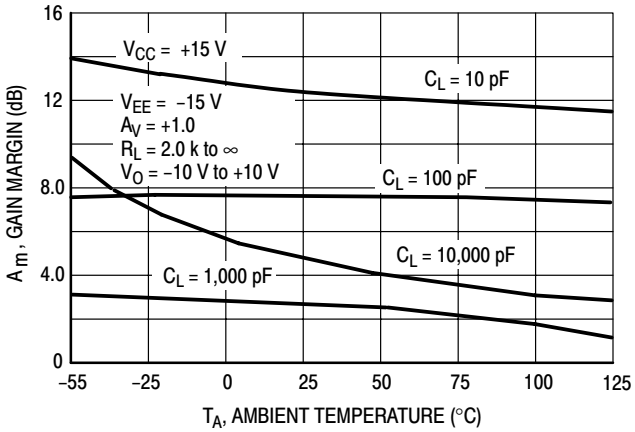


Figure 26. Gain Margin versus Temperature

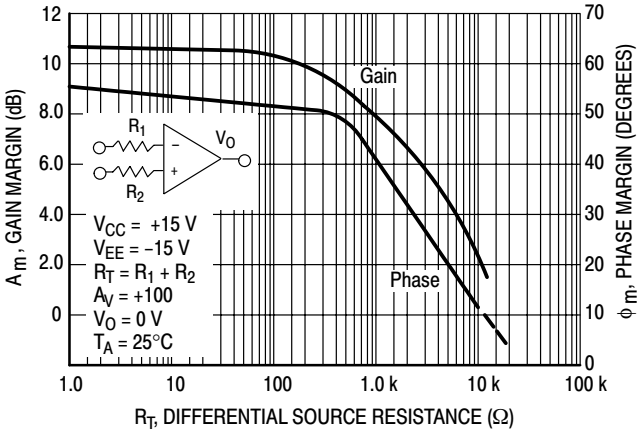


Figure 27. Phase Margin and Gain Margin versus Differential Source Resistance

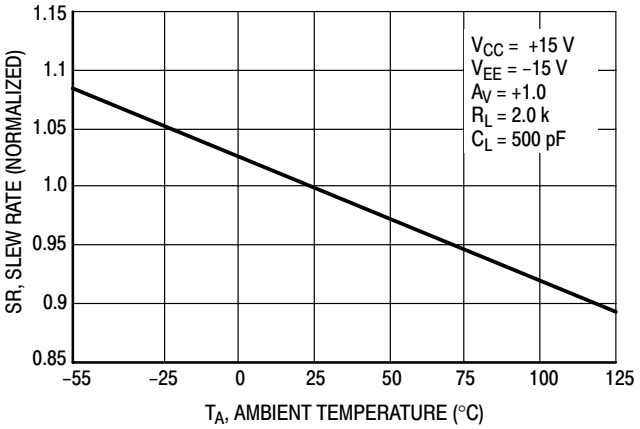


Figure 28. Normalized Slew Rate versus Temperature

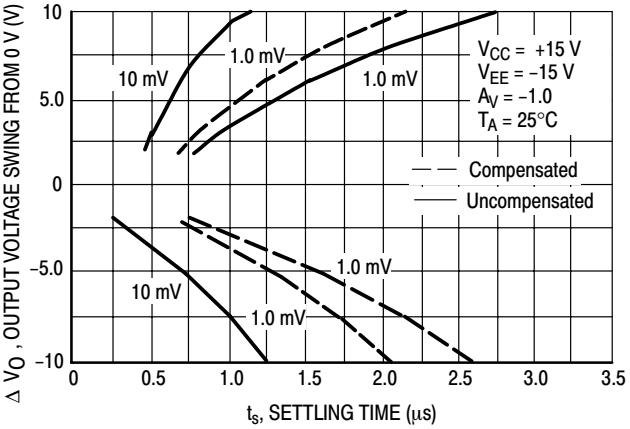


Figure 29. Output Settling Time

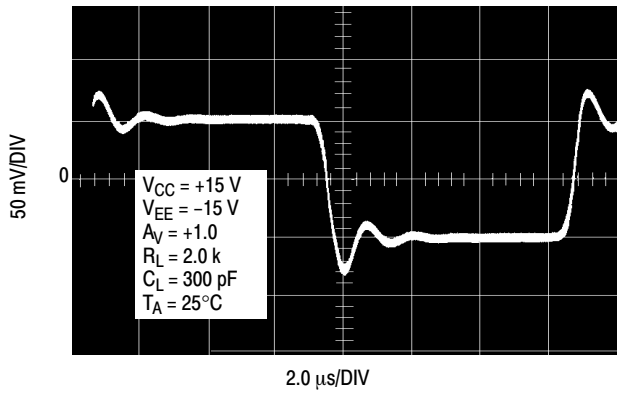


Figure 30. Small Signal Transient Response

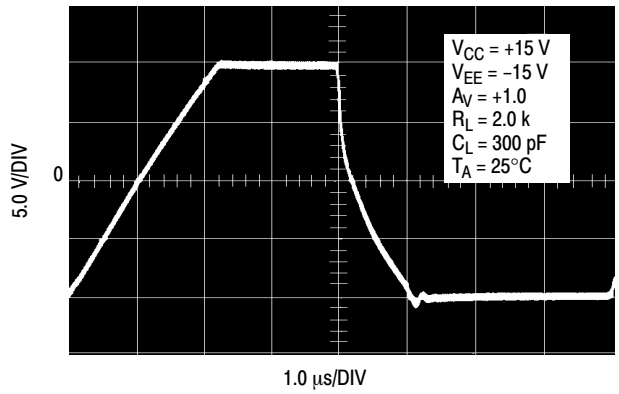


Figure 31. Large Signal Transient Response

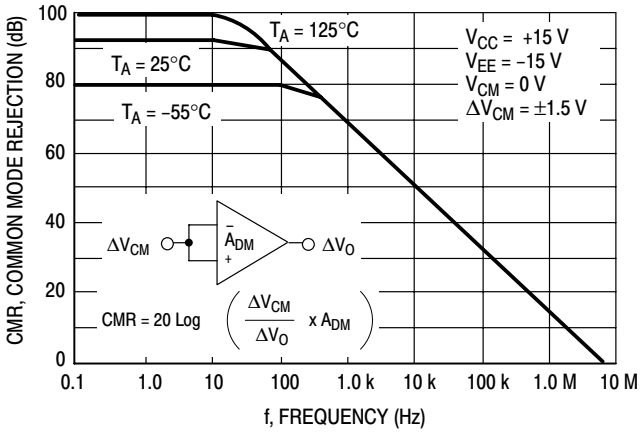


Figure 32. Common Mode Rejection versus Frequency

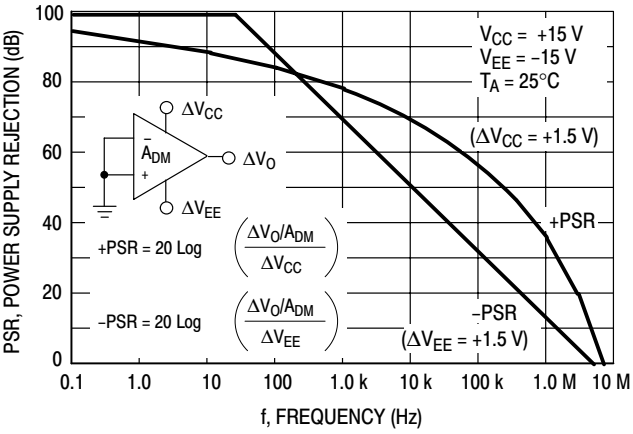


Figure 33. Power Supply Rejection versus Frequency

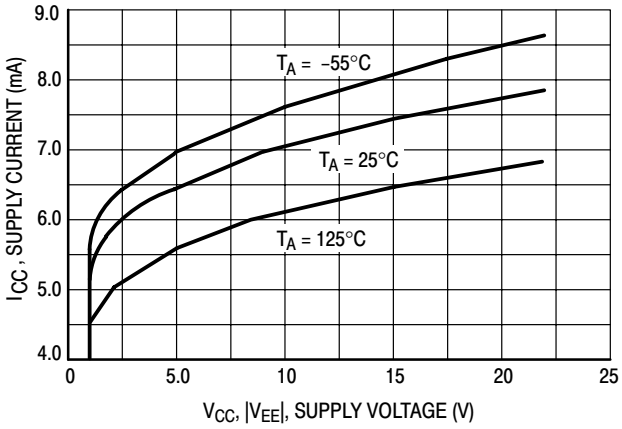


Figure 34. Supply Current versus Supply Voltage

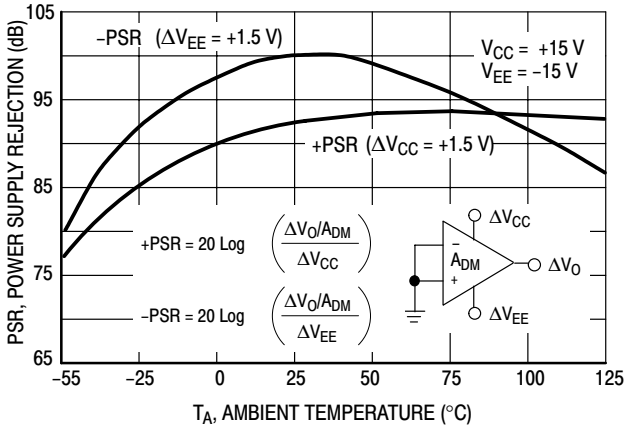


Figure 35. Power Supply Rejection versus Temperature

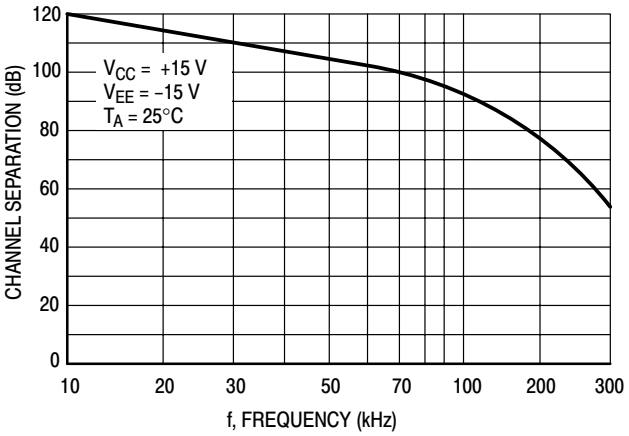


Figure 36. Channel Separation versus Frequency

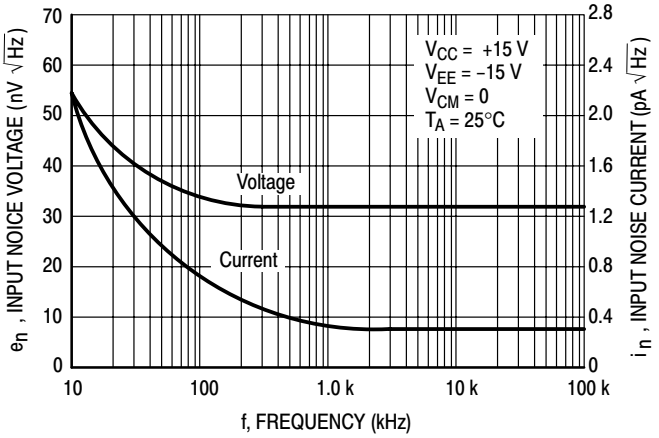


Figure 37. Input Noise versus Frequency

APPLICATIONS INFORMATION
CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{EE} and V_{CC} supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the V_{CC} voltage by approximately 3.0 V and decrease below the V_{EE} voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from V_{EE} through either inputs clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit, the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower (2.5 pF) than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D−to−A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher

values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 kΩ of feedback resistance, the MC34071 series can settle to within 1/2 LSB of 8 bits in 1.0 μs, and within 1/2 LSB of 12−bits in 2.2 μs for a 10 V step. In a inverting unity gain fast settling configuration, the symmetrical slew rate is ±13 V/μs. In the classic noninverting unity gain configuration, the output positive slew rate is +10 V/μs, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 V of the negative rail (V_{EE}), providing a 28.7 V_{pp} swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q_7, and V_{BE} of the NPN pull up transistor Q_{17}, and the voltage drop associated with the short circuit resistance, R_7. The negative swing is limited by the saturation voltage of the pull−down transistor Q_{16}, the voltage drop $I_L R_6$, and the voltage drop associated with resistance R_7, where I_L is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across R_6, thus limiting the negative swing to the saturation voltage of Q_{16}, plus the forward diode drop of D3 (≈V_{EE} +1.0 V). Thus for a given supply voltage, unprecedented peak−to−peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter−follower transistor has been eliminated, the MC34071 series offers a 20 mA minimum current sink capability, typically to an output voltage of (V_{EE} +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain bandwidth product and fast settling capability. The associated high frequency low output impedance (30 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specifications is defined at 5.0 V, these amplifiers are functional to 3.0 V @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input−output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

(Typical Single Supply Applications V_{CC} = 5.0 V)

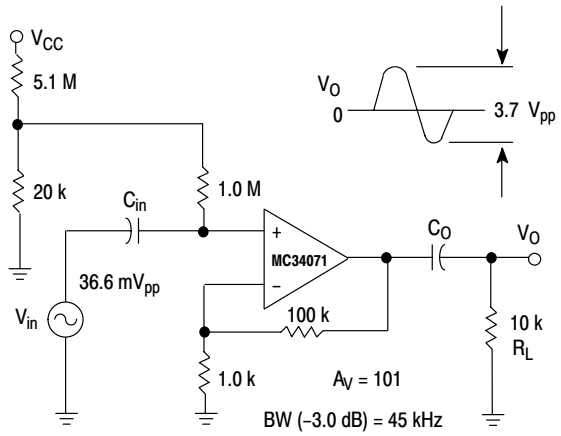


Figure 38. AC Coupled Noninverting Amplifier

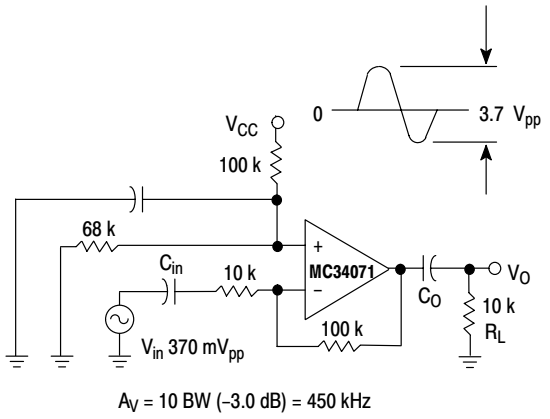


Figure 39. AC Coupled Inverting Amplifier

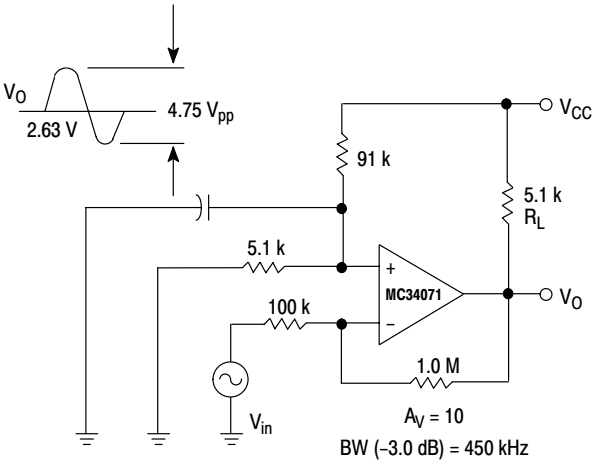


Figure 40. DC Coupled Inverting Amplifier Maximum Output Swing

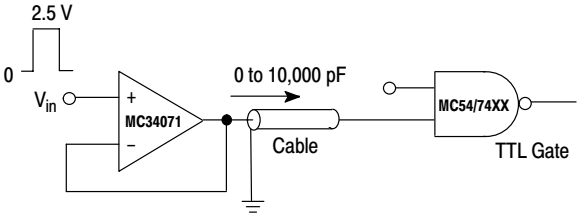


Figure 41. Unity Gain Buffer TTL Driver

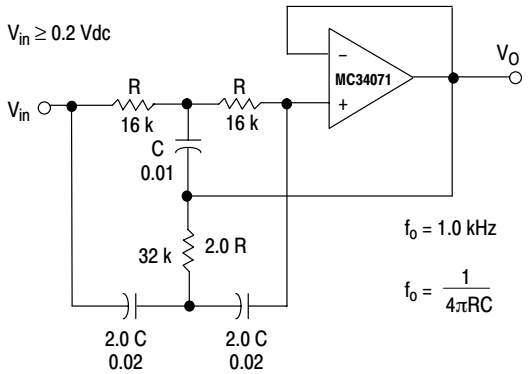
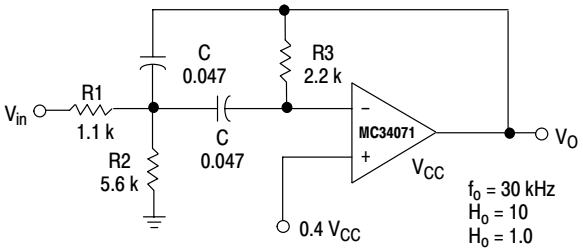


Figure 42. Active High−Q Notch Filter



Given f_o = Center Frequency
A_O = Gain at Center Frequency
Choose Value f_o, Q, A_o, C

Then:

$$R3 = \frac{Q}{\pi f_o C} \quad R1 = \frac{R3}{2H_o} \quad R2 = \frac{R1\,R3}{4Q^2R1 - R3}$$

For less than 10% error from operational amplifier $\frac{Q_o f_o}{GBW} < 0.1$

where f_o and GBW are expressed in Hz.
GBW = 4.5 MHz Typ.

Figure 43. Active Bandpass Filter

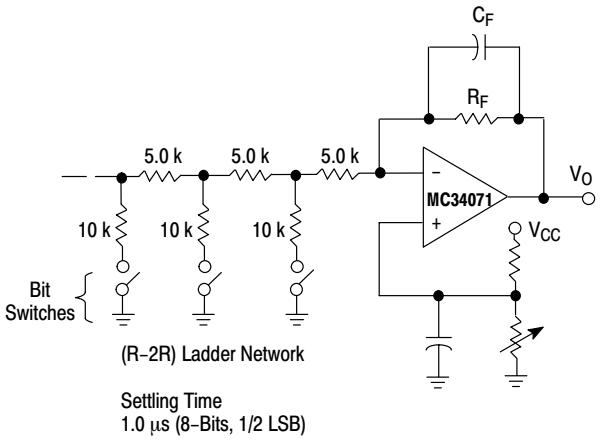


Figure 44. Low Voltage Fast D/A Converter

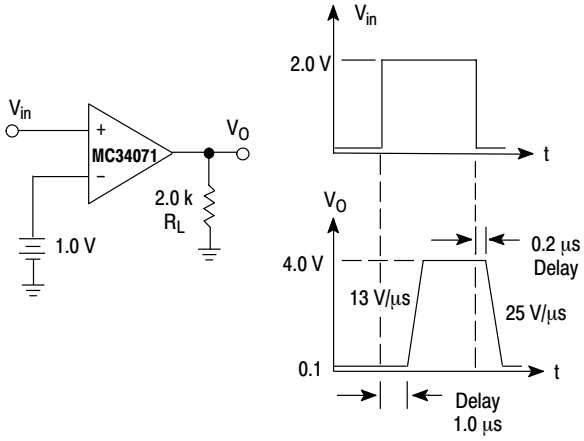


Figure 45. High Speed Low Voltage Comparator

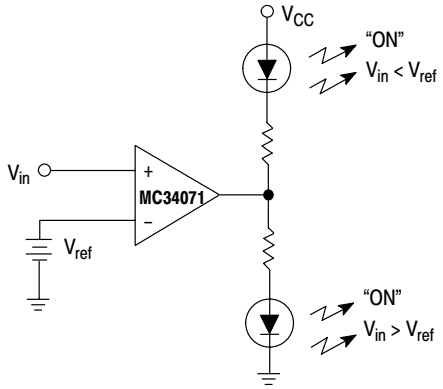


Figure 46. LED Driver

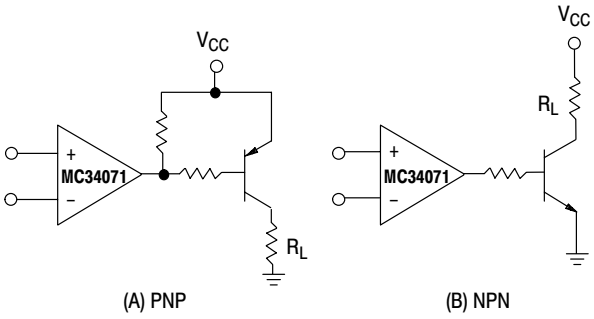


Figure 47. Transistor Driver

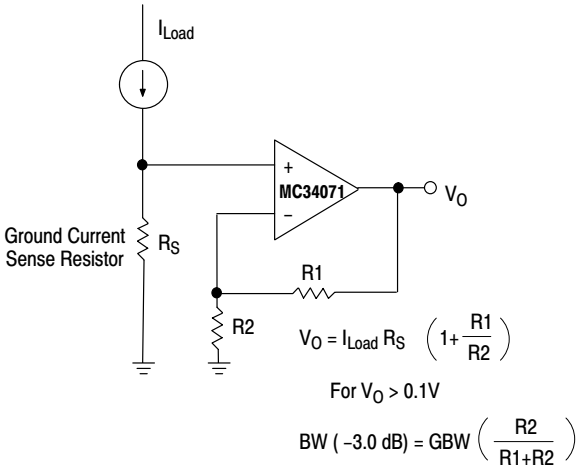


Figure 48. AC/DC Ground Current Monitor

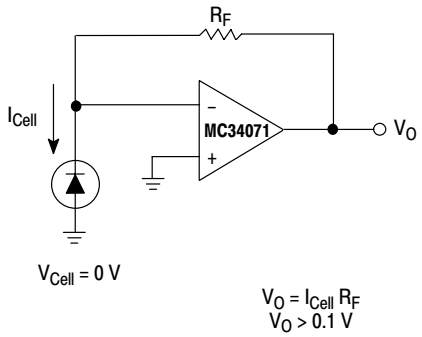


Figure 49. Photovoltaic Cell Amplifier

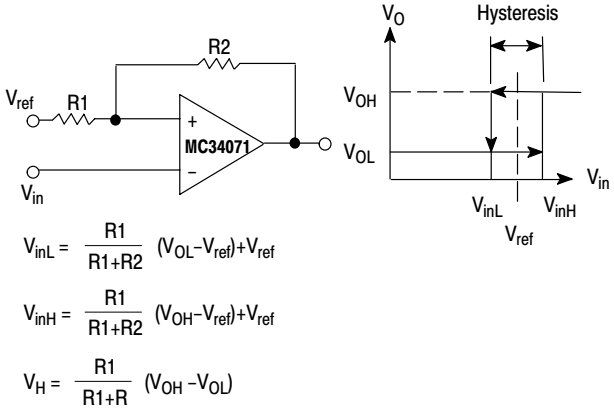


Figure 50. Low Input Voltage Comparator with Hysteresis

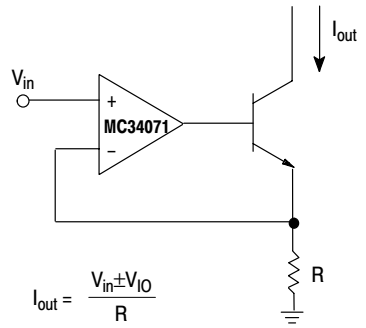


Figure 51. High Compliance Voltage to Sink Current Converter

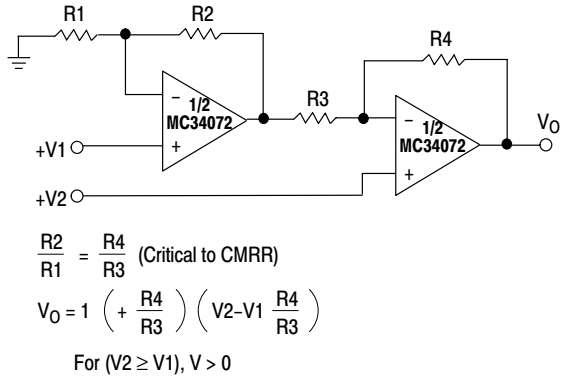


Figure 52. High Input Impedance Differential Amplifier

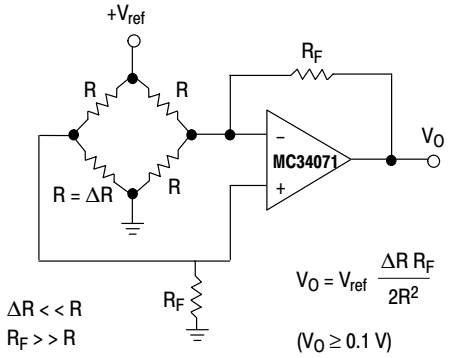


Figure 53. Bridge Current Amplifier

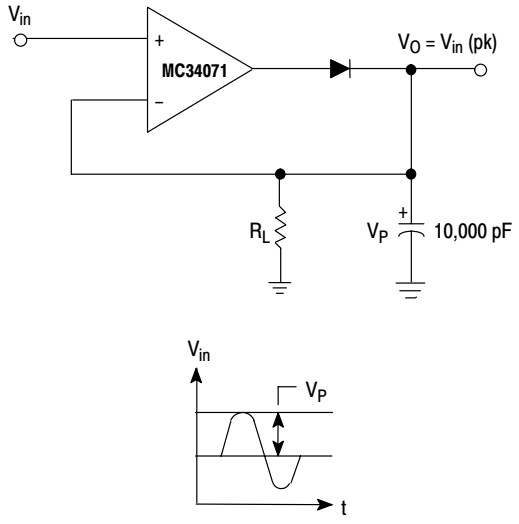


Figure 54. Low Voltage Peak Detector

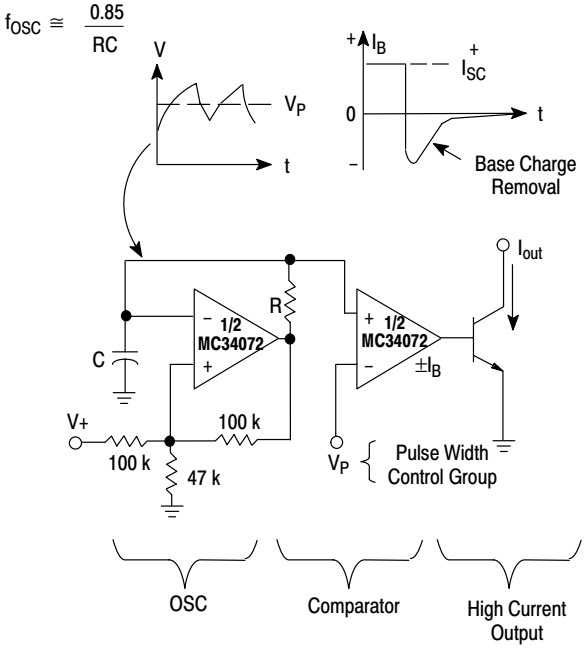


Figure 55. High Frequency Pulse Width Modulation

GENERAL ADDITIONAL APPLICATIONS INFORMATION V_S = ±15.0 V

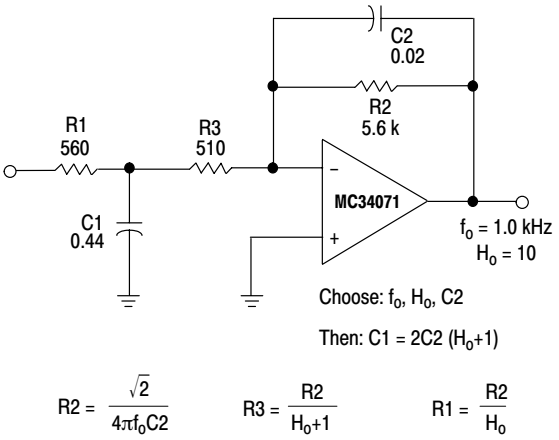


Figure 56. Second Order Low−Pass Active Filter

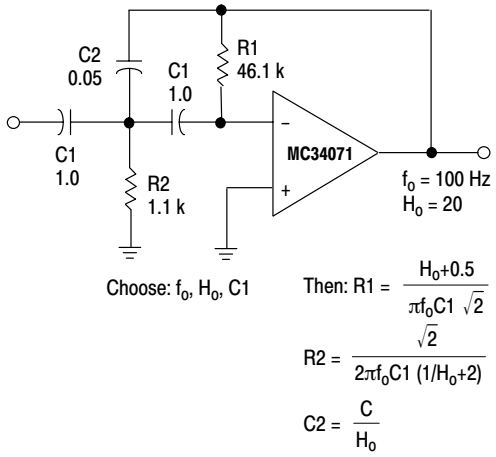


Figure 57. Second Order High−Pass Active Filter

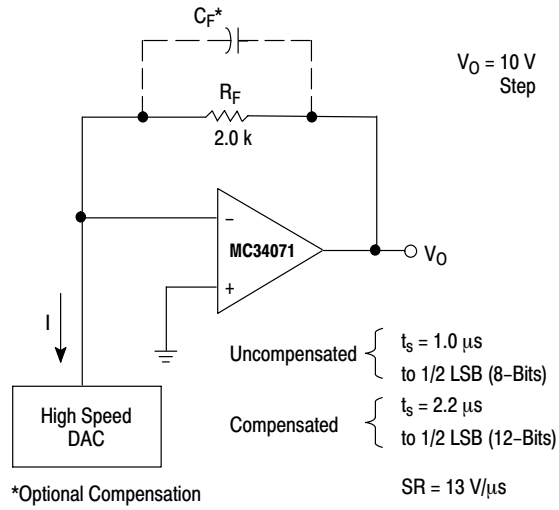


Figure 58. Fast Settling Inverter

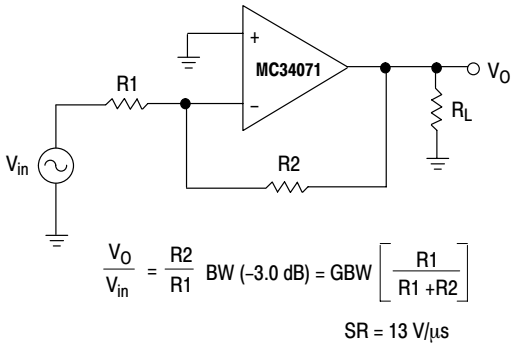


Figure 59. Basic Inverting Amplifier

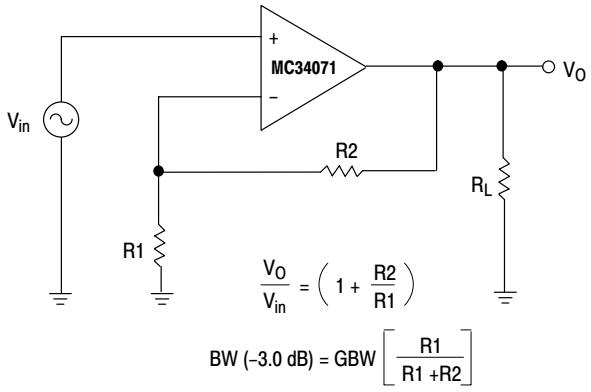


Figure 60. Basic Noninverting Amplifier

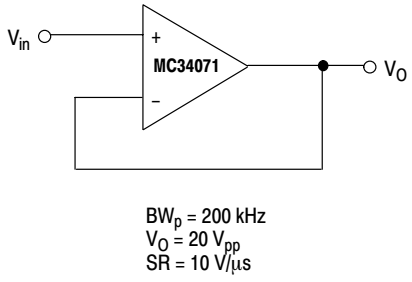


Figure 61. Unity Gain Buffer (A_V = +1.0)

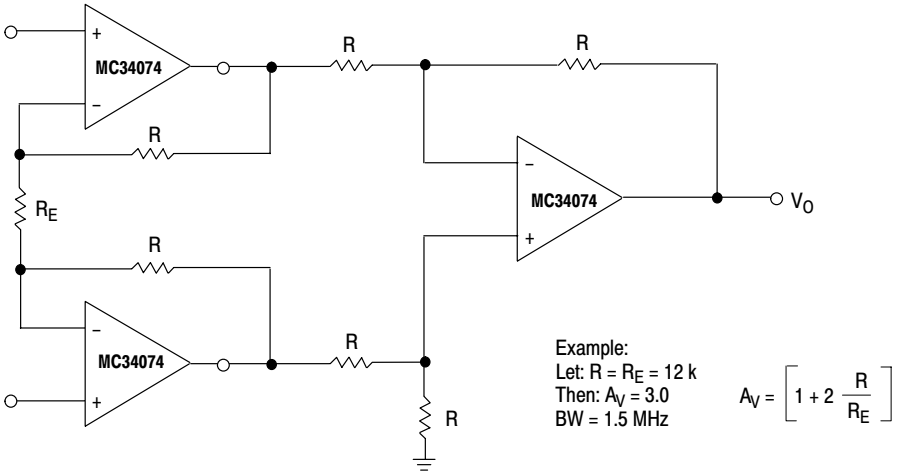
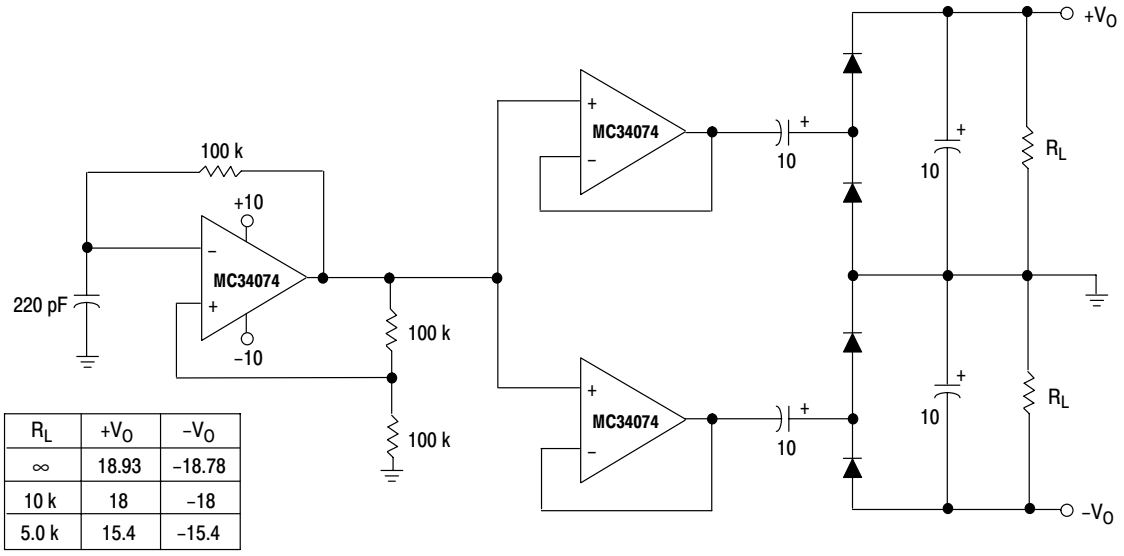


Figure 62. High Impedance Differential Amplifier



R_L	+V_O	−V_O
∞	18.93	−18.78
10 k	18	−18
5.0 k	15.4	−15.4

Figure 63. Dual Voltage Doubler

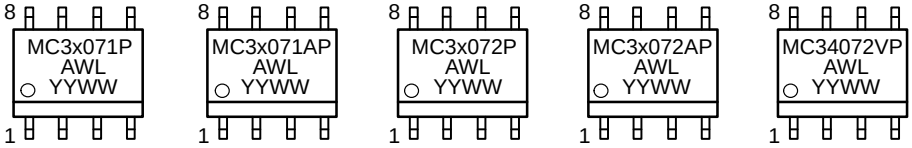
ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package	Shipping†
Single	MC34071P, MC34071AP MC34071D, MC34071AD MC34071DR2, MC34071ADR2	T_A = 0° to +70°C	DIP−8 SO−8 SO−8 / Tape & Reel	50 Units / Rail 98 Units / Rail 2500 Units / Tape & Reel
	MC33071P, MC33071AP MC33071D, MC33071AD MC33071DR2, MC33071ADR2	T_A = −40° to +85°C	DIP−8 SO−8 SO−8 / Tape & Reel	50 Units / Rail 98 Units / Rail 2500 Units / Tape & Reel
Dual	MC34072P, MC34072AP MC34072D, MC34072AD MC34072DR2, MC34072ADR2	T_A = 0° to +70°C	DIP−8 SO−8 SO−8 / Tape & Reel	50 Units / Rail 98 Units / Rail 2500 Units / Tape & Reel
	MC33072P, MC33072AP MC33072D, MC33072AD MC33072DR2, MC33072DR2G, MC33072ADR2	T_A = −40° to +85°C	DIP−8 SO−8 SO−8 / Tape & Reel	50 Units / Rail 98 Units / Rail 2500 Units / Tape & Reel
	MC34072VD MC34072VDR2 MC34072VP	T_A = −40° to +125°C	SO−8 SO−8 / Tape & Reel DIP−8	98 Units / Rail 2500 Units / Tape & Reel 50 Units / Rail
Quad	MC34074P, MC34074AP MC34074D, MC34074AD MC34074DR2, MC34074ADR2	T_A = 0° to +70°C	DIP−14 SO−14 SO−14 / Tape & Reel	25 Units / Rail 55 Units / Rail 2500 Units / Tape & Reel
	MC33074P, MC33074AP MC33074D, MC33074AD MC33074DR2, MC33074ADR2 MC33074DTB, MC33074ADTB MC33074DTBR2, MC33074ADTBR2	T_A = −40° to +85°C	DIP−14 SO−14 SO−14 / Tape & Reel TSSOP−14 TSSOP−14 / Tape & Reel	25 Units / Rail 55 Units / Rail 2500 Units / Tape & Reel 96 Units / Rail 2500 Units / Tape & Reel
	MC34074VD MC34074VDR2 MC34074VP	T_A = −40° to +125°C	SO−14 SO−14 / Tape & Reel DIP−14	55 Units / Rail 2500 Units / Tape & Reel 25 Units / Rail

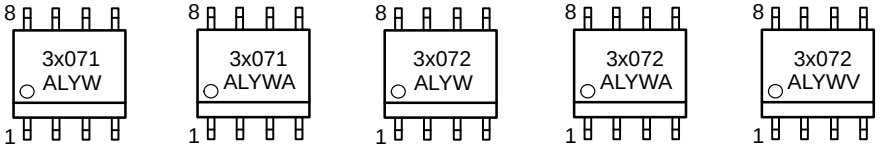
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

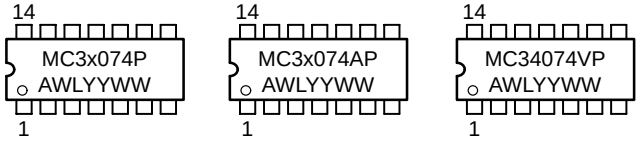
PDIP−8
P SUFFIX
CASE 626



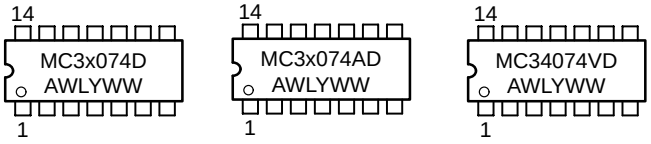
SO−8
D SUFFIX
CASE 751



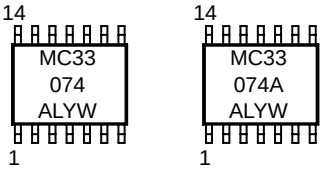
PDIP−14
P SUFFIX
CASE 646



SO−14
D SUFFIX
CASE 751A



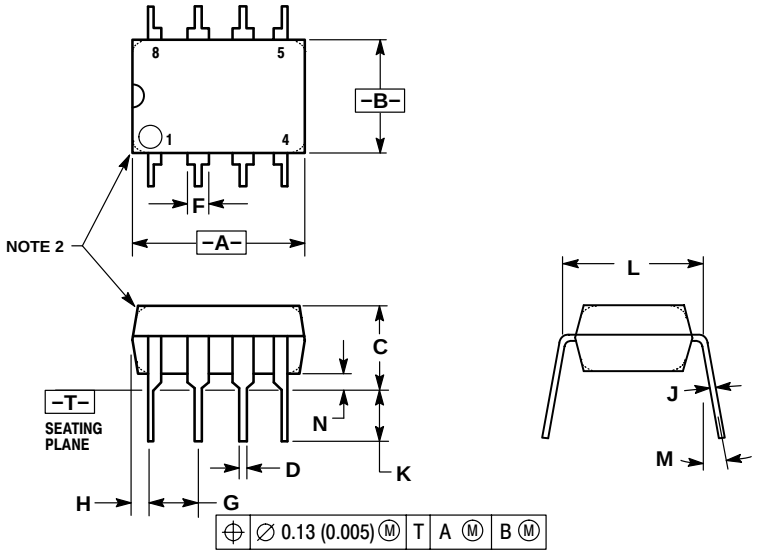
TSSOP−14
DTB SUFFIX
CASE 948G



x = 3 or 4
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE DIMENSIONS

PDIP−8
P SUFFIX
CASE 626−05
ISSUE L

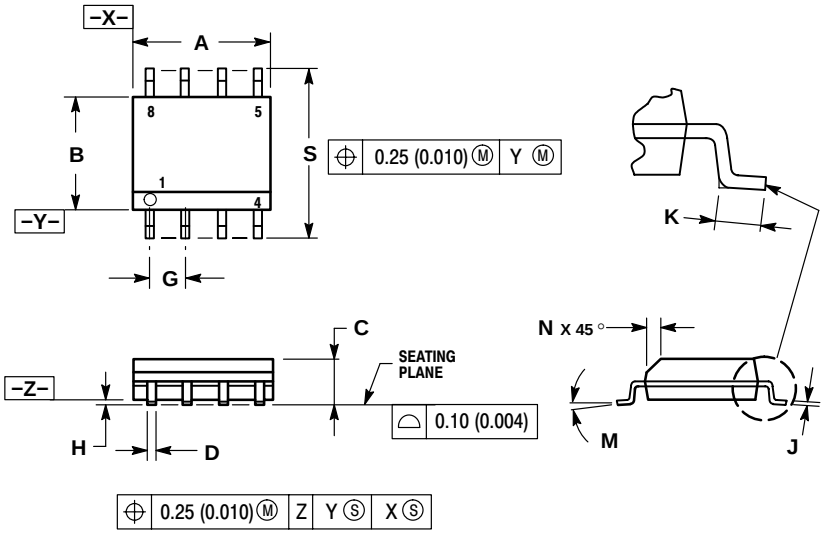


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PACKAGE DIMENSIONS

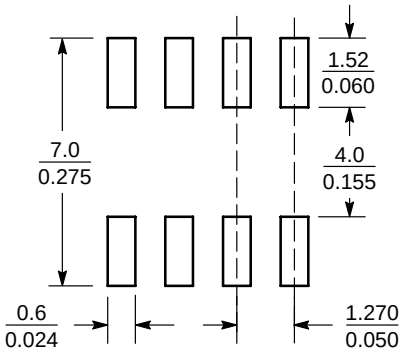
SO−8
D SUFFIX
CASE 751−07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



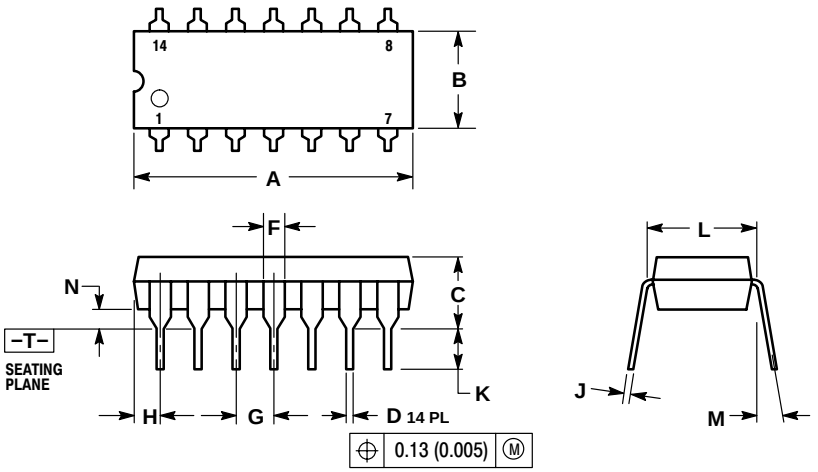
SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

SO−8

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

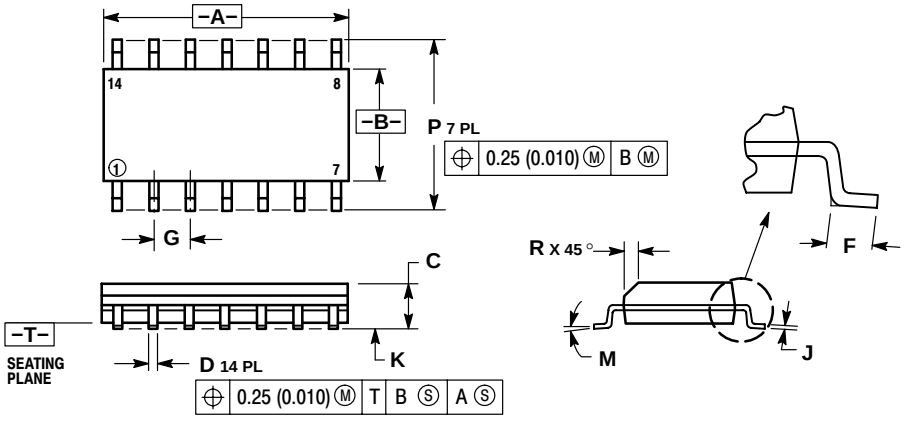
PDIP−14
P SUFFIX
CASE 646−06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

SO−14
D SUFFIX
CASE 751A−03
ISSUE F

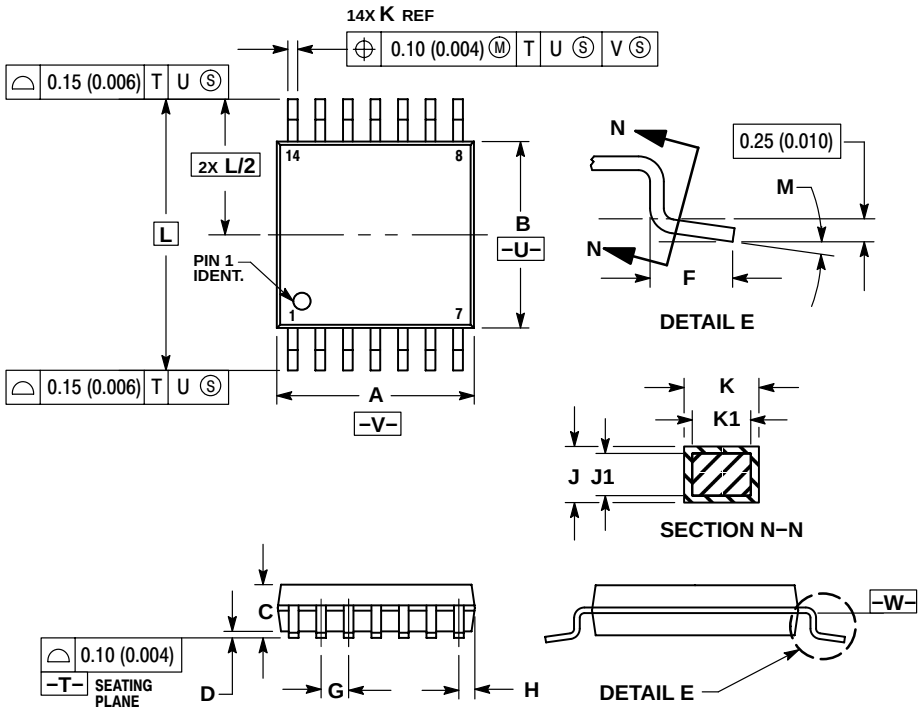


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

TSSOP−14
DTB SUFFIX
CASE 948G−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.

MC33201, MC33202, MC33204, NCV33202, NCV33204

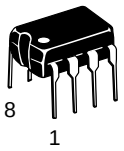
Low Voltage, Rail-to-Rail Operational Amplifiers

The MC33201/2/4 family of operational amplifiers provide rail-to-rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (± 0.9 V) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

- Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over-driven Input Signals
- High Output Current (I_{SC} = 80 mA, Typ)
- Low Supply Current (I_D = 0.9 mA, Typ)
- 600 Ω Output Drive Capability
- Extended Operating Temperature Ranges (-40° to +105°C and -55° to +125°C)
- Typical Gain Bandwidth Product = 2.2 MHz

ON Semiconductor®

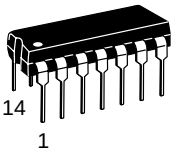
http://onsemi.com



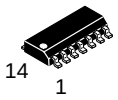
PDIP-8
P, VP SUFFIX
CASE 626

SO-8
D, VD SUFFIX
CASE 751

Micro-8
DM SUFFIX
CASE 846A



PDIP-14
P, VP SUFFIX
CASE 646



SO-14
D, VD SUFFIX
CASE 751A

TSSOP-14
DTB SUFFIX
CASE 948G

ORDERING INFORMATION

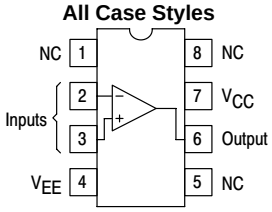
See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 12 of this data sheet.

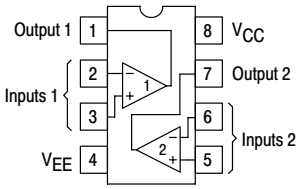
PIN CONNECTIONS

MC33201
All Case Styles



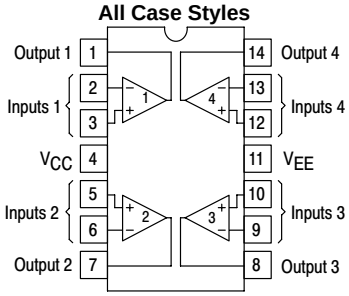
(Top View)

MC33202
All Case Styles

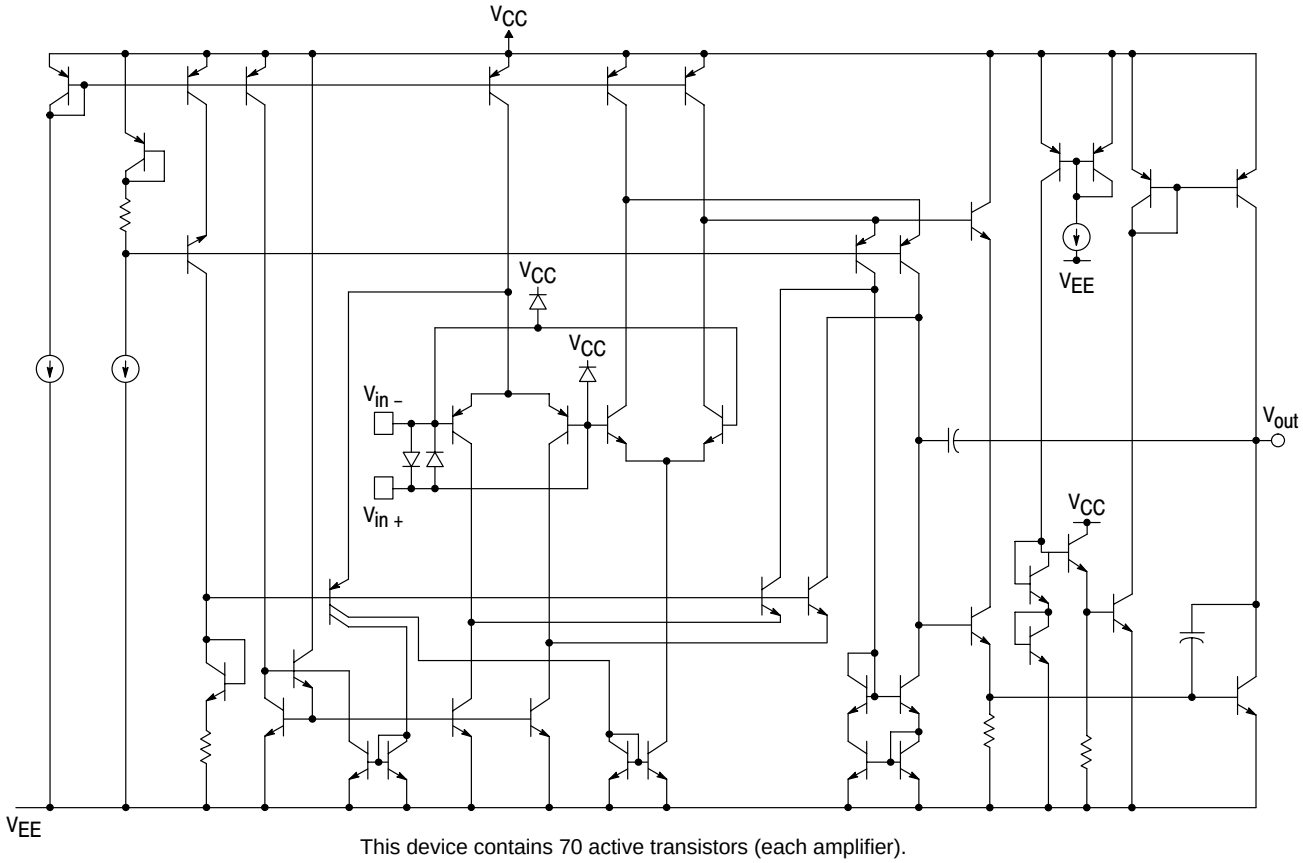


(Top View)

MC33204
All Case Styles



(Top View)



This device contains 70 active transistors (each amplifier).

Figure 1. Circuit Schematic
(Each Amplifier)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+13	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Common Mode Input Voltage Range (Note 2)	V_{CM}	V_{CC} + 0.5 V to V_{EE} - 0.5 V	V
Output Short Circuit Duration	t_S	Note 3	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	- 65 to +150	°C
Maximum Power Dissipation	P_D	Note 3	mW

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	V_{CC} = 2.0 V	V_{CC} = 3.3 V	V_{CC} = 5.0 V	Unit
Input Offset Voltage V_{IO} (max) MC33201 MC33202, NCV33202 MC33204	 ± 8.0 ±10 ±12	 ± 8.0 ±10 ±12	 ± 6.0 ± 8.0 ±10	mV
Output Voltage Swing V_{OH} (R_L = 10 kΩ) V_{OL} (R_L = 10 kΩ)	 1.9 0.10	 3.15 0.15	 4.85 0.15	 V_{min} V_{max}
Power Supply Current per Amplifier (I_D)	 1.125	 1.125	 1.125	mA

Specifications at V_{CC} = 3.3 V are guaranteed by the 2.0 V and 5.0 V tests. V_{EE} = GND.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} 0 V to 0.5 V, V_{CM} 1.0 V to 5.0 V)	3	$\lvert V_{IO} \rvert$				mV
MC33201: T_A = + 25°C			-	-	6.0	
MC33201: T_A = - 40° to +105°C			-	-	9.0	
MC33201V: T_A = - 55° to +125°C			-	-	13	
MC33202: T_A = + 25°C			-	-	8.0	
MC33202: T_A = - 40° to +105°C			-	-	11	
MC33202V: T_A = - 55° to +125°C			-	-	14	
NCV33202V: T_A = - 55° to +125°C (Note 4)			-	-	14	
MC33204: T_A = + 25°C			-	-	10	
MC33204: T_A = - 40° to +105°C			-	-	13	
MC33204V: T_A = - 55° to +125°C			-		17	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω)	4	$\Delta V_{IO}/\Delta T$				μV/°C
T_A = - 40° to +105°C			-	2.0	-	
T_A = - 55° to +125°C			-	2.0	-	
Input Bias Current (V_{CM} = 0 V to 0.5 V, V_{CM} = 1.0 V to 5.0 V)	5, 6	$\lvert I_{IB} \rvert$				nA
T_A = + 25°C			-	80	200	
T_A = - 40° to +105°C			-	100	250	
T_A = - 55° to +125°C			-	-	500	
Input Offset Current (V_{CM} = 0 V to 0.5 V, V_{CM} = 1.0 V to 5.0 V)	-	$\lvert I_{IO} \rvert$				nA
T_A = + 25°C			-	5.0	50	
T_A = - 40° to +105°C			-	10	100	
T_A = - 55° to +125°C			-	-	200	
Common Mode Input Voltage Range	-	V_{ICR}	V_{EE}	-	V_{CC}	V

1. The differential input voltage of each amplifier is limited by two internal parallel back-to-back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
2. The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 2)
4. *NCV33202 and NCV33204 are qualified for automotive use.*

DC ELECTRICAL CHARACTERISTICS (cont.) (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Large Signal Voltage Gain (V_{CC} = + 5.0 V, V_{EE} = - 5.0 V) R_L = 10 kΩ R_L = 600 Ω	7	A_{VOL}	 50 25	 300 250	 - -	kV/V
Output Voltage Swing (V_{ID} = ± 0.2 V) R_L = 10 kΩ R_L = 10 kΩ R_L = 600 Ω R_L = 600 Ω	8, 9, 10	 V_{OH} V_{OL} V_{OH} V_{OL}	 4.85 - 4.75 -	 4.95 0.05 4.85 0.15	 - 0.15 - 0.25	V
Common Mode Rejection (V_{in} = 0 V to 5.0 V)	11	CMR	60	90	-	dB
Power Supply Rejection Ratio V_{CC}/V_{EE} = 5.0 V/GND to 3.0 V/GND	12	PSRR	 500	 25	 -	μV/V
Output Short Circuit Current (Source and Sink)	13, 14	I_{SC}	50	80	-	mA
Power Supply Current per Amplifier (V_O = 0 V) T_A = - 40° to +105°C T_A = - 55° to +125°C	15	I_D	 - -	 0.9 0.9	 1.125 1.125	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_S = ± 2.5 V, V_O = - 2.0 V to + 2.0 V, R_L = 2.0 kΩ, A_V = +1.0)	16, 26	SR	 0.5	 1.0	 -	V/μs
Gain Bandwidth Product (f = 100 kHz)	17	GBW	-	2.2	-	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	20, 21, 22	A_M	-	12	-	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	20, 21, 22	ϕ_M	-	65	-	Deg
Channel Separation (f = 1.0 Hz to 20 kHz, A_V = 100)	23	CS	-	90	-	dB
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 600 Ω, THD ≤ 1 %)		BW_P	-	28	-	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 1.0 V_{pp}, A_V = 1.0) f = 1.0 kHz f = 10 kHz	24	THD	 - -	 0.002 0.008	 - -	%
Open Loop Output Impedance (V_O = 0 V, f = 2.0 MHz, A_V = 10)		$\lvert Z_O \rvert$	 -	 100	 -	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	-	200	-	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	-	8.0	-	pF
Equivalent Input Noise Voltage (R_S = 100 Ω) f = 10 Hz f = 1.0 kHz	25	e_n	 - -	 25 20	 - -	$\frac{nV}{\sqrt{Hz}}$
Equivalent Input Noise Current f = 10 Hz f = 1.0 kHz	25	i_n	 - -	 0.8 0.2	 - -	$\frac{pA}{\sqrt{Hz}}$

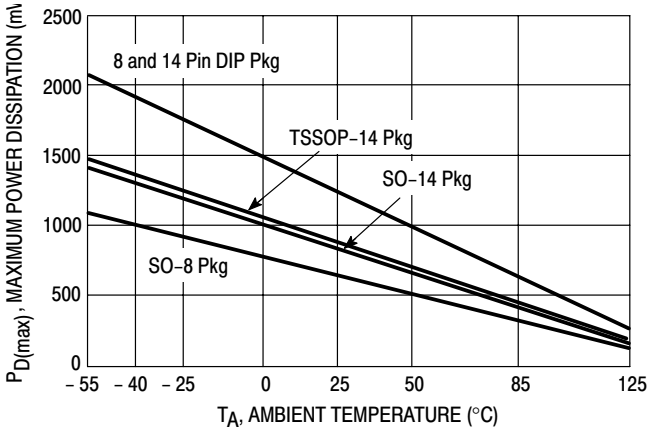


Figure 2. Maximum Power Dissipation versus Temperature

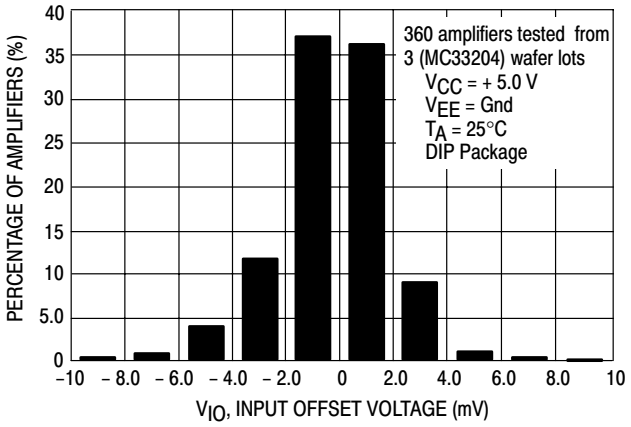


Figure 3. Input Offset Voltage Distribution

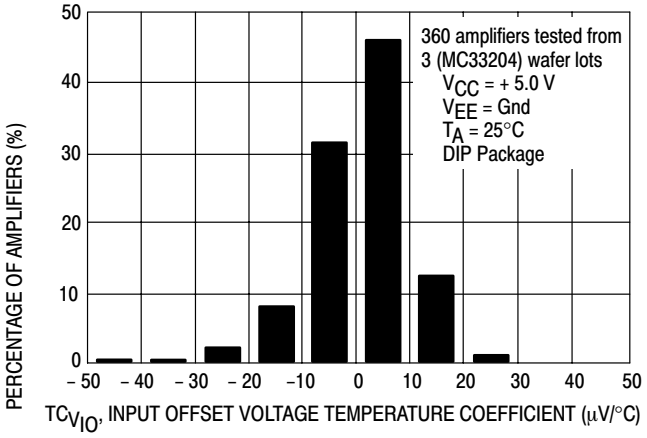


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

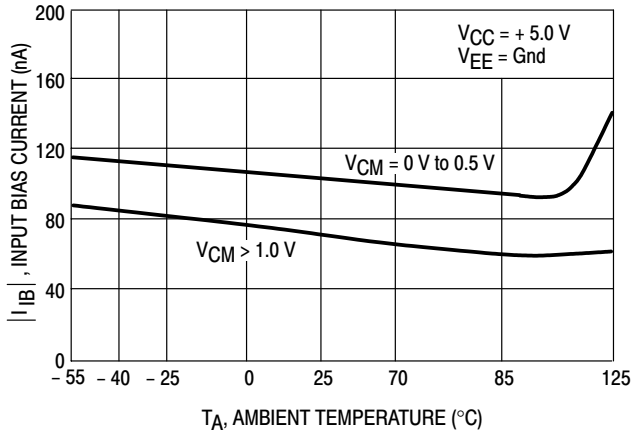


Figure 5. Input Bias Current versus Temperature

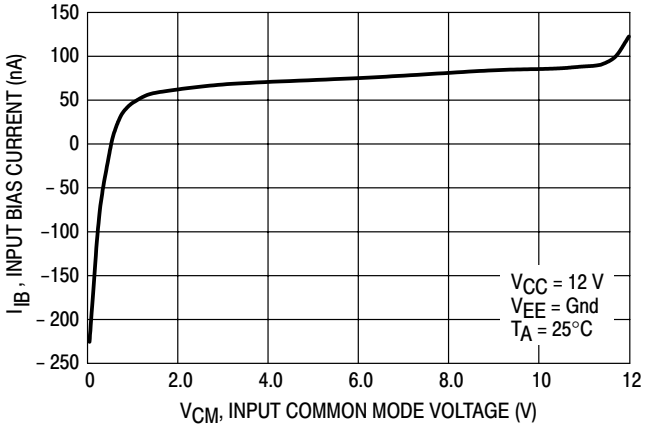


Figure 6. Input Bias Current versus Common Mode Voltage

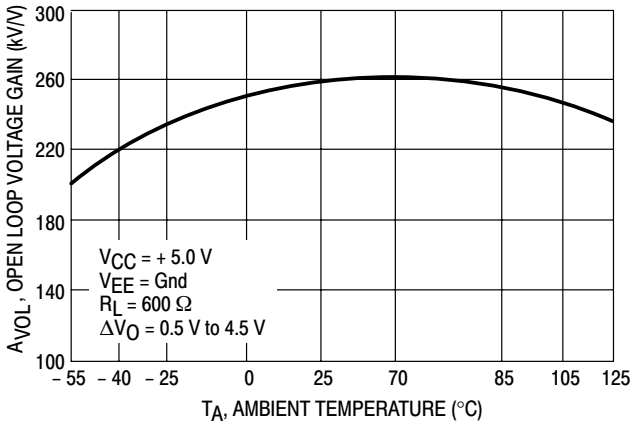


Figure 7. Open Loop Voltage Gain versus Temperature

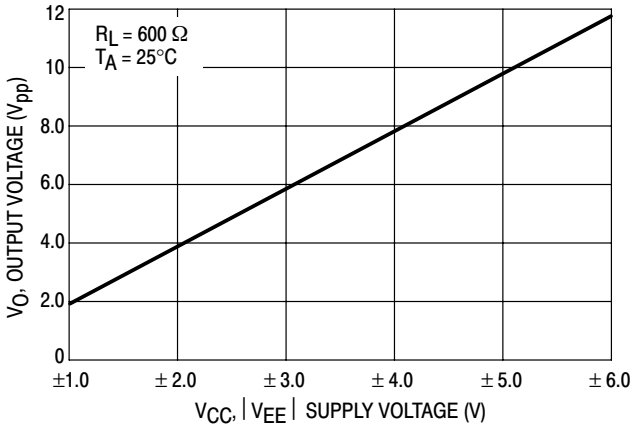


Figure 8. Output Voltage Swing versus Supply Voltage

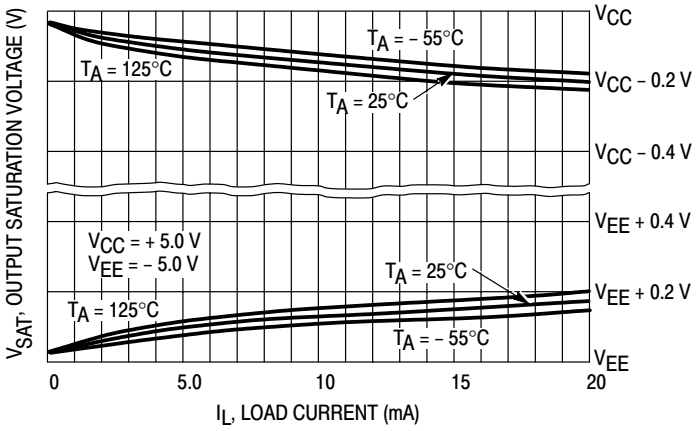


Figure 9. Output Saturation Voltage versus Load Current

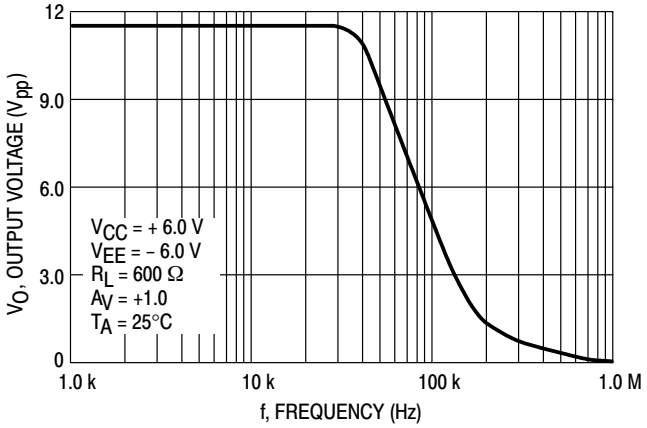


Figure 10. Output Voltage versus Frequency

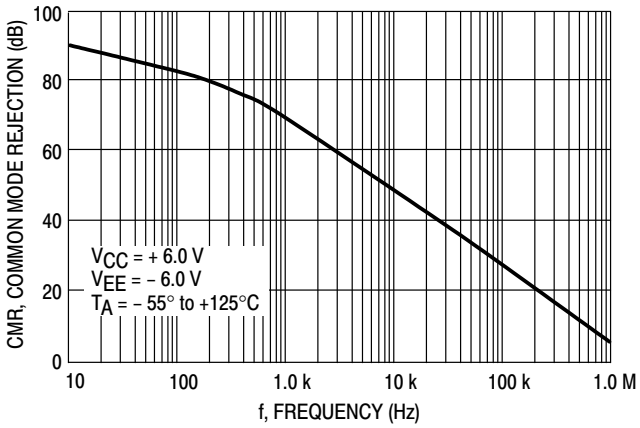


Figure 11. Common Mode Rejection versus Frequency

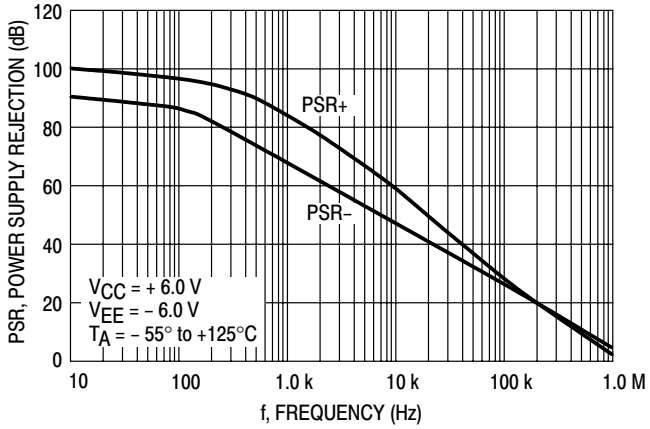


Figure 12. Power Supply Rejection versus Frequency

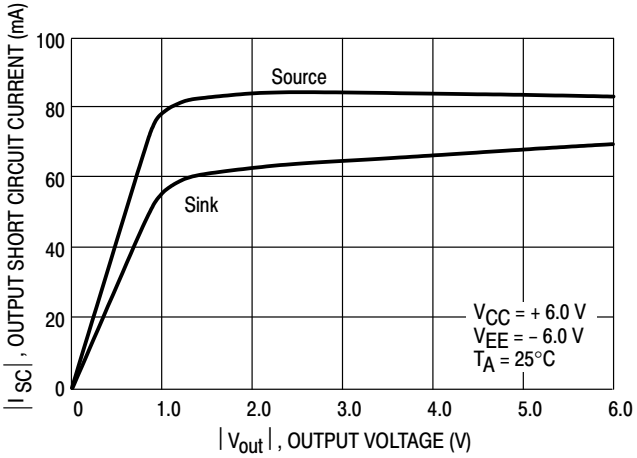


Figure 13. Output Short Circuit Current versus Output Voltage

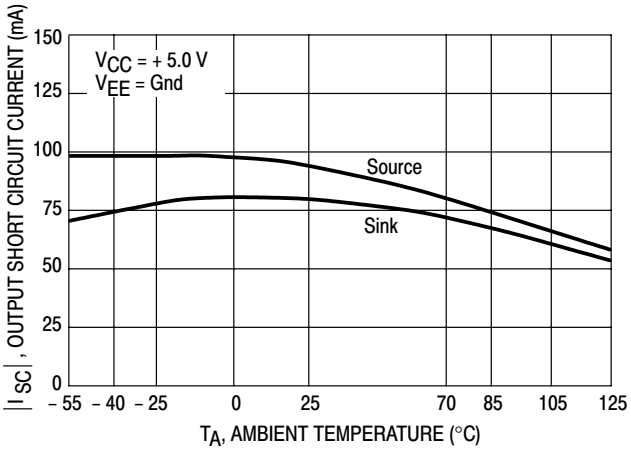


Figure 14. Output Short Circuit Current versus Temperature

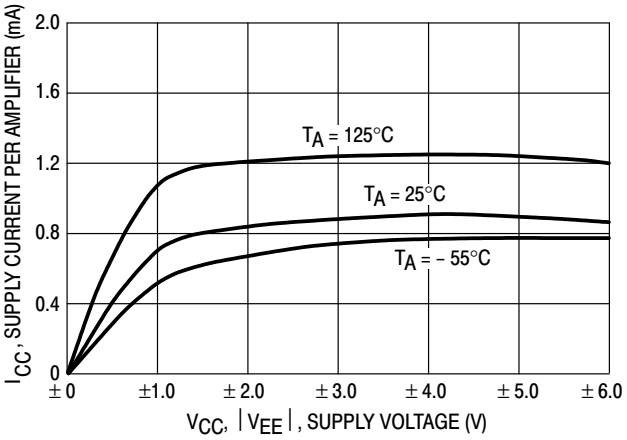


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

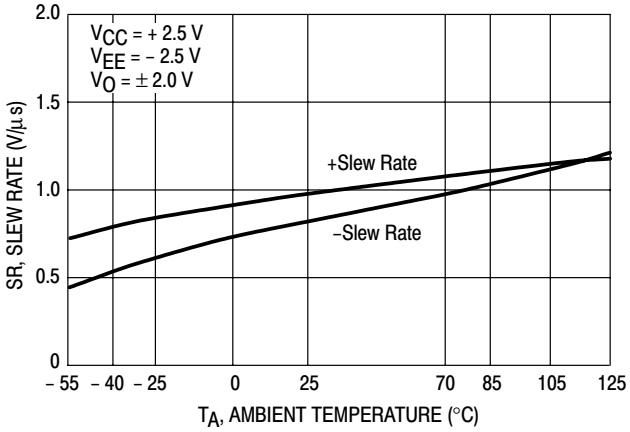


Figure 16. Slew Rate versus Temperature

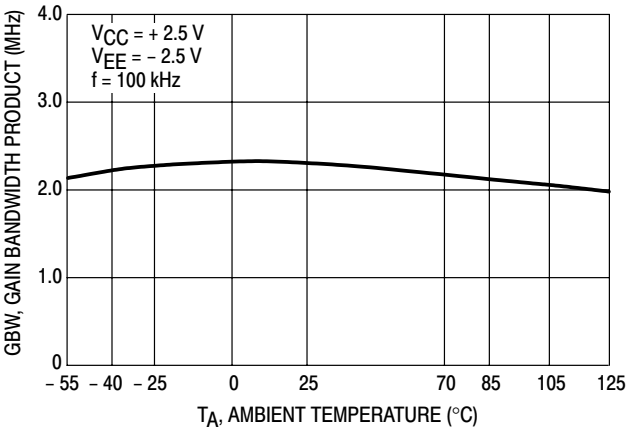


Figure 17. Gain Bandwidth Product versus Temperature

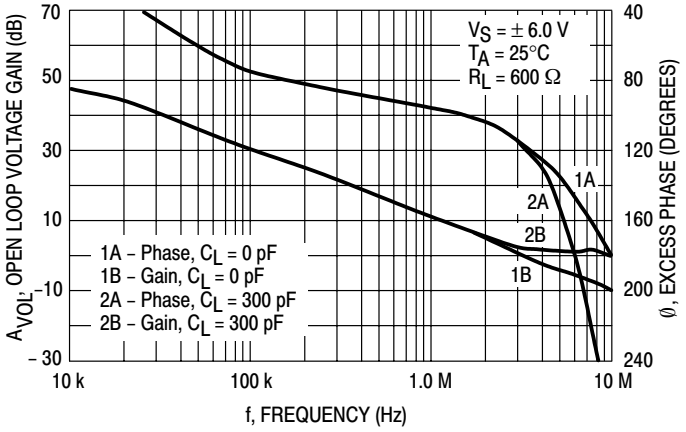


Figure 18. Voltage Gain and Phase versus Frequency

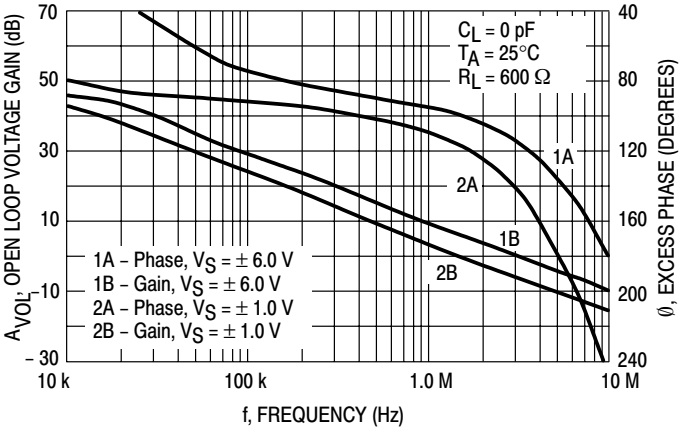


Figure 19. Voltage Gain and Phase versus Frequency

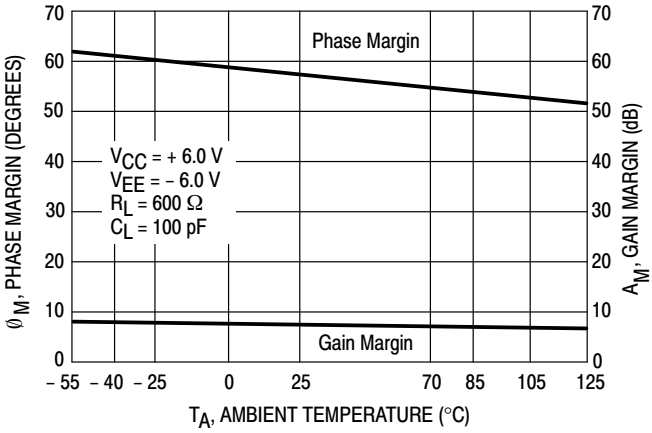


Figure 20. Gain and Phase Margin versus Temperature

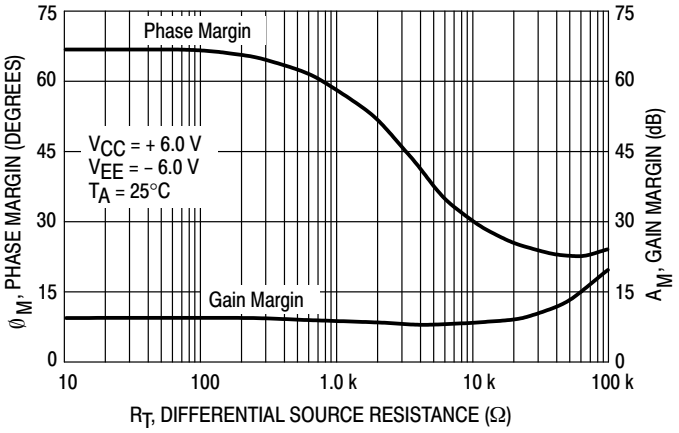


Figure 21. Gain and Phase Margin versus Differential Source Resistance

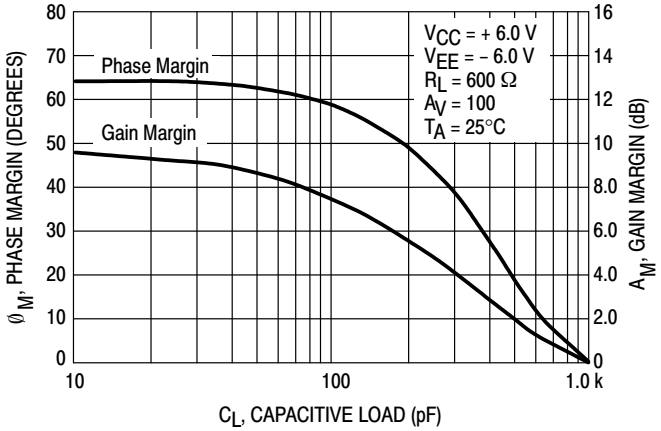


Figure 22. Gain and Phase Margin versus Capacitive Load

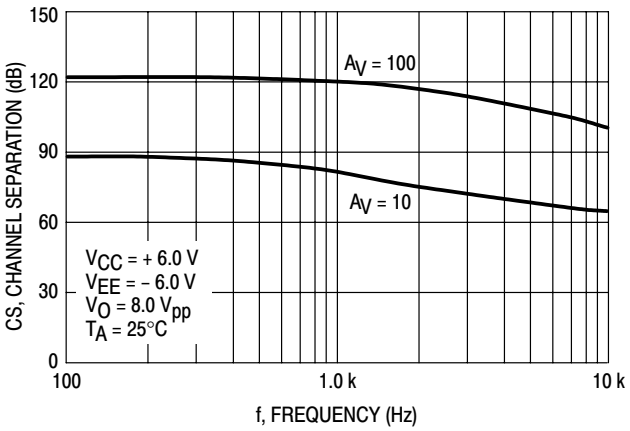


Figure 23. Channel Separation versus Frequency

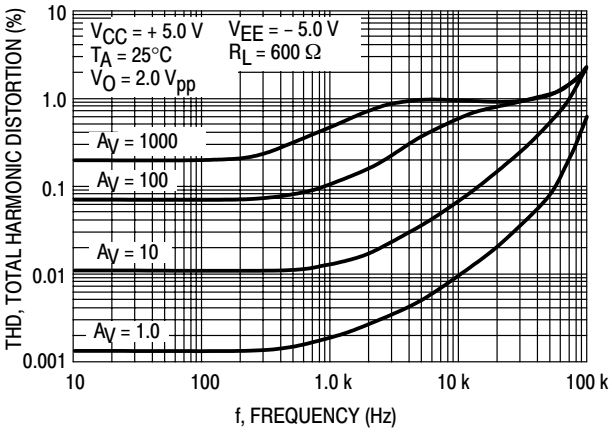


Figure 24. Total Harmonic Distortion versus Frequency

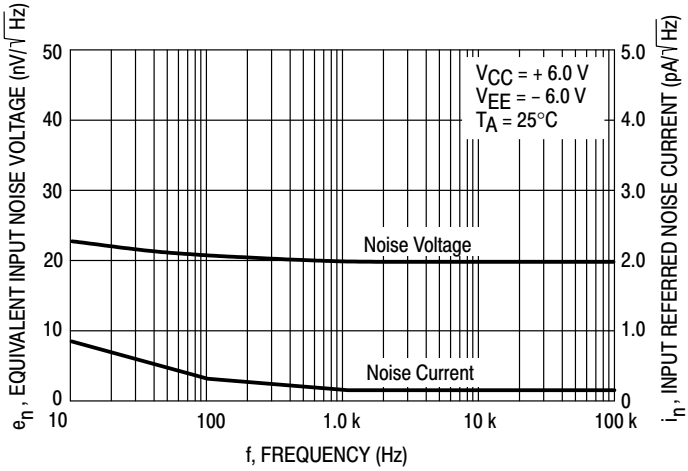


Figure 25. Equivalent Input Noise Voltage and Current versus Frequency

DETAILED OPERATING DESCRIPTION

General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail-to-rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

Circuit Information

Rail-to-rail performance is achieved at the input of the amplifiers by using parallel NPN-PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross-coupling techniques have been used to keep this change to a minimum.

In addition to its rail-to-rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 Ω loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

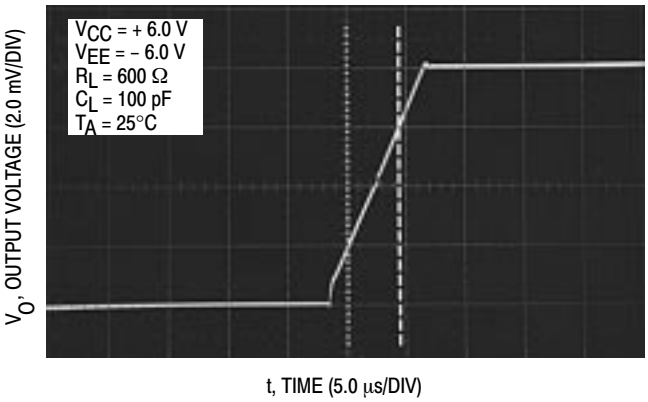


Figure 26. Noninverting Amplifier Slew Rate

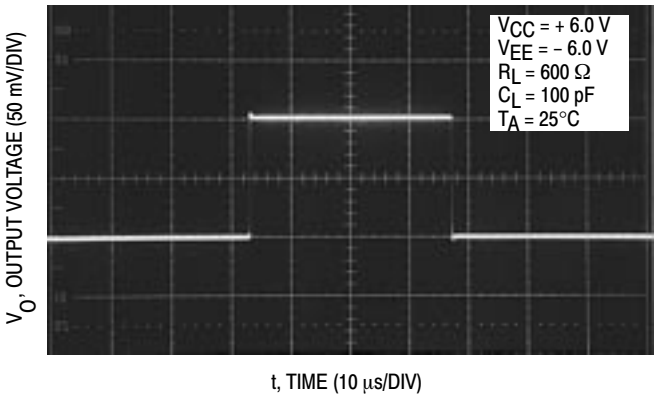


Figure 27. Small Signal Transient Response

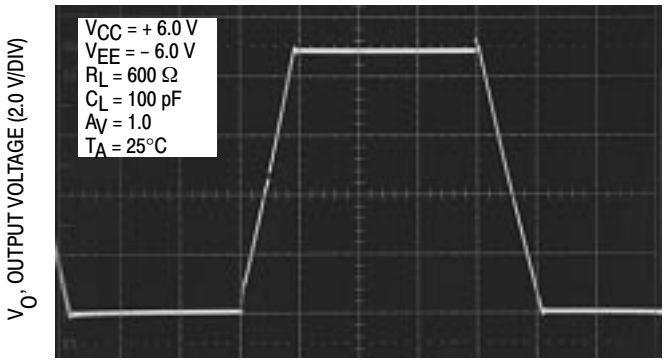
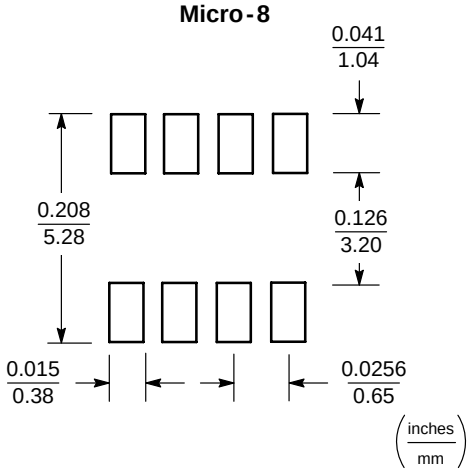


Figure 28. Large Signal Transient Response

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.

Micro-8



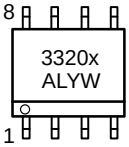
ORDERING INFORMATION

Operational Amplifier Function	Device	Operating Temperature Range	Package	Shipping
Single	MC33201D	T_A= -40° to +105°C	SO-8	98 Units / Rail
	MC33201DR2		SO-8	2500 Units / Tape & Reel
	MC33201P		Plastic DIP	50 Units / Rail
	MC33201VD	T_A = -55° to 125°C	SO-8	98 Units / Rail
Dual	MC33202D	T_A= -40 ° to +105°C	SO-8	98 Units / Rail
	MC33202DR2		SO-8	2500 Units / Tape & Reel
	MC33202DMR2		Micro-8	4000 Units / Tape & Reel
	MC33202P		Plastic DIP	50 Units / Rail
	MC33202VD	T_A = -55° to 125°C	SO-8	98 Units / Rail
	MC33202VDR2		SO-8	2500 Units / Tape & Reel
	NCV33202VDR2*		SO-8	2500 Units / Tape & Reel
	MC33202VP		Plastic DIP	50 Units / Rail
Quad	MC33204D	T_A= -40 ° to +105°C	SO-14	55 Units / Rail
	MC33204DR2		SO-14	2500 Units / Tape & Reel
	MC33204DTB		TSSOP-14	96 Units / Rail
	MC33204DTBR2		TSSOP-14	2500 Units / Tape & Reel
	MC33204P		Plastic DIP	25 Units / Rail
	MC33204VD	T_A = -55° to 125°C	SO-14	55 Units / Rail
	MC33204VDR2		SO-14	2500 Units / Tape & Reel
	NCV33204DR2*		SO-14	2500 Units / Tape & Reel
	NCV33204DTBR2*		TSSOP-14	2500 Units / Tape & Reel
	MC33204VP		Plastic DIP	25 Units / Rail

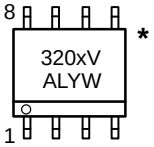
*NCV33202 and NCV33204 are qualified for automotive use.

MARKING DIAGRAMS

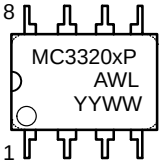
SO-8
D SUFFIX
CASE 751



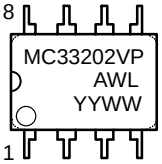
SO-8
VD SUFFIX
CASE 751



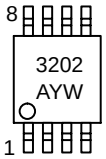
PDIP-8
P SUFFIX
CASE 626



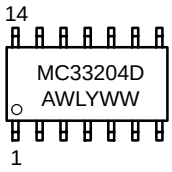
PDIP-8
VP SUFFIX
CASE 626



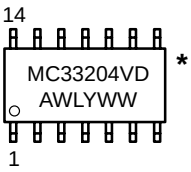
Micro-8
DM SUFFIX
CASE 846A



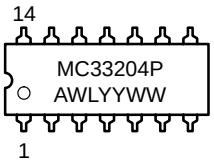
SO-14
D SUFFIX
CASE 751A



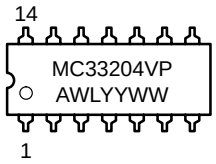
SO-14
VD SUFFIX
CASE 751A



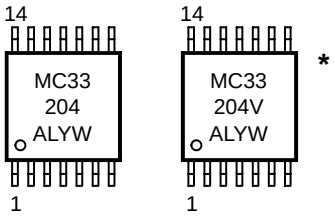
PDIP-14
P SUFFIX
CASE 646



PDIP-14
VP SUFFIX
CASE 646



TSSOP-14
DTB SUFFIX
CASE 948G

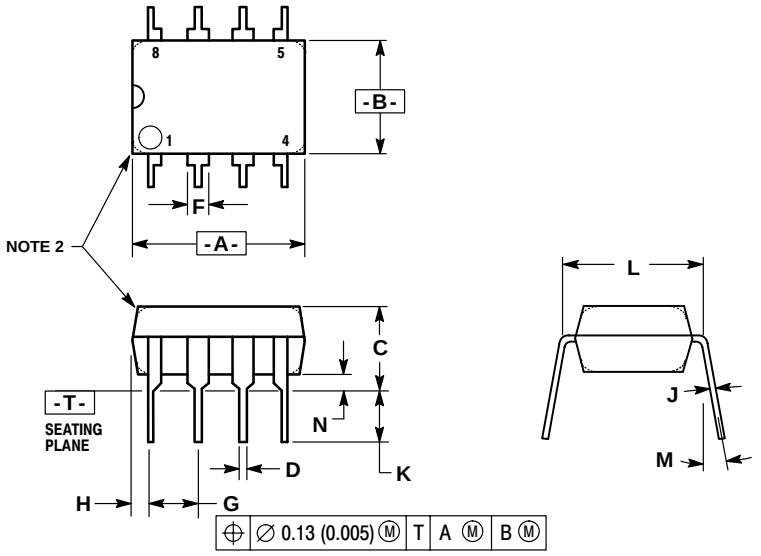


x = 1 or 2
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

*This marking diagram applies to NCV3320x

PACKAGE DIMENSIONS

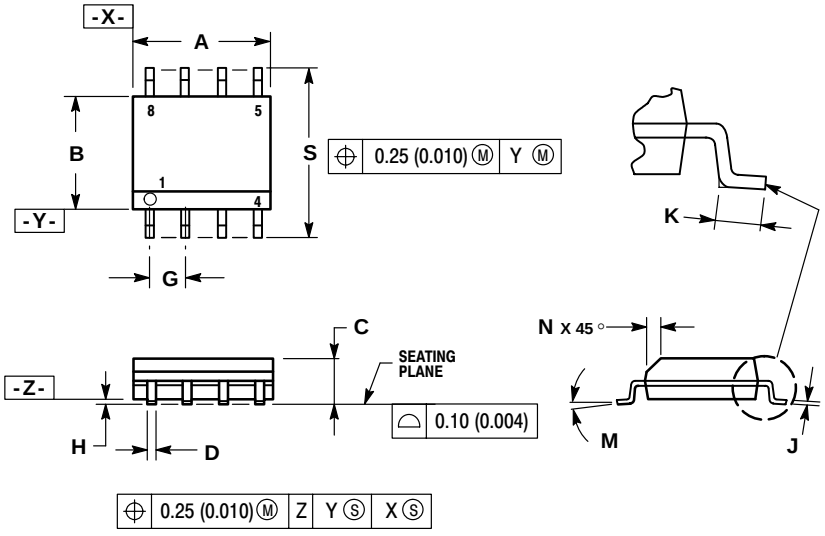
PDIP-8
P, VP SUFFIX
CASE 626-05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

SO-8
D, VD SUFFIX
CASE 751-07
ISSUE AA

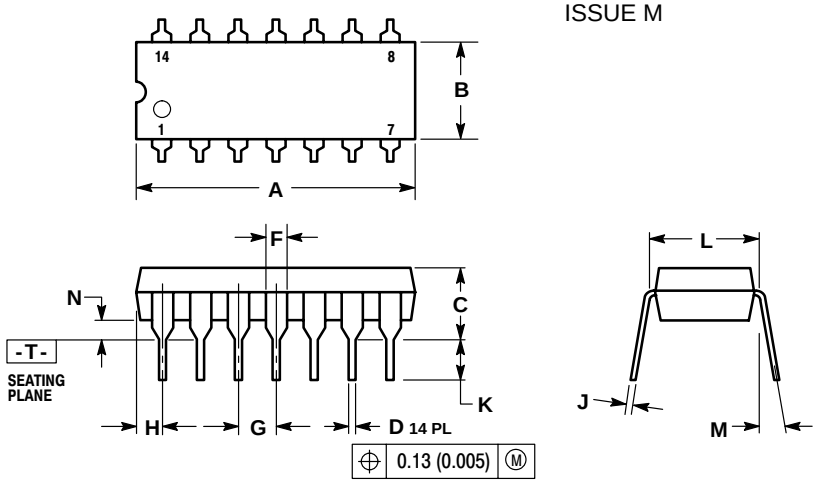


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDAARD IS 751−07

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PACKAGE DIMENSIONS

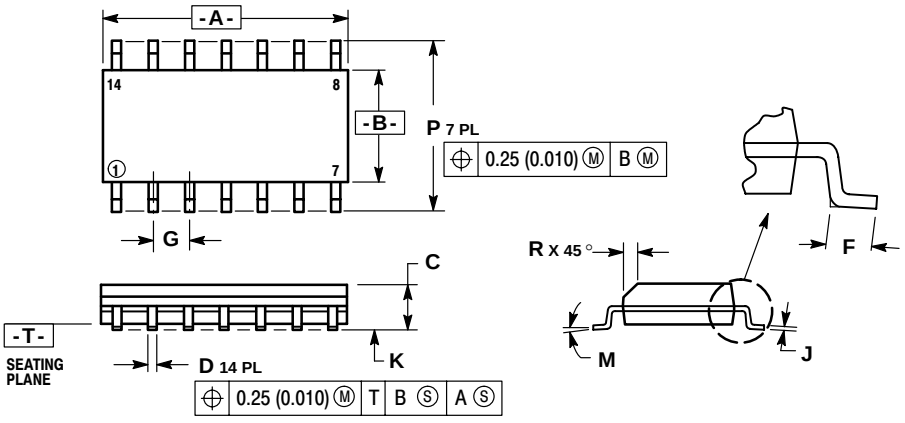
PDIP-14
P, VP SUFFIX
CASE 646-06
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

SO-14
D, VD SUFFIX
CASE 751A-03
ISSUE F

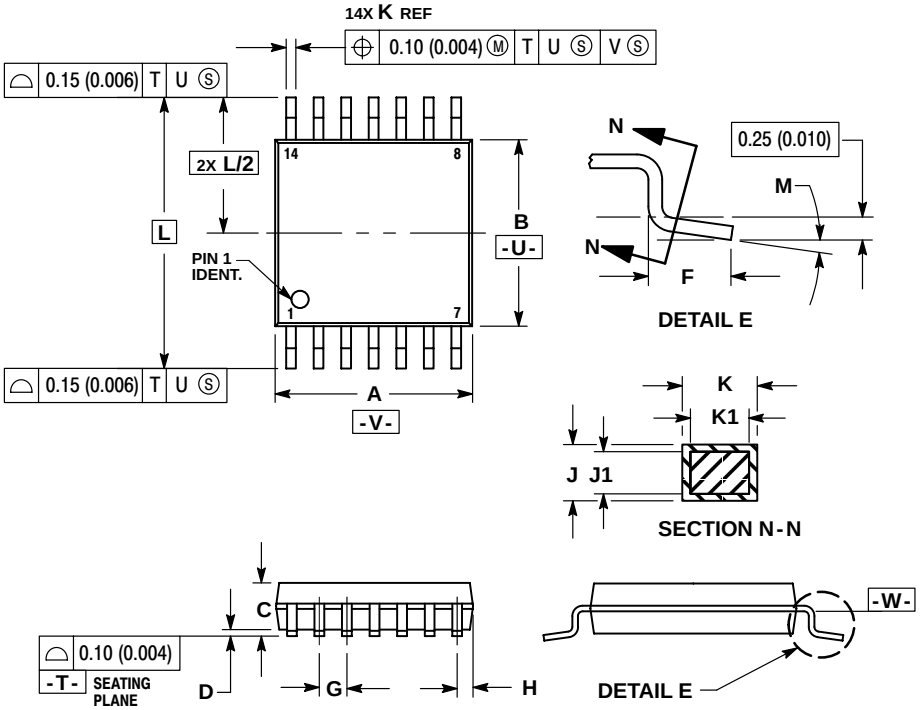


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

TSSOP-14
DTB SUFFIX
CASE 948G-01
ISSUE O

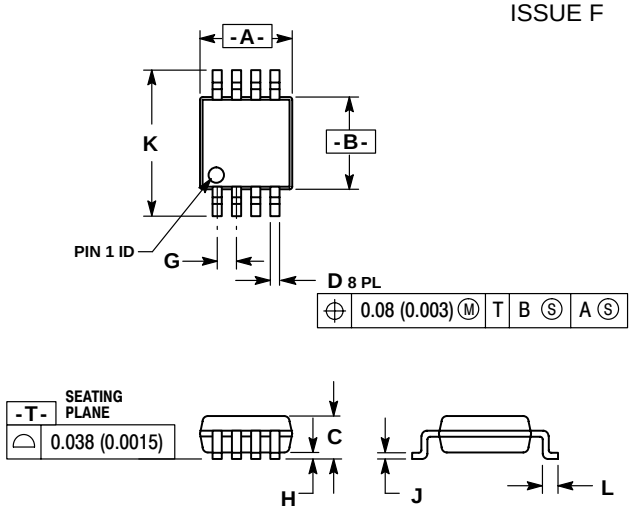


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

PACKAGE DIMENSIONS

Micro-8
DM SUFFIX
CASE 846A-02
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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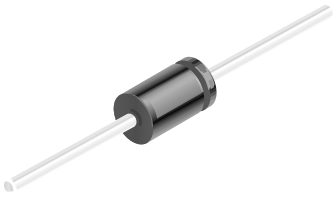
1N4001 - 1N4007

Features

- Low forward voltage drop.
- High surge current capability.



DO-41
COLOR BAND DENOTES CATHODE

General Purpose Rectifiers

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ T_A = 75°C	1.0							A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
T_{stg}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

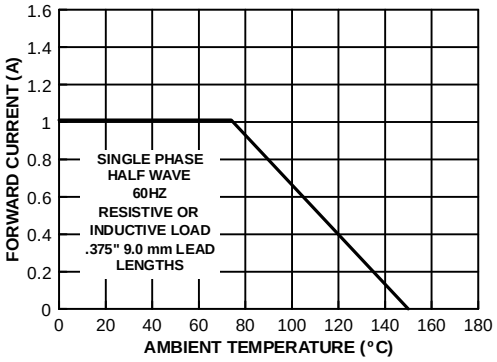
Electrical Characteristics

T_A = 25°C unless otherwise noted

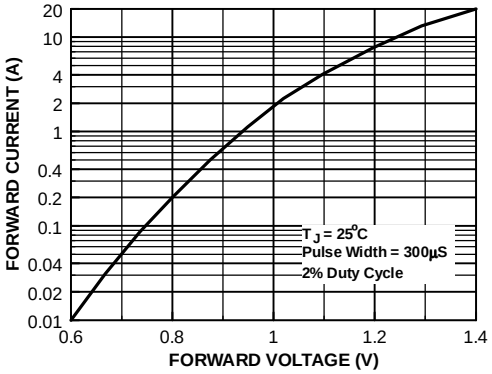
Symbol	Parameter	Device							Units
		4001	4002	4003	4004	4005	4006	4007	
V_F	Forward Voltage @ 1.0 A	1.1							V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle T_A = 75°C	30							µA
I_R	Reverse Current @ rated V_R T_A = 25°C T_A = 100°C	5.0 500							µA µA
C_T	Total Capacitance V_R = 4.0 V, f = 1.0 MHz	15							pF

Typical Characteristics

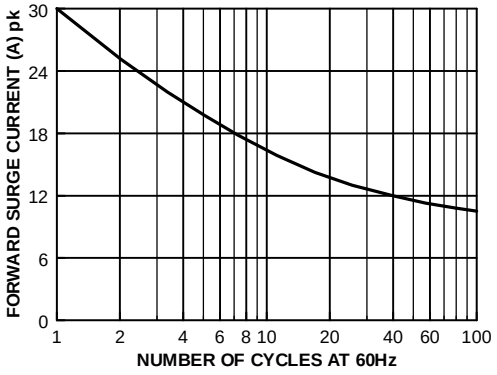
Forward Current Derating Curve



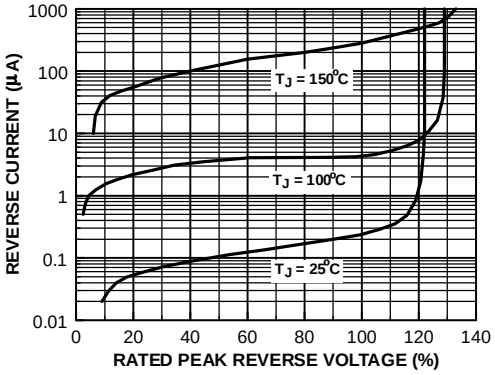
Forward Characteristics



Non-Repetitive Surge Current



Reverse Characteristics



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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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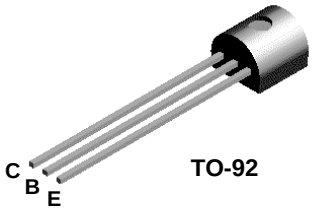
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

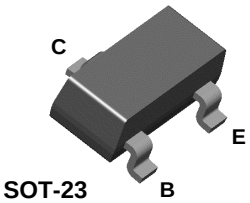
FAIRCHILD SEMICONDUCTOR™

Jameco Part Number 178597

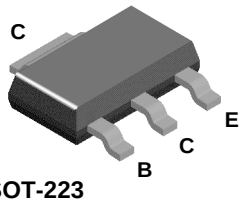
2N3904 MMBT3904 PZT3904



TO-92



SOT-23
Mark: 1A



SOT-223

NPN General Purpose Amplifier

This device is designed as a general purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier.

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

T_A = 25°C unless otherwise noted

Symbol	Characteristic	Max			Units
		2N3904	*MMBT3904	**PZT3904	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

**Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

NPN General Purpose Amplifier
(continued)

Electrical Characteristics
T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1.0 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	6.0		V
I_{BL}	Base Cutoff Current	V_{CE} = 30 V, V_{EB} = 3V		50	nA
I_{CEX}	Collector Cutoff Current	V_{CE} = 30 V, V_{EB} = 3V		50	nA
ON CHARACTERISTICS*					
h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 1.0 V I_C = 1.0 mA, V_{CE} = 1.0 V I_C = 10 mA, V_{CE} = 1.0 V I_C = 50 mA, V_{CE} = 1.0 V I_C = 100 mA, V_{CE} = 1.0 V	40 70 100 60 30	 300 	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA		0.2 0.3	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA	0.65	0.85 0.95	V V
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	300		MHz
C_{obo}	Output Capacitance	V_{CB} = 5.0 V, I_E = 0, f = 1.0 MHz		4.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 1.0 MHz		8.0	pF
NF	Noise Figure	I_C = 100 μA, V_{CE} = 5.0 V, R_S =1.0kΩ,f=10 Hz to 15.7kHz		5.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = 3.0 V, V_{BE} = 0.5 V, I_C = 10 mA, I_{B1} = 1.0 mA		35	ns
t_r	Rise Time			35	ns
t_s	Storage Time	V_{CC} = 3.0 V, I_C = 10mA I_{B1} = I_{B2} = 1.0 mA		200	ns
t_f	Fall Time			50	ns

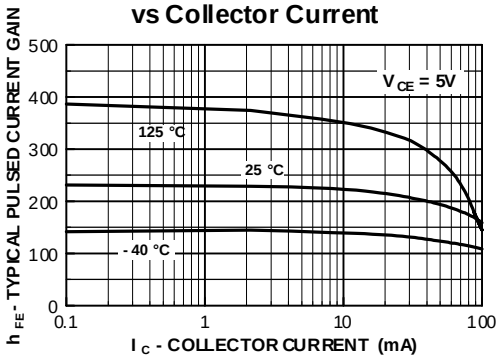
*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Spice Model

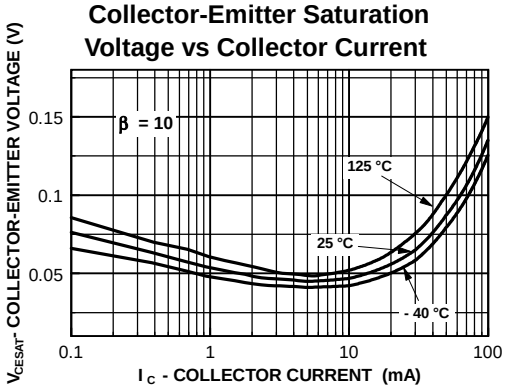
NPN (Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259 Ise=6.734 Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75 Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)

Typical Characteristics

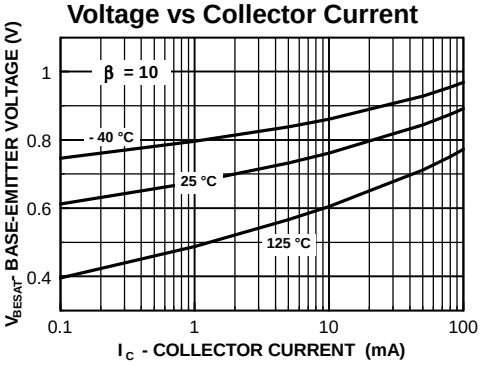
Typical Pulsed Current Gain vs Collector Current



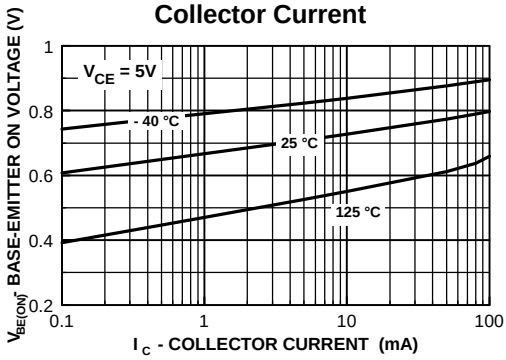
Collector-Emitter Saturation Voltage vs Collector Current



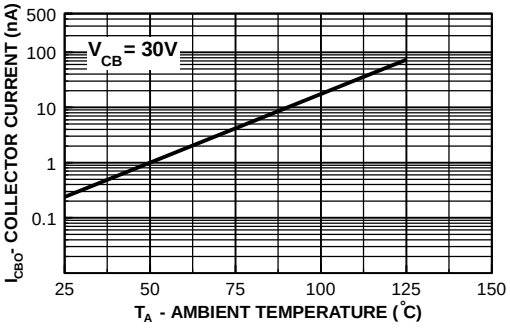
Base-Emitter Saturation Voltage vs Collector Current



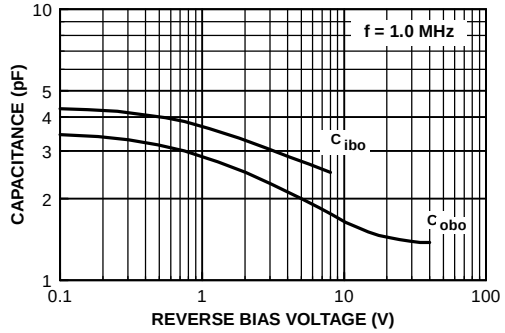
Base-Emitter ON Voltage vs Collector Current



Collector-Cutoff Current vs Ambient Temperature

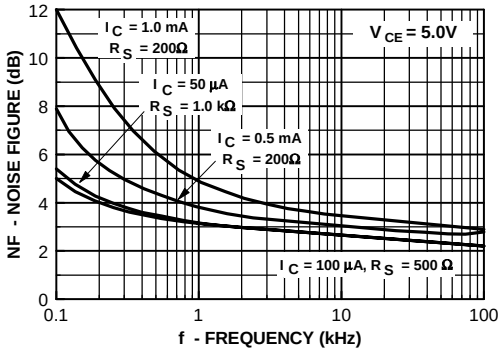


Capacitance vs Reverse Bias Voltage

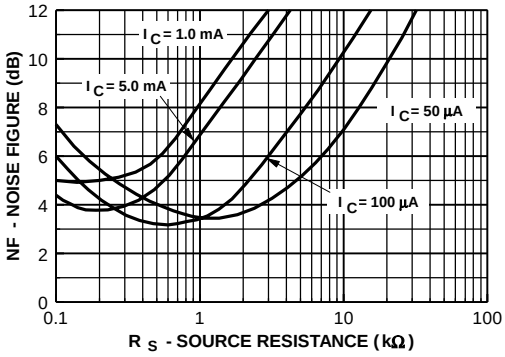


Typical Characteristics (continued)

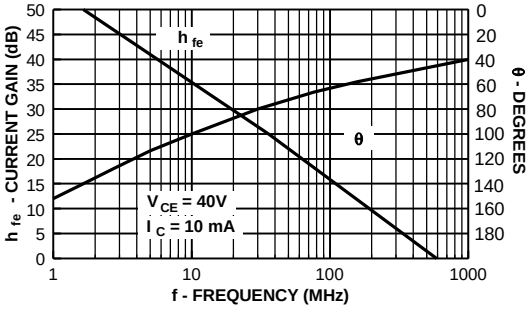
Noise Figure vs Frequency



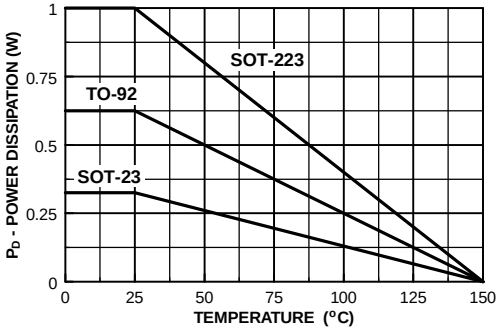
Noise Figure vs Source Resistance



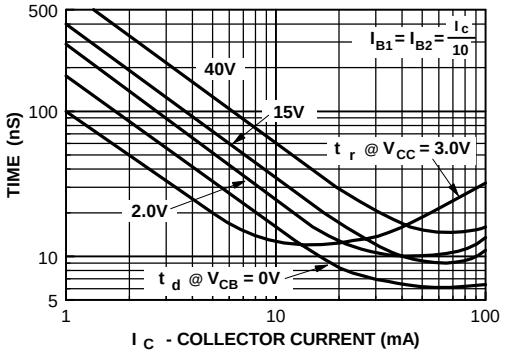
Current Gain and Phase Angle vs Frequency



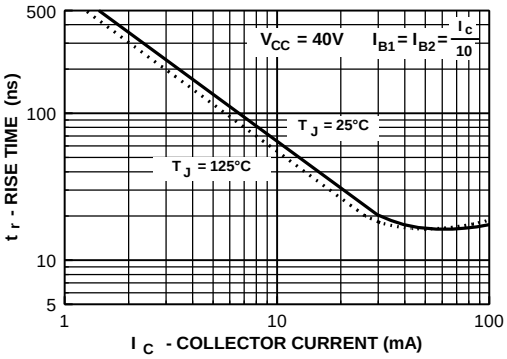
Power Dissipation vs Ambient Temperature



Turn-On Time vs Collector Current

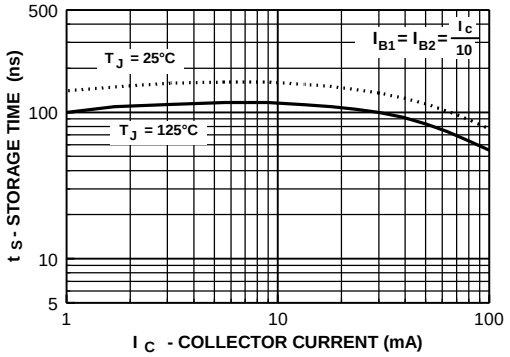


Rise Time vs Collector Current

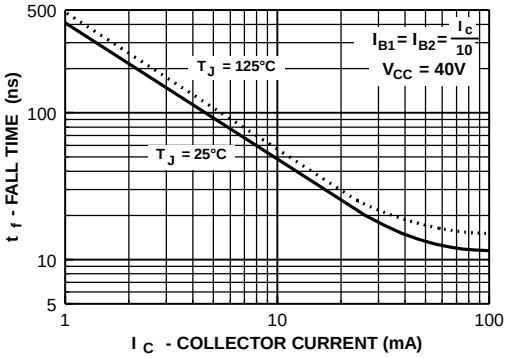


Typical Characteristics (continued)

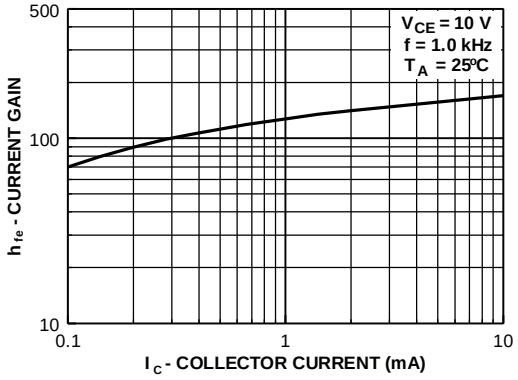
Storage Time vs Collector Current



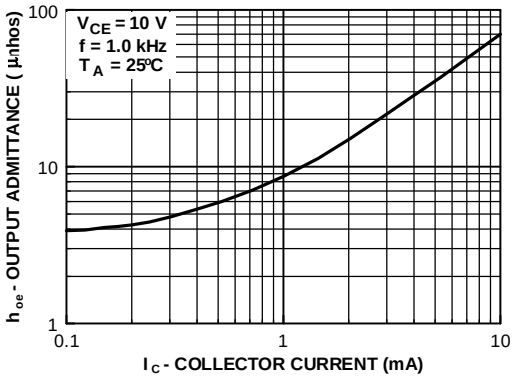
Fall Time vs Collector Current



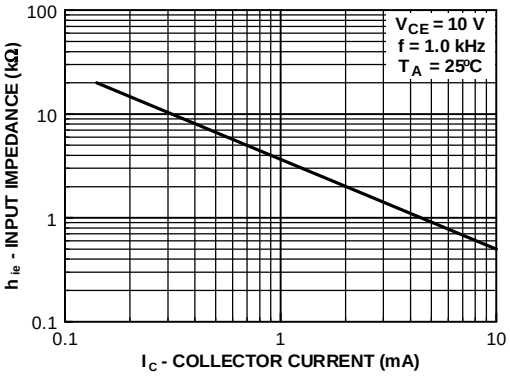
Current Gain



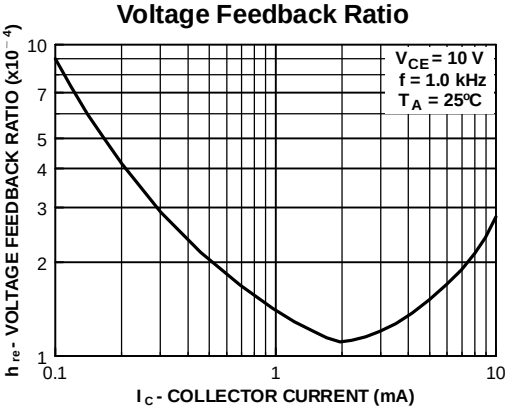
Output Admittance



Input Impedance



Voltage Feedback Ratio



Test Circuits

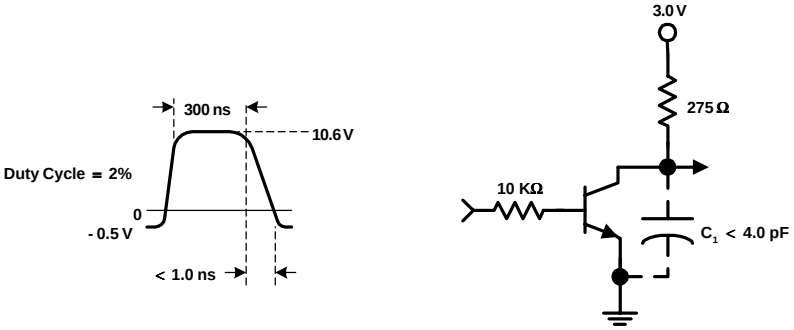


FIGURE 1: Delay and Rise Time Equivalent Test Circuit

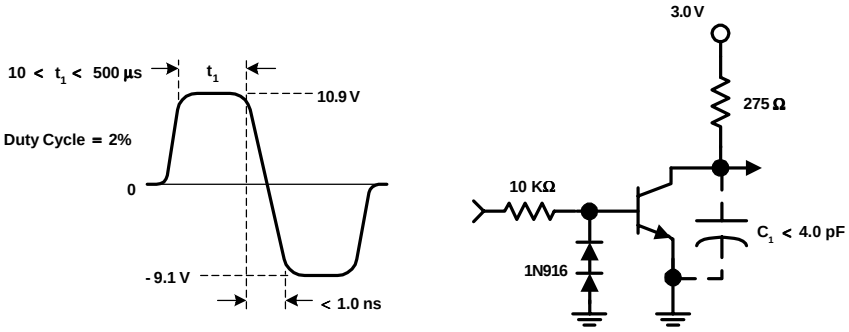
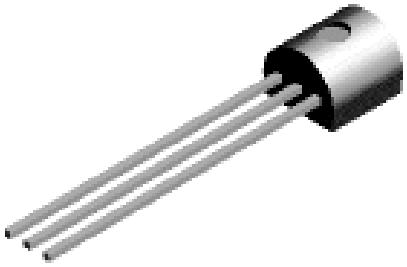


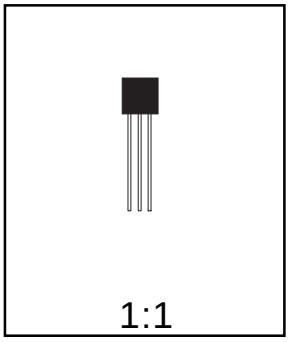
FIGURE 2: Storage and Fall Time Equivalent Test Circuit

TO-92 Package Dimensions

FAIRCHILD SEMICONDUCTOR™

TO-92 (FS PKG Code 92, 94, 96)





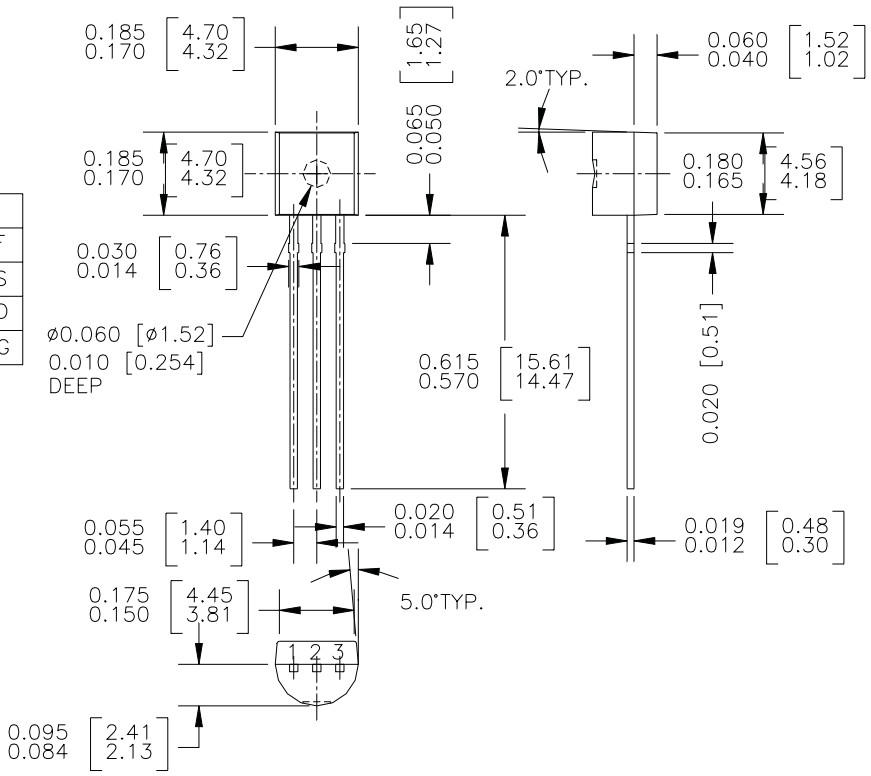
Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.1977

TO−92 (92,94,96)

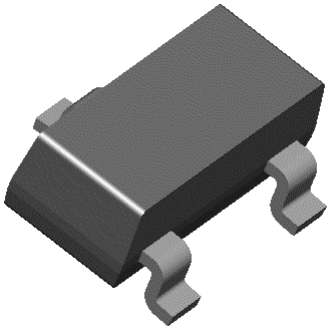
PIN	92		94		96	
	B	F	B	F	B	F
1	E	D	E	D	B	S
2	B	S	C	G	E	D
3	C	G	B	S	C	G

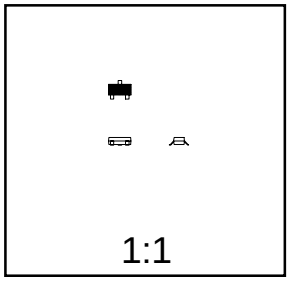


SOT-23 Package Dimensions

FAIRCHILD SEMICONDUCTOR™

SOT-23 (FS PKG Code 49)

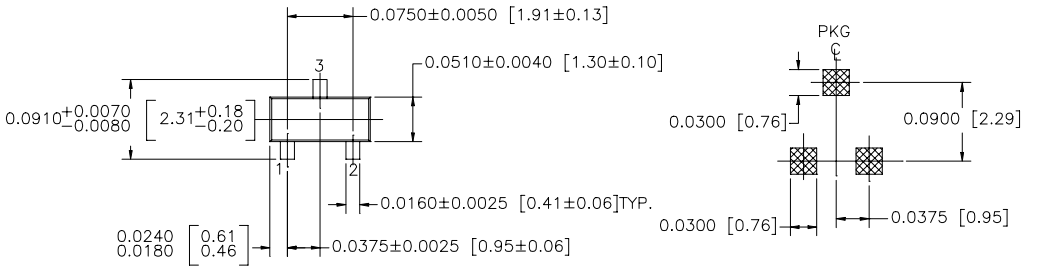


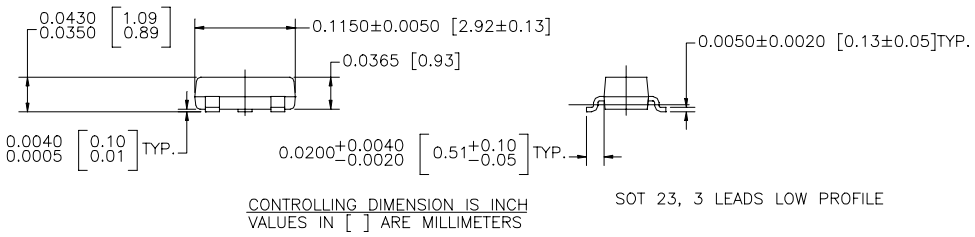


Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0082





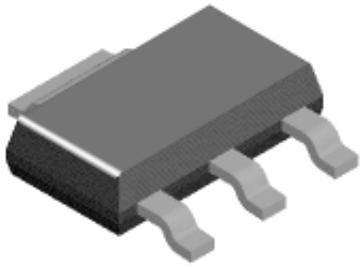
NOTE : UNLESS OTHERWISE SPECIFIED

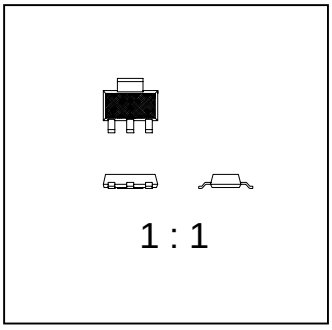
1. STANDARD LEAD FINISH 150 MICROINCHES / 3.81 MICROMETERS MINIMUM TIN / LEAD (SOLDER) ON ALLOY 42
2. REFERENCE JEDEC REGISTRATION TO−236, VARIATION AB, ISSUE G, DATED JUL 1993

SOT-223 Package Dimensions

FAIRCHILD SEMICONDUCTOR™

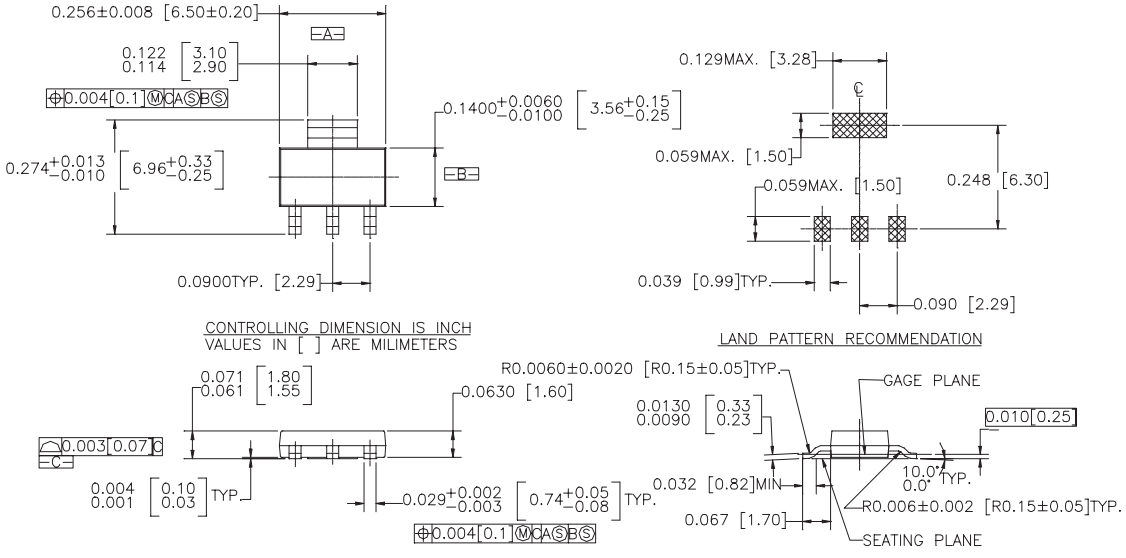
SOT-223 (FS PKG Code 47)





Scale 1:1 on letter size paper

Part Weight per unit (gram): 0.1246



NOTES : UNLESS OTHERWISE SPECIFIED
1. STANDARD LEAD FINISH TO BE 150 MICROINCHES/ 3.81 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.
2. REFERENCE JEDEC REGISTRATION TO−261, VARIATION AA, ISSUE A, DATED JAN 1990

SOT223, 4 LEADS

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FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

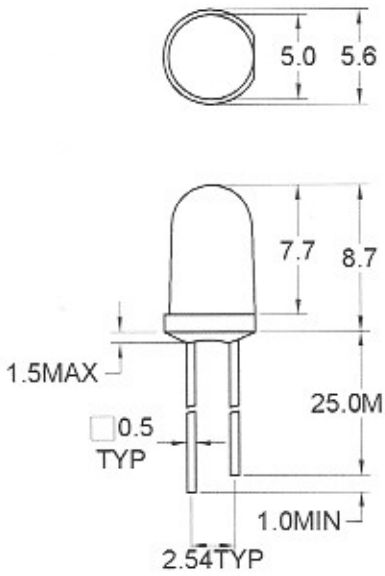
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

LIGITEK

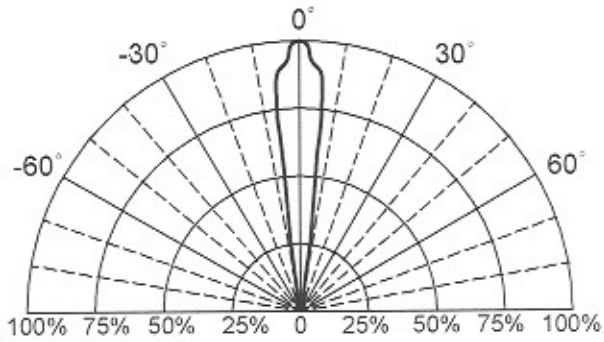
SUPER BRIGHT ROUND TYPE LED LAMPS **LVX3833H SERIES**

Package Dimension



Note:1.All dimension are in millimeter tolerance is ± 0.25mm unless otherwise noted
2.Specifications are subject to change without notice

Directivity Radiation



• Part Selection And Application Information (Ratings At 25℃ Ambient)

PART NO	MATERIAL	COLOR		Dominant wave length λDnm	Spectral halfwidth △λ nm	Forward voltage @20mA(v)		Luminous intensity @20mA(mcd)		Viewing angle 2θ1/2 (deg)
		Emitted	Lens			Min.	Max.	Min.	Typ.	
LUR3833H	AlGaInP/GaP	Red	Water Clear	630	20	1.7	2.6	4000	7700	12
LUY3833H	AlGaInP/GaP	Yellow	Water Clear	590	20	1.7	2.6	2700	5000	12

• Absolute Maximun Rating (Ta=25℃)

PARAMETER	RED	GREEN	YELLOW	ORANGE	UNIT	REMARK
	UR(H)		UY(H)			
Forward Current	50		50		mA	
Peak Forward Current Duty 1/10@10KHz	100		100		mA	
Power Dissipation	130		130		mW	
Reverse Current @5v	10		10		μA	
Operating Temperature	-40℃ TO +85℃					
Storage Temperature	-40℃ TO +100℃					

Lead Soldering Temperature 260℃ For 5 Seconds(2.0mm From Body)

LEDTECH ELECTRONICS CORP.

Ledtech Electronics Corp.
(USA Sales Office)
19209 Parthenia St. Ste D
Northridge, CA 91324
(Ph) 818-701-7240
(Fax) 818-701-7217

SPECIFICATION

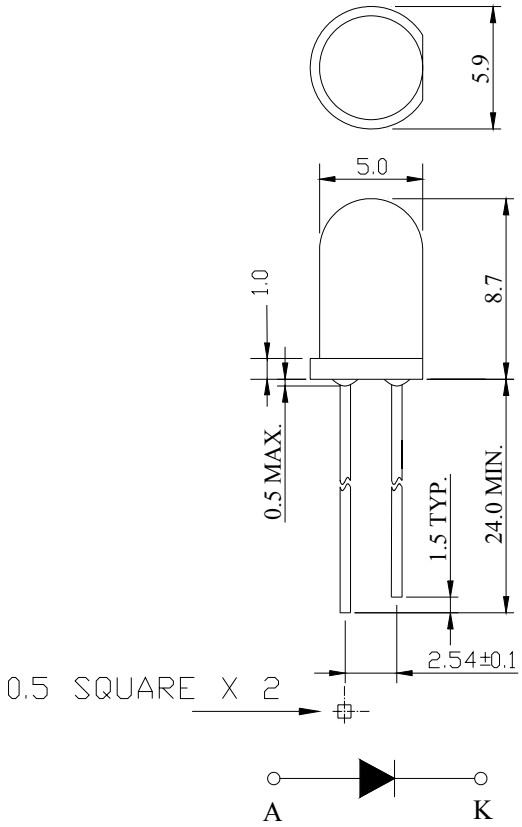
PART NO. : UT1813-83-UJE1-P22-TAA

5.0mm ROUND LED LAMP

Approved by	Checked by	Prepared by
Sam	*Yang*	*Min Bao*

Description

This hyper red lamp is made with AlGaInP/GaAs chip and water clear epoxy resin.



Notes:

1. ALL DIMENSIONS ARE IN mm.
2. TOLERANCE IS ±0.25mm UNLESS OTHERWISE NOTED.

Description

Part No.	LED Chip		Lens Color
	Material	Emitting Color	
UT1813-83-UJE1-P22-TAA	AlGaInP/GaAs	Hyper red	Water clear

Absolute Maximum Ratings at Ta=25℃

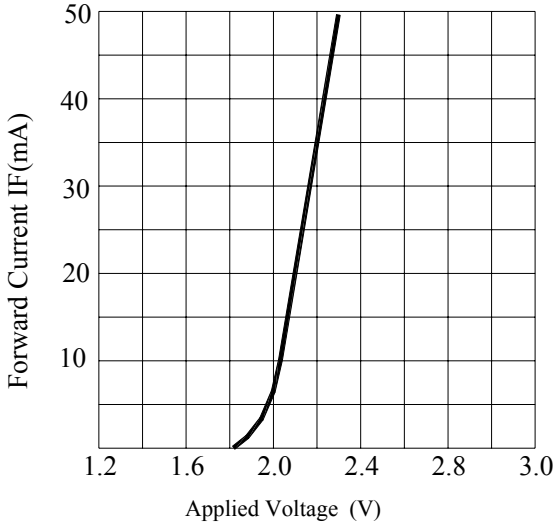
Parameter	Symbol	Rating	Unit
Power Dissipation	PD	75	mW
Reverse Voltage	VR	5	V
D.C. Forward Current	If	30	mA
Reverse (Leakage) Current	Ir	100	μA
Peak Current(1/10Duty Cycle,0.1ms Pulse Width.)	If(Peak)	100	mA
Operating Temperature Range	Topr.	-25 to +85	℃
Storage Temperature Range	Tstg.	-40 to +100	℃
Lead Soldering Temp.(1.6mm from body) for 5 seconds	Tsol.	260	℃
Electrostatic discharge	ESD.	300	V

Electrical and Optical Characteristics:

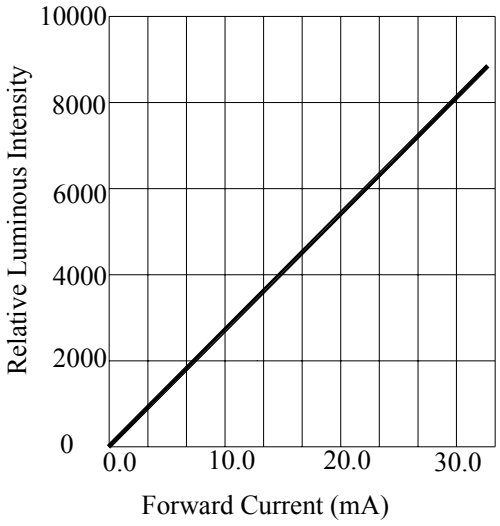
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Luminous Intensity	Iv	If=20mA	3000	5500		mcd
Forward Voltage	Vf	If=20mA		2.1	2.5	V
Peak Wavelength	λP	If=20mA		632		nm
Dominant Wavelength	λD	If=20mA		625		nm
Reverse (Leakage) Current	Ir	Vr=5V			100	μA
Viewing Angle	2 θ 1/2	If=20mA		25		deg
Spectrum Line Halfwidth	Δλ	If=20mA		20		nm

1. NOTE: THE DATAS TESTED BY IS TESTER
2. Customer's special requirements are also welcome.

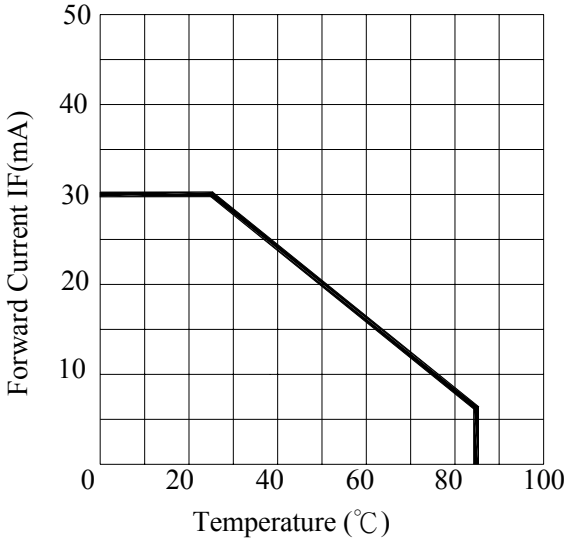
Typical Electrical / Optical Characteristics Curves :



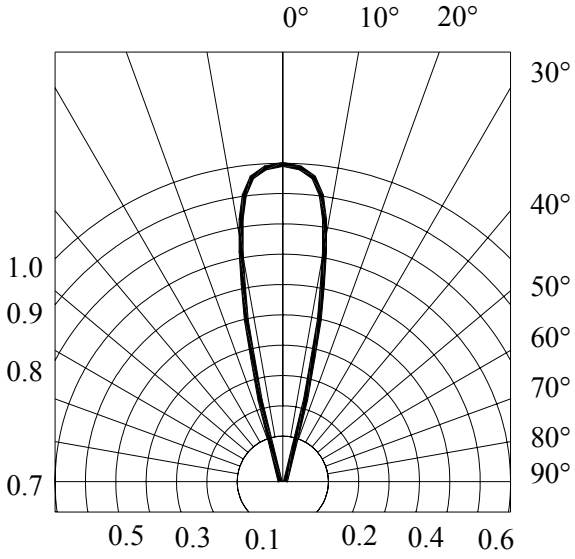
FORWARD CURRENT VS.APPLIED VOLTAGE



FORWARD CURRENT VS. LUMINOUS INTENSITY



FORWARD CURRENT VS. AMBIENT TEMPERATURE



RADIATION DIAGRAM

Precautions:

TAKE NOTE OF THE FOLLOWING IN USE OF LED

1. Temperature in use

   Since the light generated inside the LED needs to be emitted to outside efficiently, a resin with high light transparency is used; therefore, additives to improve the heat resistance or moisture resistance (silica gel , etc) which are used for semiconductor products such as transistors cannot be added to the resin.

   Consequently, the heat resistant ability of the resin used for LED is usually low; therefore, please be careful on the following during use.

   Avoid applying external force, stress, and excessive vibration to the resins and terminals at high temperature. The glass transition temperature of epoxy resin used for the LED is approximately 120-130°C.

   At a temperature exceeding this limit, the coefficient of liner expansion of the resin doubles or more compared to that at normal temperature and the resin is softened.

   If external force or stress is applied at that time, it may cause a wire rupture.

2. Soldering

   Please be careful on the following at soldering.

   After soldering, avoided applying external force, stress, and excessive vibration until the products go to cooling process (normal temperature), <Same for products with terminal leads>

   (1) Soldering measurements:

   Distance between melted solder side to bottom of resin shall be 1.6mm or longer.

   (2) Solder dip: Preheat: 90°C max. (Backside of PCB), Within 60 seconds

   Solder bath: 260±5°C (Solder temperature), Within 5 seconds

   (3) Soldering iron : 350°C max. (Temperature of soldering iron tip), Within 3 seconds

3. Insertion

   Pitch of the LED leads and pitch of mounting holes need to be same

4. Others

   Since the heat resistant ability of the LED resin is low, SMD components are used on the same PCB, please mount the LED after adhesive baking process for SMD components. In case adhesive baking is done after LED lamp insertion due to a production process reason, make sure not to apply external force, stress, and excessive vibration to the LED and follow the conditions below.

   Baking temperature: 120°C max. Baking time: Within 60 seconds

   If soldering is done sequentially after the adhesive baking, please perform the soldering after cooling down the LED to normal temperature.

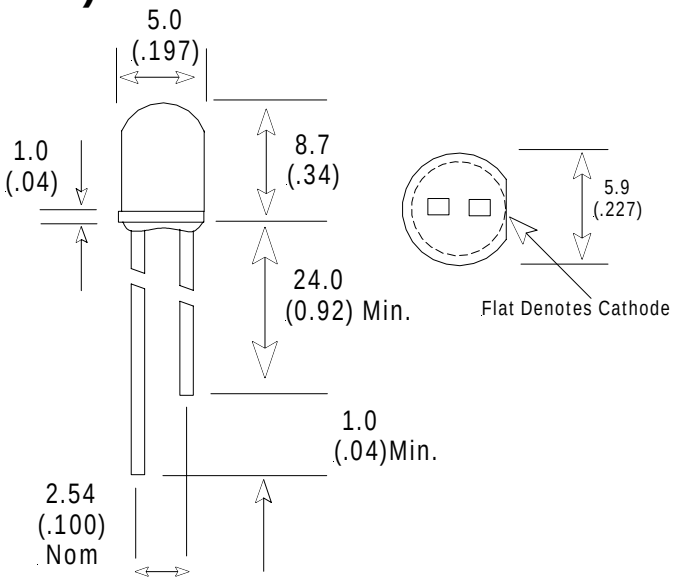
MCD Electronics Incorporated

Jameco Part Number 183222

Innovative Solutions With Light

MCDL-513SBC4 (5MM 470nm Blue 25°)

Lens Color: **Water Clear**
Lens Dimension: **5 mm**



Absolute Maximum Ratings At Ta = 25° C

Parameter	Max		Unit
DC Forward Current (mA)	**20**		**mA**
Reverse Voltage	**5**		**V**
Power Dissipation (mW)	**200**		**mW**
Continuous forward Current (mW)	**100**		**mW**
Peak Forward Current, tw ,=1 msec. Duty ,= 1/20	**500**		**mA**
Operation Temperature (°C)	**-40° -**	**+85°**	
Storage Temperature (°C)	**-40°**	**+100°**	
Solder DIP (5 seconds, 1.6 mm from body) Temperature	**260**	**± 5°C**	

Electrical Characteristics At Ta= 25°C

Symbol	Parameter	Test Cond.	Min.	Typ.	Max.	Unit
V_F	Forward Voltage	I_F = 20mA	3.20	3.60	4.30	V
I_R	Reverse Current	V_R=5V	**	**	10	µA

Part Number	Emitted Color		Peak Wavelength λ PEAK	Viewing Angle 2θ Degrees	I_V (I_F = 20mA) MCD		
					Min	Typ	Max
MCDL-513SBC4	InGaN	Blue	470	25	2,000	3,000	3,500

Notes:
1. All Dimensions are in millimeters (inches).
2. Tolerance is ± 0.25mm (0.010") unless otherwise specified.
3. Protruded resin under flange is 1.5mm (0.059") max.
4. Lead spacing is measured where the leads emerge from the package.

LEDTECH ELECTRONICS CORP.

Ledtech Electronics Corp.
(USA Sales Office)
19209 Parthenia St. Ste D
Northridge, CA 91324
(Ph) 818-701-7240
(Fax) 818-701-7217

SPECIFICATION

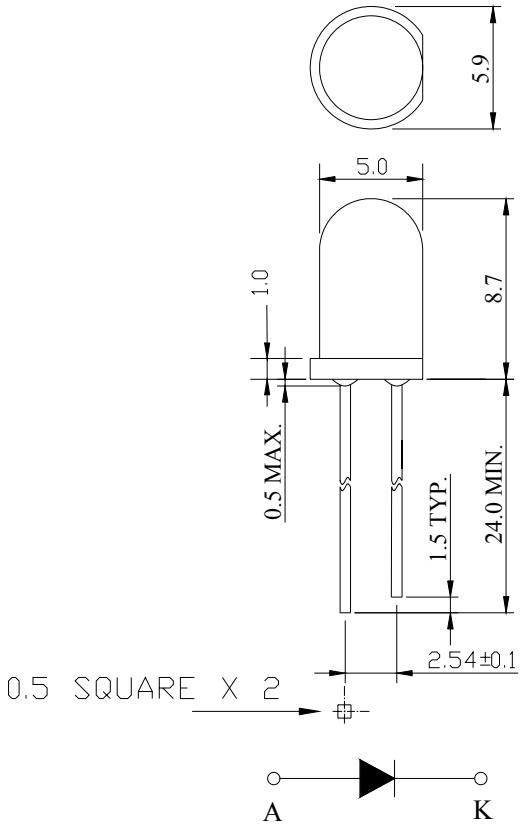
PART NO. : UT1813-83-UJE1-P22-TAA

5.0mm ROUND LED LAMP

Approved by	Checked by	Prepared by
Sam	*Yang*	*Min Bao*

Description

This hyper red lamp is made with AlGaInP/GaAs chip and water clear epoxy resin.



Notes:

1. ALL DIMENSIONS ARE IN mm.
2. TOLERANCE IS ±0.25mm UNLESS OTHERWISE NOTED.

Description

Part No.	LED Chip		Lens Color
	Material	Emitting Color	
UT1813-83-UJE1-P22-TAA	AlGaInP/GaAs	Hyper red	Water clear

Absolute Maximum Ratings at Ta=25℃

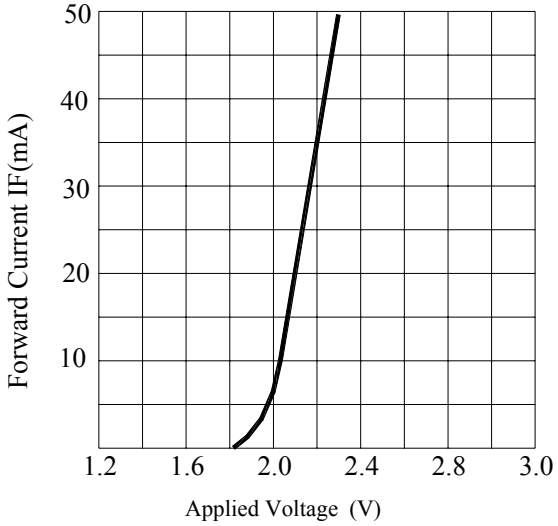
Parameter	Symbol	Rating	Unit
Power Dissipation	PD	75	mW
Reverse Voltage	VR	5	V
D.C. Forward Current	If	30	mA
Reverse (Leakage) Current	Ir	100	μA
Peak Current(1/10Duty Cycle,0.1ms Pulse Width.)	If(Peak)	100	mA
Operating Temperature Range	Topr.	-25 to +85	℃
Storage Temperature Range	Tstg.	-40 to +100	℃
Lead Soldering Temp.(1.6mm from body) for 5 seconds	Tsol.	260	℃
Electrostatic discharge	ESD.	300	V

Electrical and Optical Characteristics:

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Luminous Intensity	Iv	If=20mA	3000	5500		mcd
Forward Voltage	Vf	If=20mA		2.1	2.5	V
Peak Wavelength	λP	If=20mA		632		nm
Dominant Wavelength	λD	If=20mA		625		nm
Reverse (Leakage) Current	Ir	Vr=5V			100	μA
Viewing Angle	2 θ 1/2	If=20mA		25		deg
Spectrum Line Halfwidth	Δλ	If=20mA		20		nm

1. NOTE: THE DATAS TESTED BY IS TESTER
2. Customer's special requirements are also welcome.

Typical Electrical / Optical Characteristics Curves :



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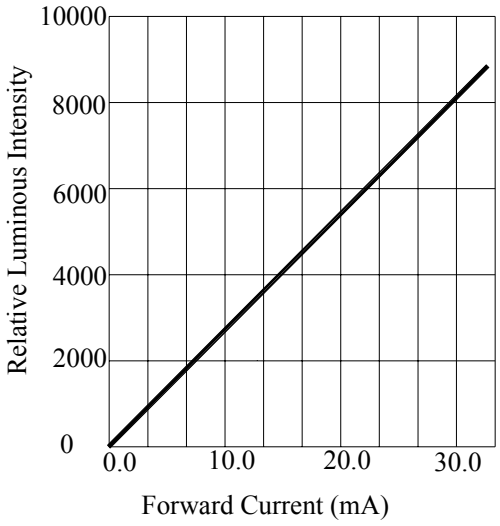

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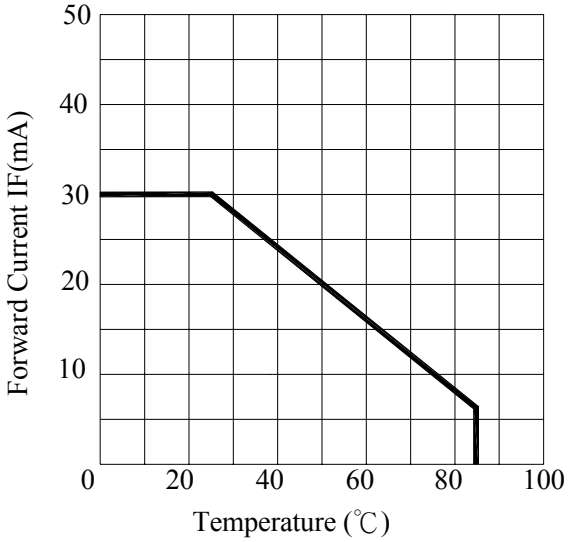
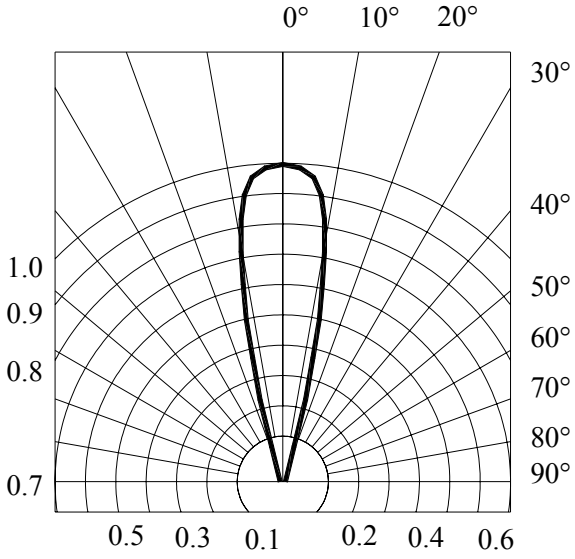


FORWARD CURRENT VS. AMBIENT TEMPERATURE



RADIATION DIAGRAM

Precautions:

TAKE NOTE OF THE FOLLOWING IN USE OF LED

1. Temperature in use

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