

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES SEPEMBER 7, 2016 DATA SHEET

General Description

The IDT5T9302I 2.5V differential clock buffer is a user-selectable differential input to two LVDS outputs. The fanout from a differential input to two LVDS outputs reduces loading on the preceding driver and provides an efficient clock distribution network. The IDT5T9302I can act as a translator from a differential HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input to LVDS outputs. A single-ended 3.3V / 2.5V LVTTL input can also be used to translate to LVDS outputs. The redundant input capability allows for an asynchronous change-over from a primary clock source to a secondary clock source. Selectable reference inputs are controlled by SEL.

The IDT5T9302I outputs can be asynchronously enabled/ disabled. When disabled, the outputs will drive to the value selected by the G_L pin. Multiple power and grounds reduce noise.

Applications

- Clock distribution

Features

- Guaranteed low skew: 50ps (maximum)
 - Very low duty cycle distortion: 125ps (maximum)
 - High speed propagation delay: 1.5ns (maximum)
 - Up to 450MHz operation
 - Selectable inputs
 - Hot insertable and over-voltage tolerant inputs
 - 3.3V/2.5V LVTTL, HSTL eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML or LVDS input interface
 - Selectable differential inputs to two LVDS outputs
 - Power-down mode
 - 2.5V V_{DD}
 - -40°C to 85°C ambient operating temperature
 - Available in Lead-free (RoHS 6) package
 - **Not Recommended For New Designs**
 - **For functional replacement part use 8SLVP1102**

Pin Assignment

GND	1	20	A2
nPD	2	19	nA2
nc	3	18	GND
V _{DD}	4	17	V _{DD}
nQ1	5	16	nQ2
Q1	6	15	Q2
V _{DD}	7	14	V _{DD}
SEL	8	13	GL
nG	9	12	nA1
GND	10	11	A1

20-Lead TSSOP, E-Pad
4.4mm x 6.5mm x 0.925mm
package body
G Package
Top View

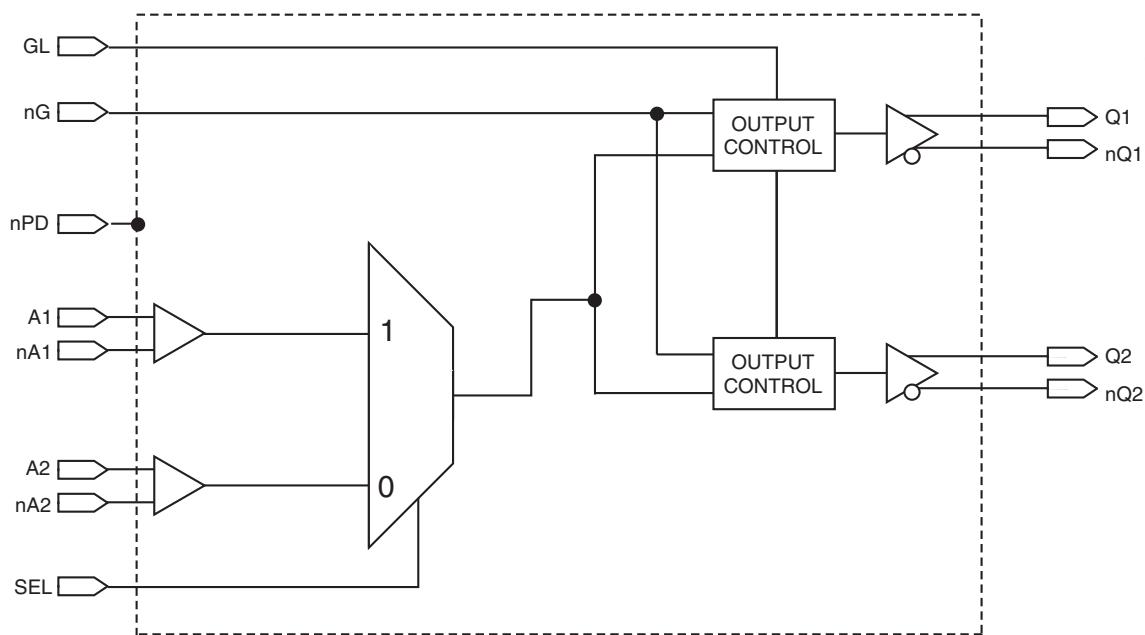


Table 1. Pin Descriptions

Name	Type	Description
A[1:2]	Input	Adjustable ^(1, 4) Clock input. A[1:2] is the "true" side of the differential clock input.
nA[1:2]	Input	Adjustable ^(1, 4) Complementary clock inputs. nA[1:2] is the complementary side of A[1:2]. For LVTTL single-ended operation, nA[1:2] should be set to the desired toggle voltage for A[1:2]: 3.3V LVTTL VREF = 1650mV 2.5V LVTTL VREF = 1250mV
nG	Input	LVTTL Gate control for differential outputs Q1, nQ1 and Q2, nQ2. When nG is LOW, the differential outputs are active. When nG is HIGH, the differential outputs are asynchronously driven to the level designated by GL ⁽²⁾ . See Table 3A.
GL	Input	LVTTL Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH. See Table 3A.
Q[1:2]	Output	LVDS Clock outputs.
nQ[1:2]	Output	LVDS Complementary clock outputs.
SEL	Input	LVTTL Reference clock select. When LOW, selects A2 and nA2. When HIGH, selects A1 and nA1. See Table 3B.
nPD	Input	LVTTL Power-down control. Shuts off entire chip. If LOW, the device goes into low power mode. Inputs and outputs are disabled. Both "true" and "complementary" outputs will pull to VDD. Set HIGH for normal operation. ⁽³⁾
V _{DD}	Power	Power supply for the device core and inputs.
GND	Power	Power supply return for all power.
nc	Unused	No connect; recommended to connect to GND.

NOTES:

1. Inputs are capable of translating the following interface standards:
Single-ended 3.3V and 2.5V LVTTL levels
Differential HSTL and eHSTL levels
Differential LVEPECL (2.5V) and LVPECL (3.3V) levels
Differential LVDS levels
Differential CML levels
2. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.
3. It is recommended that the outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting nPD.
4. The user must take precautions with any differential input interface standard being used in order to prevent instability when there is no input signal.

Table 2. Pin Characteristics (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			3		pF

NOTE: This parameter is measured at characterization but not tested.

Function Tables

Table 3A. Gate Control Output Table

Control Output		Outputs	
GL	nG	Q[1:2]	nQ[1:2]
0	0	Toggling	Toggling
0	1	LOW	HIGH
1	0	Toggling	Toggling
1	1	HIGH	LOW

Table 3B. Input Selection Table

Selection SEL pin	Inputs
0	A2, nA2
1	A1, nA1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Power Supply Voltage, V _{DD}	-0.5V to +3.6V
Input Voltage, V _I	-0.5V to +3.6V
Output Voltage, V _O Not to exceed 3.6V	-0.5 to V _{DD} +0.5V
Storage Temperature, T _{STG}	-65°C to 150°C
Junction Temperature, T _J	150°C

Recommended Operating Range

Symbol	Description	Minimum	Typical	Maximum	Units
T _A	Ambient Operating Temperature	-40	+25	+85	°C
V _{DD}	Internal Power Supply Voltage	2.3	2.5	2.7	V

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics⁽¹⁾, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical ⁽²⁾	Maximum	Units
I_{DDQ}	Quiescent V_{DD} Power Supply Current	$V_{DD} = \text{Max.}$, All Input Clocks = LOW ⁽²⁾ ; Outputs enabled			240	mA
I_{TOT}	Total Power V_{DD} Supply Current	$V_{DD} = 2.7\text{V}$; $F_{\text{REFERENCE}} = 450\text{MHz}$			250	mA
I_{nPD}	Total Power Down Supply Current	$nPD = \text{LOW}$			5	mA

NOTE 1: These power consumption characteristics are for all the valid input interfaces and cover the worst case conditions.

NOTE 2: The true input is held LOW and the complementary input is held HIGH.

Table 4B. LVCMS/LVTTL DC Characteristics⁽¹⁾, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical ⁽²⁾	Maximum	Units
I_{IH}	Input High Current	$V_{DD} = 2.7\text{V}$			± 5	μA
I_{IL}	Input Low Current	$V_{DD} = 2.7\text{V}$			± 5	μA
V_{IK}	Clamp Diode Voltage	$V_{DD} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		-0.7	-1.2	V
V_{IN}	DC Input Voltage		-0.3		3.6	V
V_{IH}	DC Input High Voltage		1.7			V
V_{IL}	DC Input Low Voltage				0.7	V
V_{THI}	DC Input Threshold Crossing Voltage			$V_{DD}/2$		V
V_{REF}	Single-Ended Reference Voltage ⁽³⁾	3.3V LVTTL		1.65		V
		2.5V LVTTL		1.25		V

NOTE 1: See *Recommended Operating Range* table.

NOTE 2: Typical values are at $V_{DD} = 2.5\text{V}$, $+25^\circ\text{C}$ ambient.

NOTE 3: For A[1:2] single-ended operation, nA[1:2] is tied to a DC reference voltage.

Table 4C. Differential DC Characteristics⁽¹⁾, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical ⁽²⁾	Maximum	Units
I_{IH}	Input High Current	$V_{DD} = 2.7\text{V}$			± 5	μA
I_{IL}	Input Low Current	$V_{DD} = 2.7\text{V}$			± 5	μA
V_{IK}	Clamp Diode Voltage	$V_{DD} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		-0.7	-1.2	V
V_{IN}	DC Input Voltage		-0.3		3.6	V
V_{DIF}	DC Differential Voltage ⁽³⁾		0.1			V
V_{CM}	DC Common Mode Input Voltage		0.05		V_{DD}	V

NOTE 1: See *Recommended Operating Range* table.

NOTE 2: Typical values are at $V_{DD} = 2.5\text{V}$, $+25^\circ\text{C}$ ambient.

NOTE 3: V_{DIF} specifies the minimum input differential voltage ($V_{TR} - V_{CP}$) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.

NOTE 4: V_{CM} specifies the maximum allowable range of $(V_{TR} + V_{CP})/2$.

Table 4D. LVDS DC Characteristics⁽¹⁾, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical ⁽²⁾	Maximum	Units
V _{OT(+)}	Differential Output Voltage for the True Binary State		247		454	mV
V _{OT(-)}	Differential Output Voltage for the False Binary State		247		454	mV
ΔV _{OT}	Change in V _{OT} Between Complementary Output States				50	mV
V _{OS}	Output Common Mode Voltage (Offset Voltage)		1.125	1.2	1.375	V
ΔV _{OS}	Change in V _{OS} Between Complementary Output States				50	mV
I _{OS}	Outputs Short Circuit Current	V _{OUT+} and V _{OUT-} = 0V		12	24	mA
I _{OSD}	Differential Outputs Short Circuit Current	V _{OUT+} = V _{OUT-}		6	12	mA

NOTE 1: See *Recommended Operating Range* table.NOTE 2: Typical values are at V_{DD} = 2.5V, +25°C ambient.

AC Electrical Characteristics

Table 5A. HSTL Differential Input AC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter	Value	Units
V _{DIF}	Input Signal Swing ⁽¹⁾	1	V
V _X	Differential Input Signal Crossing Point ⁽²⁾	750	mV
D _H	Duty Cycle	50	%
V _{THI}	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
t _R / t _F	Input Signal Edge Rate ⁽⁴⁾	2	V/ns

NOTE 1: The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.NOTE 2: A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.

NOTE 3: In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4: The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

Table 5B. eHSTL AC Differential Input Characteristics, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing ⁽¹⁾	1	V
V_X	Differential Input Signal Crossing Point ⁽²⁾	900	mV
D_H	Duty Cycle	50	%
V_{THI}	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
t_R / t_F	Input Signal Edge Rate ⁽⁴⁾	2	V/ns

NOTE 1: The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.

NOTE 2: A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.

NOTE 3: In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4: The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

Table 5C. LVEPECL (2.5V) and LVPECL (3.3V) Differential Input AC Characteristics, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Maximum	Units
V_{DIF}	Input Signal Swing ⁽¹⁾	732	mV
V_X	Differential Input Cross Point Voltage ⁽²⁾	1082	mV
		1880	mV
D_H	Duty Cycle	50	%
V_{THI}	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
t_R / t_F	Input Signal Edge Rate ⁽⁴⁾	2	V/ns

NOTE 1: The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.

NOTE 2: A 1082mV LVEPECL (2.5V) and 1880 LVPECL (3.3V) crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.

NOTE 3: In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4: The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

Table 5D. LVDS Differential Input AC Characteristics, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Maximum	Units
V_{DIF}	Input Signal Swing ⁽¹⁾	400	mV
V_X	Differential Input Cross Point Voltage ⁽²⁾	1.2	V
D_H	Duty Cycle	50	%
V_{THI}	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
t_R / t_F	Input Signal Edge Rate ⁽⁴⁾	2	V/ns

NOTE 1: The 400mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.

NOTE 2: A 1.2V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.

NOTE 3: In all cases, input waveform timing is marked at the differential cross-point of the input signals.

NOTE 4: The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

Table 5E. AC Differential Input Characteristics⁽¹⁾, T_A = -40°C to 85°C

Symbol	Parameter	Minimum	Typical	Maximum	Units
V _{DIF}	AC Differential Voltage ⁽²⁾	0.1		3.6	V
V _X	Differential Input Cross Point Voltage	0.05		V _{DD}	V
V _{CM}	Common Mode Input Voltage Range ⁽³⁾	0.05		V _{DD}	V
V _{IN}	Input Voltage	-0.3		3.6	V/ns

NOTE 1: The output will not change state until the inputs have crossed and the minimum differential voltage range defined by V_{DIF} has been met or exceeded.

NOTE 2: V_{DIF} specifies the minimum input voltage (V_{TR} – V_{CP}) required for switching where V_{TR} is the “true” input level and V_{CP} is the “complement” input level. The AC differential voltage must be achieved to guarantee switching to a new state.

NOTE 3: V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2.

Table 5E. AC Characteristics^(1,5), T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
t _{sk(o)}	Same Device Output Pin-to-Pin Skew ⁽²⁾				50	ps
t _{sk(p)}	Pulse Skew ⁽³⁾				125	ps
t _{sk(pp)}	Part-to-Part Skew ⁽⁴⁾				350	ps
t _{pLH}	Propagation Delay, Low-to-High	A[1:2]/nA[1:2] Crosspoint to Qx/nQx Crosspoint	1.35	1.35	1.5	ns
t _{pHL}	Propagation Delay, High-to-Low				1.5	ns
f _o	Output Frequency ⁽⁶⁾				450	MHz
t _{PGE}	Output Gate Enable Crossing V _{THI} -to-Qx/Qx Crosspoint				3.5	ns
t _{PGD}	Output Gate Enable Crossing V _{THI} -to-Qx/Qx Crosspoint Driven to Designated Level				3.5	ns
t _{PWRDN}	nPD Crossing V _{THI} -to-Qx = V _{DD} , Qx = V _{DD}				100	μS
t _{PWRUP}	Output Gate Disable Crossing V _{THI} to Qx/nQx Driven to Designated Level				100	μS

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: AC propagation measurements should not be taken within the first 100 cycles of startup.

NOTE 2: Skew measured between crosspoints of all differential output pairs under identical input and output interfaces, transitions and load conditions on any one device.

NOTE 3: Skew measured is the difference between propagation delay times t_{pHL} and t_{pLH} of any differential output pair under identical input and output interfaces, transitions and load conditions on any one device.

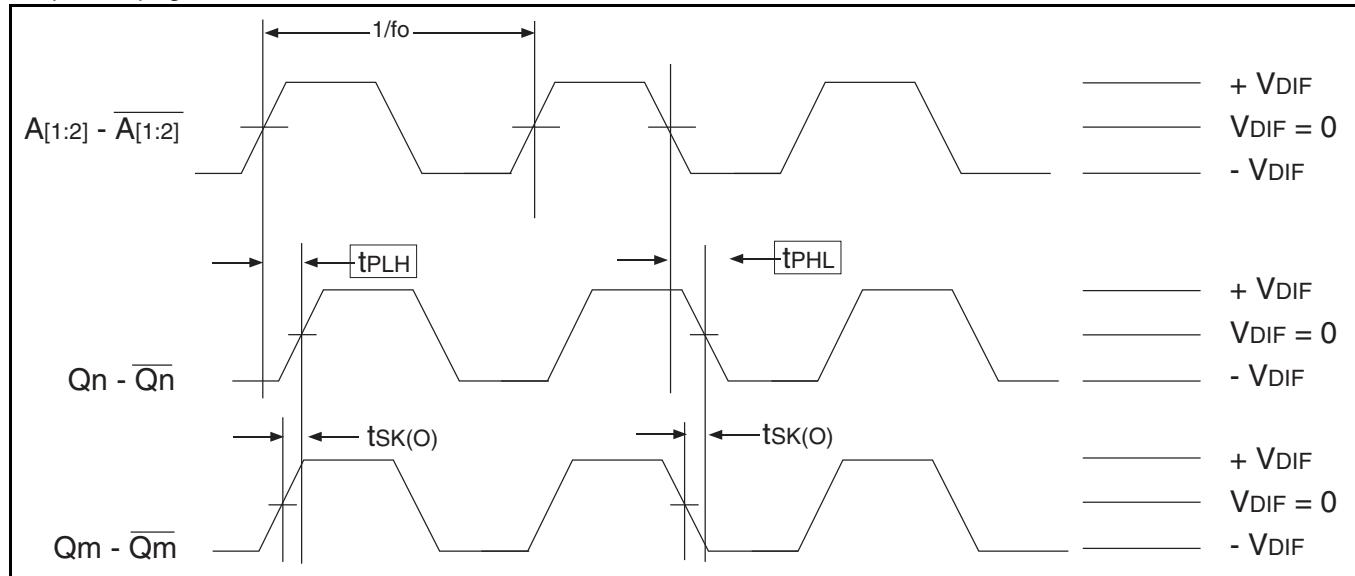
NOTE 4: Skew measured is the magnitude of the difference in propagation times between any single differential output pair of two devices, given identical transitions and load conditions at identical V_{DD} levels and temperature.

NOTE 5: All parameters are tested with a 50% input duty cycle.

NOTE 6: Guaranteed by design but not production tested.

Differential AC Timing Waveforms

Output Propagation and Skew Waveforms



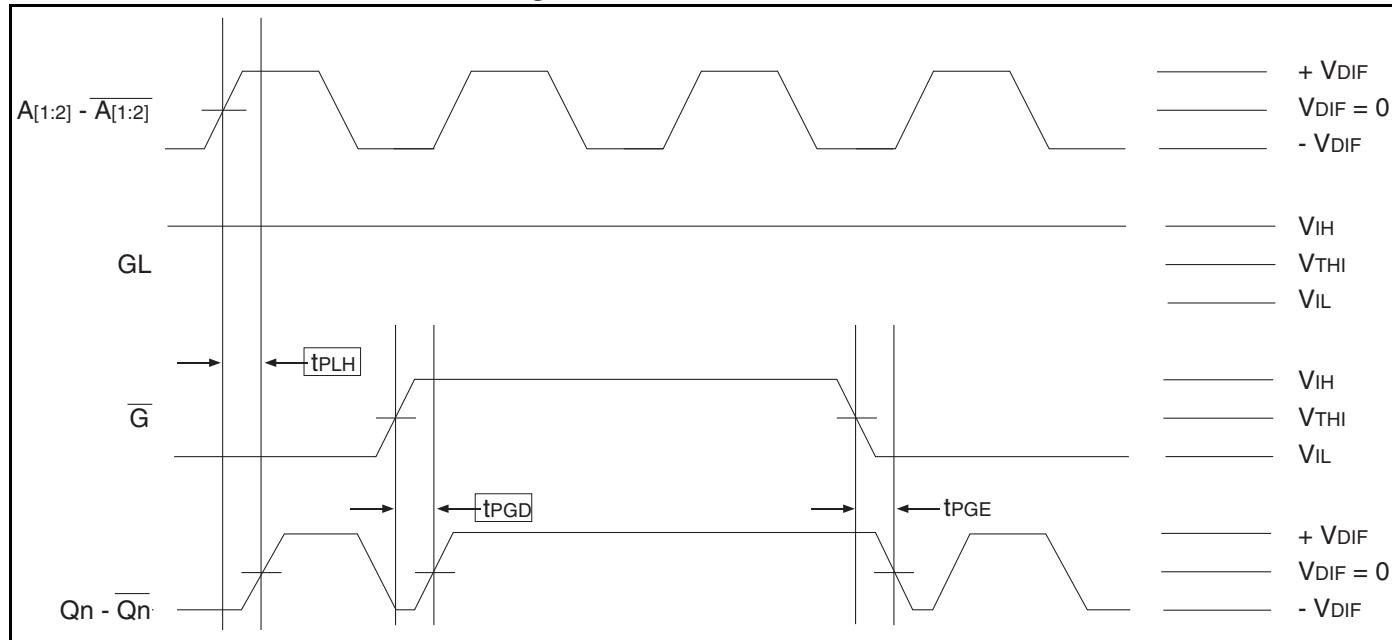
NOTE 1: Pulse skew is calculated using the following expression:

$$t_{SK(p)} = |t_{PHL} - t_{PLH}|$$

Note that the t_{PHL} and t_{PLH} shown above are not valid measurements for this calculation because they are not taken from the same pulse.

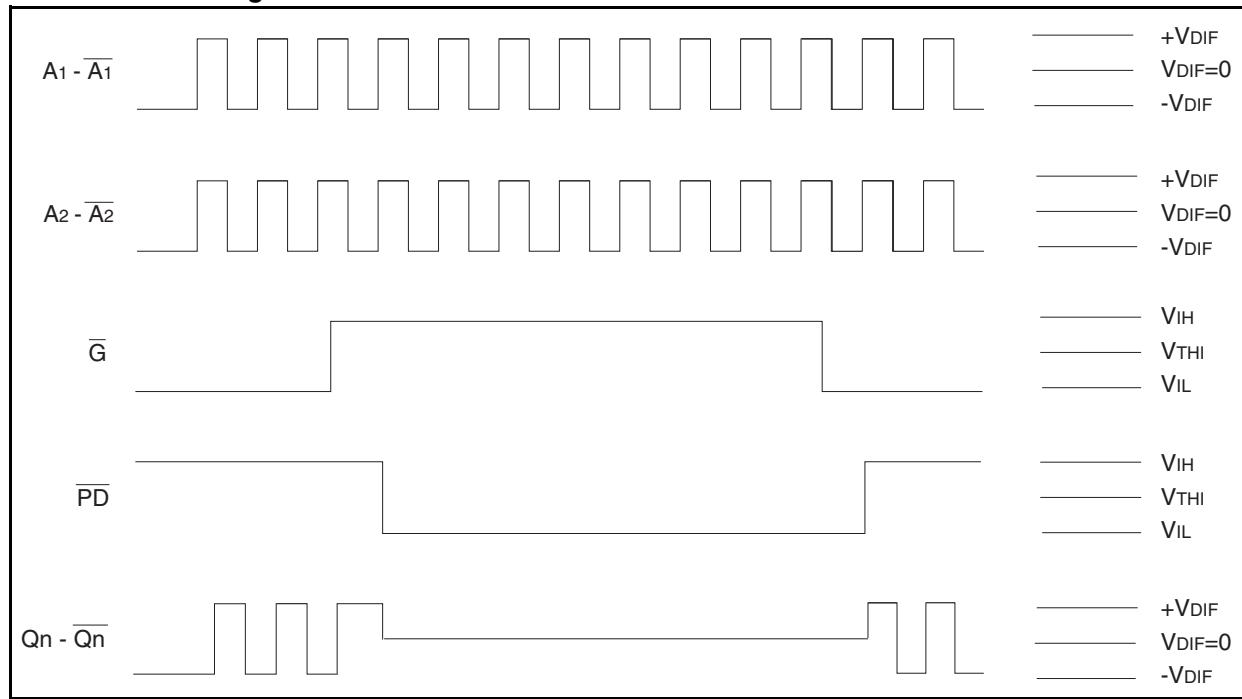
NOTE 2: AC propagation measurements should not be taken within the first 100 cycles of startup.

Differential Gate Disabled/Enable Showing Runt Pulse Generation



NOTE 1: As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time the nG signal to avoid this problem.

Power Down Timing

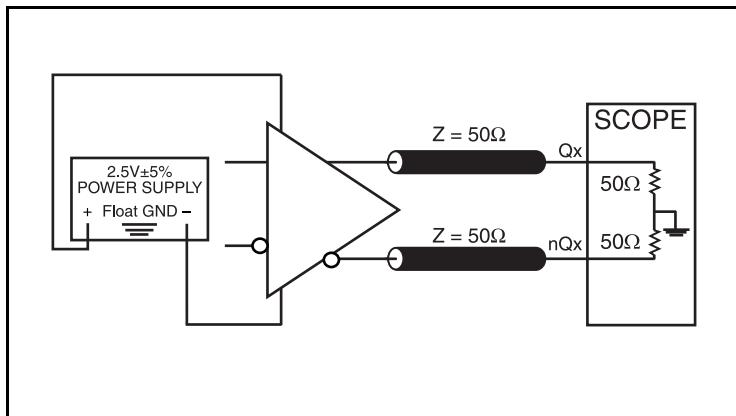


NOTE 1: It is recommended that outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting nPD.

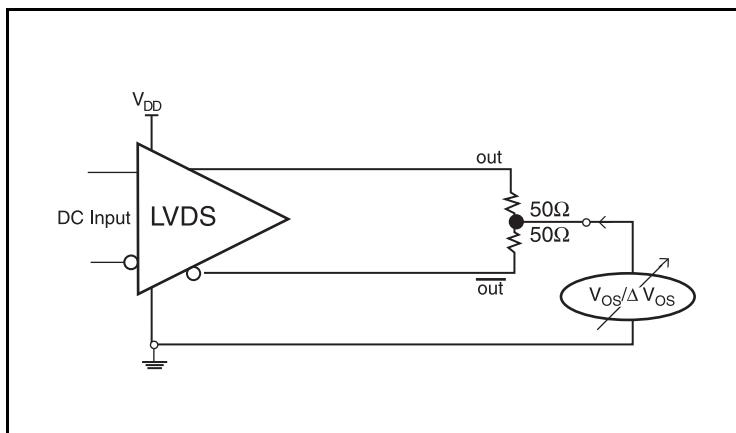
NOTE 2: The *Power Down Timing* diagram assumes that GL is HIGH.

NOTE 3: It should be noted that during power-down mode, the outputs are both pulled to V_{DD} . In the *Power Down Timing* diagram this is shown when Q_x/nQ_x goes to $V_{DIF} = 0$.

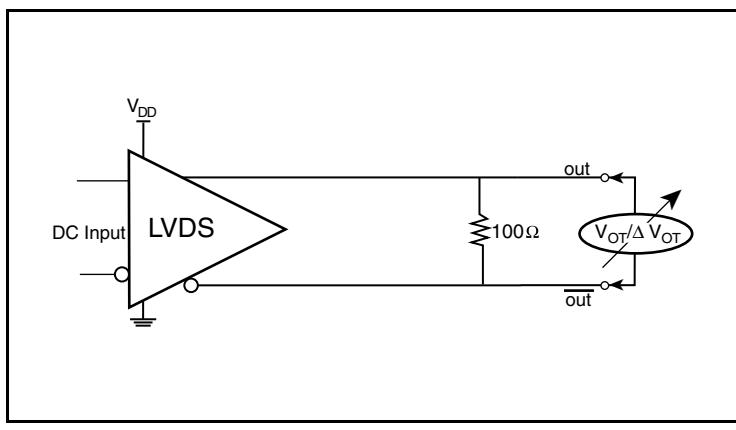
Parameter Measurement Information



LVDS Output Load AC Test Circuit



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 1*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

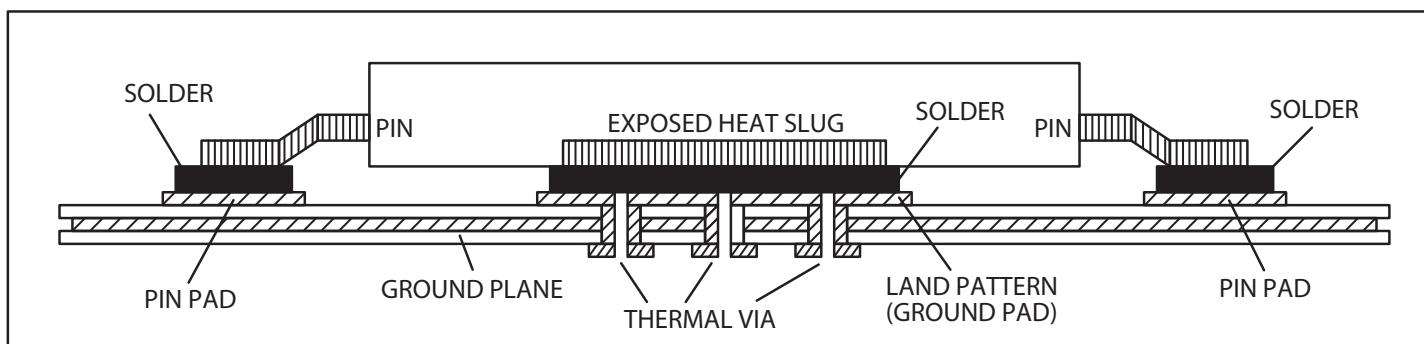


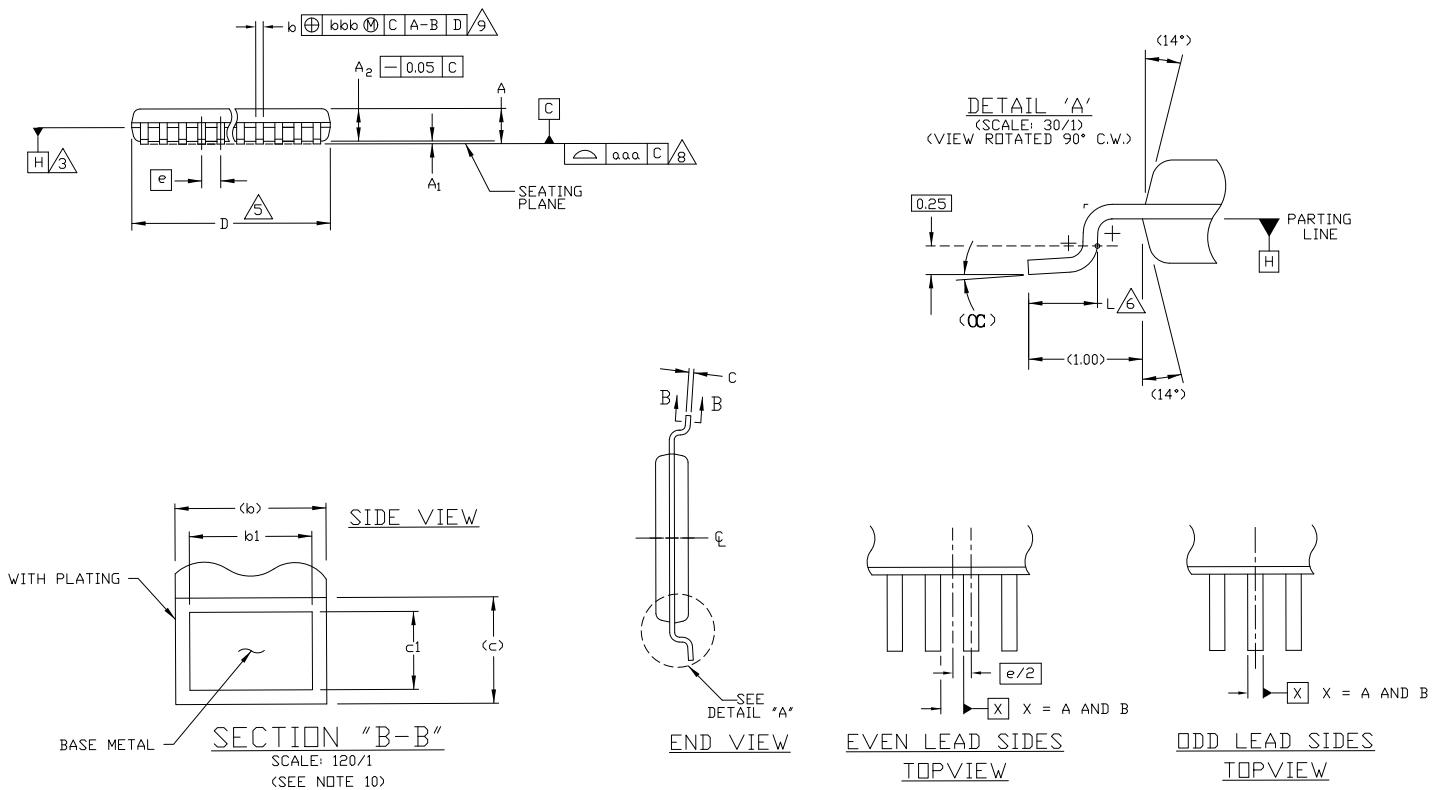
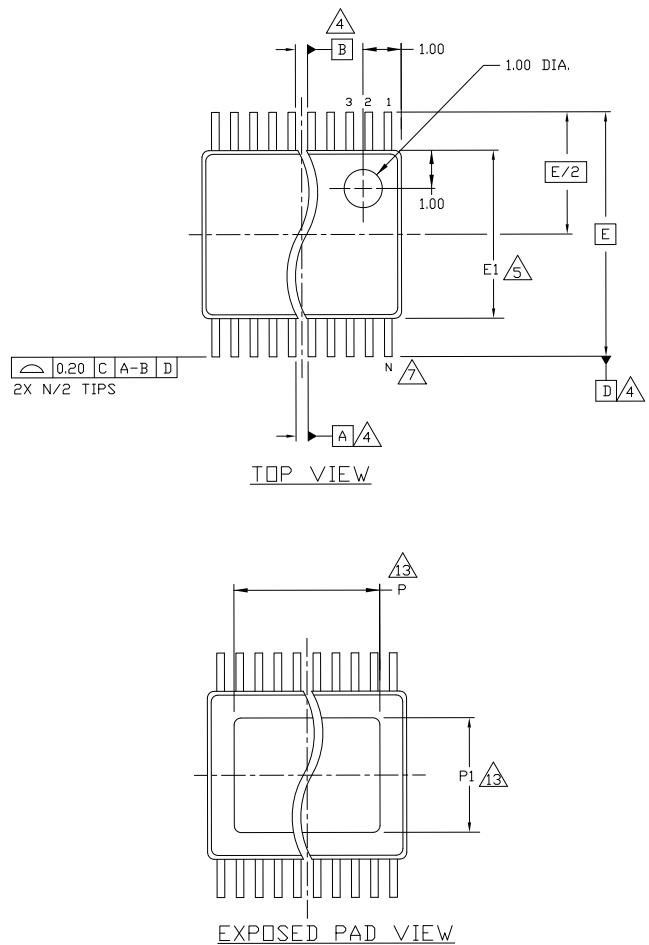
Figure 1. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Package Drawing and Dimensions

Table 7. Package Dimensions for 20 Lead TSSOP, E-Pad

All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N		20	
A			1.10
A1	0.5		0.15
A2	0.85	0.90	0.95
aaa		0.076	
b	0.19		0.30
b1	0.19	0.22	0.25
bbb		0.10	
c	0.09		0.20
c1	0.09	0.127	0.16
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
e	0.65 Basic		
E	6.40 Basic		
L	0.50	0.60	0.70
P			4.2
P1			3.0
cc	0°		8°

NOTE: Reference Document: IDT PSC-4284



Ordering Information

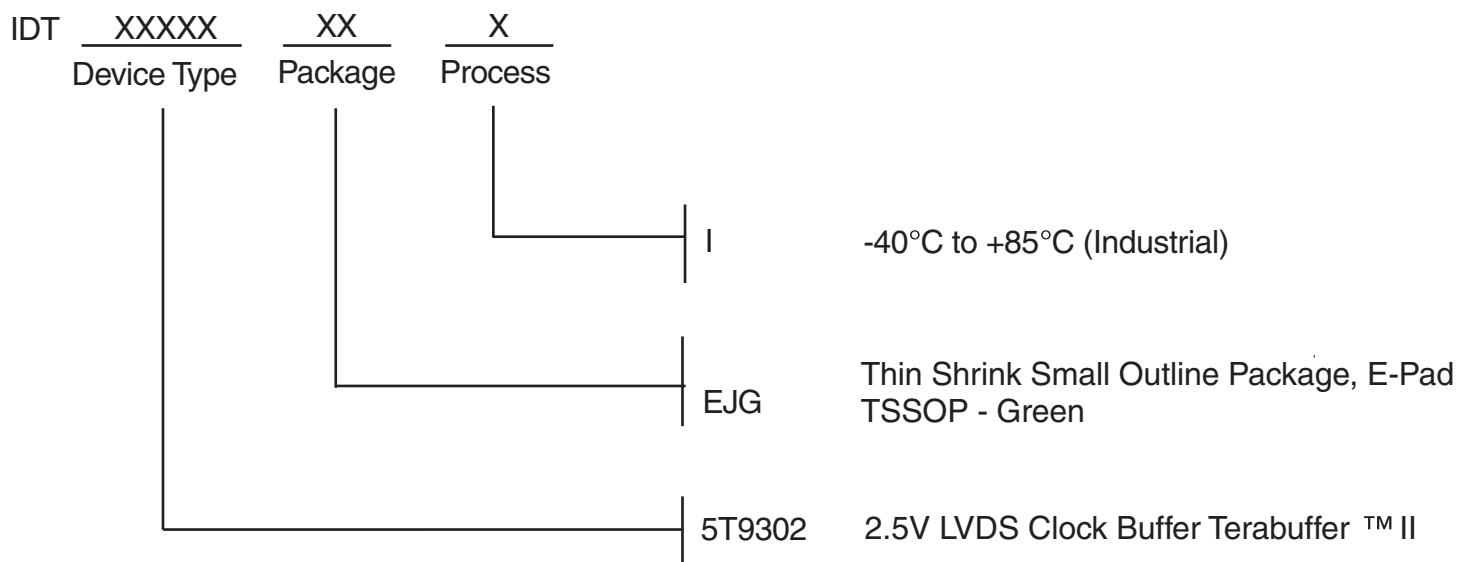


Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
5T9302EJGI	IDT5T9302EJGI	“Lead-Free” 20 Lead TSSOP, E-Pad	Tube	-40°C to 85°C
5T9302EJGI8	IDT5T9302EJGI	“Lead-Free” 20 Lead TSSOP, E-Pad	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T8	13	Ordering information - Removed leaded devices	12/16/14
A		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02.	3/10/16



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications, such as those requiring extended temperature ranges, high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Product specification subject to change without notice. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright ©2014 Integrated Device Technology, Inc.. All rights reserved.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[IDT \(Integrated Device Technology\):](#)

[5T9302EJGI](#) [5T9302EJGI8](#)