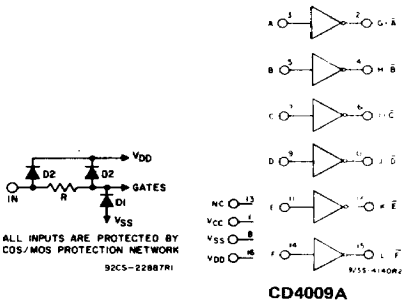
CMOS
Hex Buffers/Converters

Inverting Type: CD4009A
Non-Inverting Type: CD4010A

The RCA-CD4009A and CD4010A Hex Buffer/Converters may be used as COS/MOS to TTL or DTL logic-level converters or CMOS high sink-current drivers.
The CD4049A and CD4050A are preferred hex buffer replacements for the CD4009A and CD4010A, respectively, in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069B Hex Inverter is recommended.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



Features:

- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **High sink current for driving 2 TTL loads**
- **High-to-low level logic conversion**

Applications:

- **CMOS to DTL/TTL hex converter**
- **CMOS current "sink" or "source" driver**
- **CMOS high-to-low logic-level converter**
- **Multiplexer — 1 to 6 or 6 to 1**

Fig. 1 – Logic diagrams.

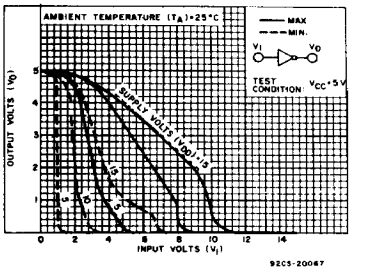


Fig. 2 – Minimum & maximum voltage transfer characteristics – CD4009A.

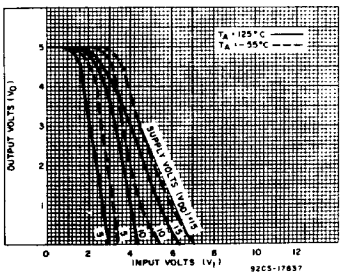


Fig. 3 – Typical voltage transfer characteristics as function of temp. – CD4009A.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range : V_{DD} , V_{CC})	3	12	V
Input Voltage Range (V_I)	V_{CC}*	12	V

* The CD4009 and CD4010 have high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{DD} \geq V_I \geq V_{CC}$.

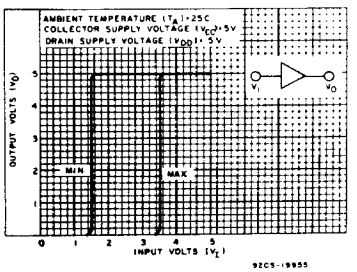


Fig. 4 – Minimum & maximum voltage transfer characteristics (V_{DD} = 5) – CD4010A.

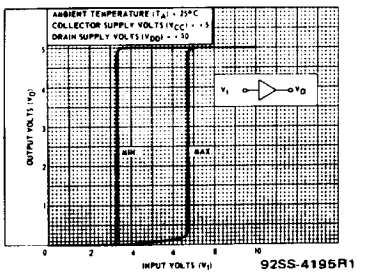


Fig. 5 – Minimum & maximum voltage transfer characteristics (V_{DD} = 10) – CD4010A.

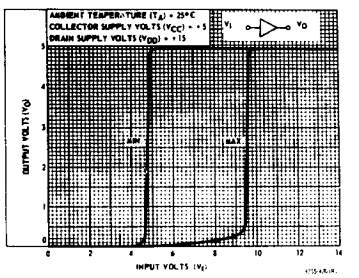


Fig. 6 – Minimum & maximum voltage transfer characteristics (V_{DD} = 15) – CD4010A.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{CC}* (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.3	0.01	0.3	20	3	0.03	3	42	μA
	–	–	10	0.5	0.01	0.5	30	5	0.05	5	70	
	–	–	15	10	0.02	10	100	50	0.5	50	500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL} CD4010A	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH} All Types	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Inputs Low, V_{NL} CD4009A	3.6	–	5	1 Min.; 1.5 Typ.								
	7.2	–	10	2 Min.; 3 Typ.								
Noise Margin: Inputs Low, V_{NML} CD4010A	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH} CD4010A	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current : N-Channel (Sink), I_DN Min.	0.4	–	5	3.75	4	3	2.1	3.6	4	3	2.4	mA
	0.5	–	10	10	10	8	5.6	9.6	10	8	6.4	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.31	-0.5	-0.25	-0.175	-0.3	-0.5	-0.25	-0.2	
	2.5	–	5	-1.85	-1.75	-1.25	-0.9	-1.5	-1.75	-1.25	-1	
	9.5	–	10	-0.9	-0.8	-0.6	-0.4	-0.72	-0.8	-0.6	-0.48	
Input Leakage Current, I_{IL},I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

* $V_{CC} = V_{DD}$

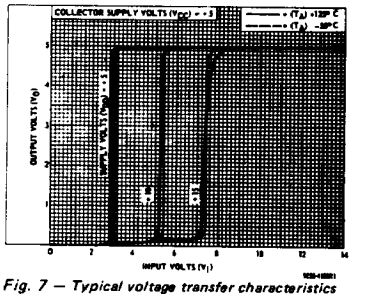


Fig. 7 — Typical voltage transfer characteristics as a function of temperature — CD4010A.

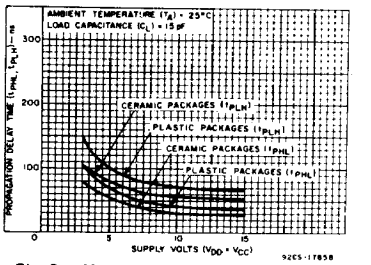


Fig. 8 — Maximum propagation delay time vs. V_{DD} — CD4010A.

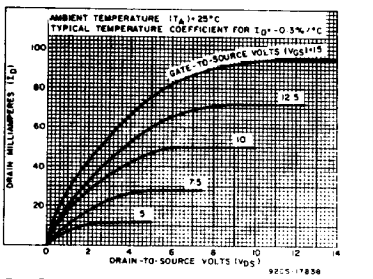


Fig. 9 — Typical n-channel drain characteristics.

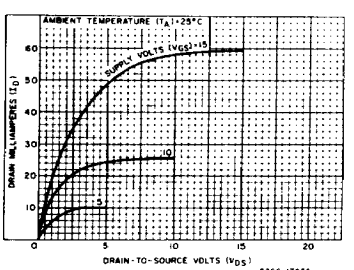


Fig. 10 — Minimum n-channel drain characteristics.

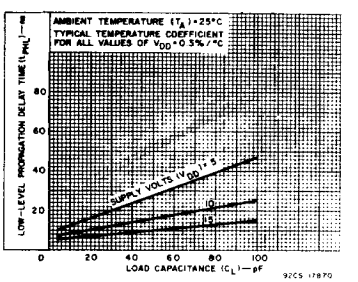


Fig. 11 — Typical high-to-low level propagation delay time vs. C_L.

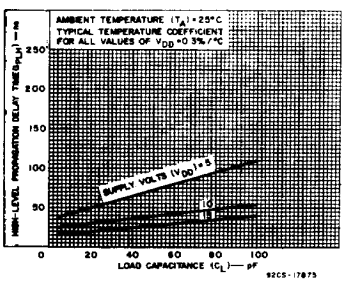


Fig. 12 — Typical low-to-high level propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

CHARACTERISTIC	CONDITION			LIMIT		UNITS
	V_{DD} (V)	V_I (V)	V_{CC} (V)	Typ.	Max.	
D, F, K, H Packages						
Propagation Delay Time: Low-to-High, t_{PLH}	5	5	5	50	80	ns
	10	10	10	25	55	
	10	10	5	15	30	
High-to-Low, t_{PHL}	5	5	5	15	55	
	10	10	10	10	30	
	10	10	5	10	25	
Transition Time: Low-to-High, t_{TLH}	5	5	5	80	125	ns
	10	10	10	50	100	
High-to-Low, t_{THL}	5	5	5	20	45	
	10	10	10	16	40	
Input Capacitance, C_I CD4009A	–	–	–	15	–	pF
CD4010A	–	–	–	5	–	
E Package						
Propagation Delay Time: Low-to-high, t_{PLH}	5	5	5	50	100	ns
	10	10	10	25	70	
	10	10	5	15	40	
High-to-Low, t_{PHL}	5	5	5	15	70	
	10	10	10	10	40	
	10	10	5	10	35	
Transition Time: Low-to-High, t_{PLH}	5	5	5	80	160	ns
	10	10	10	50	120	
High-to-Low, t_{THL}	5	5	5	20	60	
	10	10	10	16	50	
Input Capacitance, C_I CD4009A	–	–	–	15	–	pF
CD4010A	–	–	–	5	–	

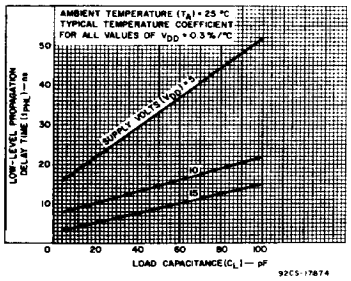


Fig. 13 — Typical high-to-low level propagation delay time vs. C_L (driving TTL, DTL).

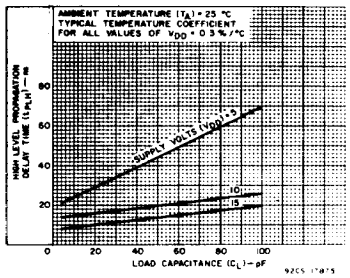


Fig. 14 — Typical low-to-high level propagation delay time vs. C_L (driving TTL, DTL)

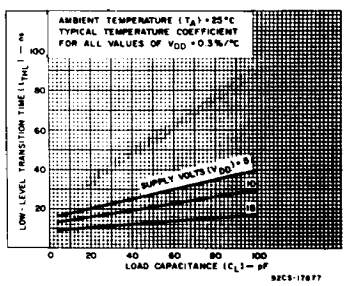


Fig. 15 — Typical high-to-low level transition time vs. C_L.

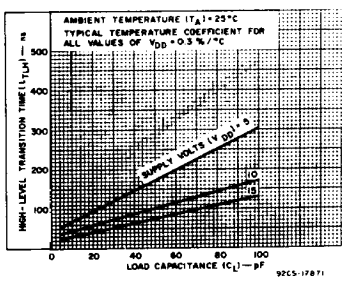


Fig. 16 — Typical low-to-high level transition time vs. C_L.

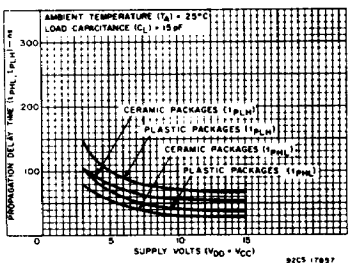


Fig. 17 — Maximum propagation delay time vs. V_{DD} – CD4009A.

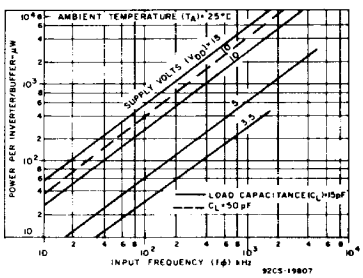


Fig. 18 — Typical dissipation characteristics.