

## DESCRIPTION

The 78P2351R is Teridian's second generation Line Interface Unit (LIU) for 155 Mbit/s electrical SDH interfaces (STM1e). The device is a single chip solution that includes an integrated Clock & Data Recovery in both the transmit and receive paths for easy, cost efficient NRZ to CMI conversion.

The device interfaces to 75Ω coaxial cable through wideband transformers and can handle over 12.7dB of cable loss. By eliminating the needs for synchronous clocks, the small 78P2351R (7x7mm MLF package) is ideal for new STM1e (ES1) Small Form-factor Pluggable (SFP) transceiver modules.

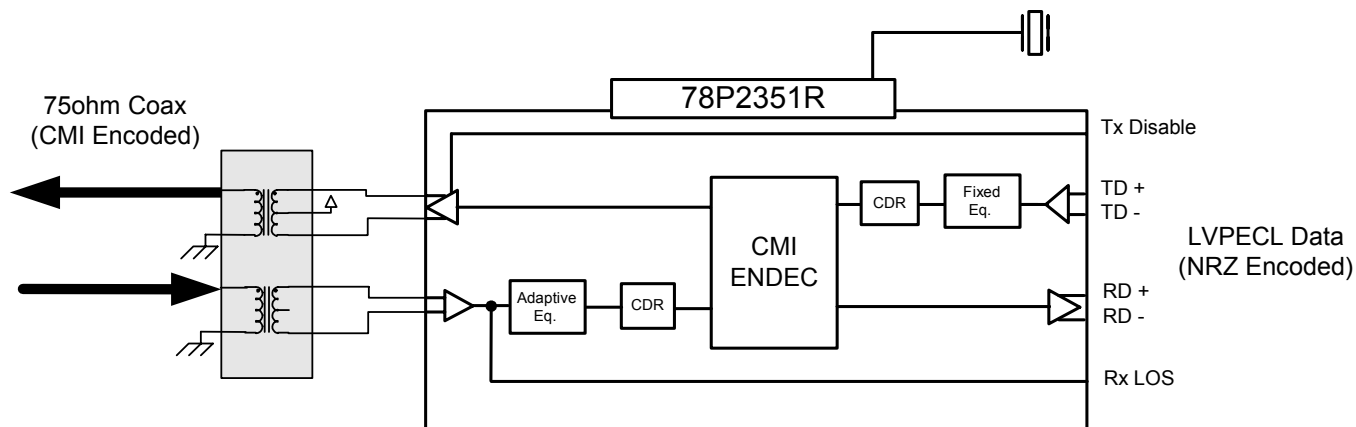
## APPLICATIONS

- STM1e SFP modules
- SDH/ATM Line Cards
- Add Drop Multiplexers (ADMs)
- PDH/SDH Test Equipment
- Digital Microwave Radios
- Multi-Service Switches

## FEATURES

- ITU-T G.703 compliant, adjustable cable driver for 155.52 Mbps CMI-coded coax transmission
- Integrated adaptive CMI equalizer and CDR in receive path handles over 12.7dB of cable loss
- LVPECL-compatible system interface with integrated CDR in transmit path for flexible NRZ to CMI conversion
- Configurable via HW control pins or 4-wire serial port interface
- Compliant with ANSI T1.105.03-1994; ITU-T G.813, G.825, G.958; and Telcordia GR-253-CORE for jitter performance
- Receive Loss of Signal (Rx LOS) detection
- Receive Monitor Mode handles up to 20dB of flat loss (at max 6dB cable loss)
- Optional fixed backplane equalizer compensates for up to 1.5m of trace
- Operates from a single 3.3V supply
- Available in a small 7x7mm 56-pin QFN package
- Industrial Temperature: -40°C to +85°C

## BLOCK DIAGRAM



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## FUNCTIONAL DESCRIPTION

The 78P2351R contains all the necessary transmit and receive circuitry for connection between 155.52Mbit/s NRZ data sources (STS-3/STM-1) and CMI encoded electrical interfaces (ES1/STM-1e). The 78P2351R system interface mimics a 3.3V optical transceiver module and only requires a reference clock and wideband transformer to complete the electrical interface. The chip can be controlled via control pins or serial port register settings.

In hardware mode (pin control) the SPSL pin must be low. Additionally, the following unused pins must be set accordingly:

- SDO pin must be tied low
- SDI pin must be tied low
- SEN pin must be tied high

In software mode (SPSL pin high), control pins set register defaults upon power-up or reset. The 78P2351R can then be configured via the 4-wire serial control interface. See Pin Descriptions section for more information.

## REFERENCE CLOCK

The 78P2351R requires a reference clock supplied to the CKREFP/N pins. For reference frequencies of 19.44MHz or 77.76MHz, the device accepts a single ended CMOS level input at CKREFP (with CKREFN pin tied to ground). For reference frequency of 155.52MHz, the device accepts a differential LVPECL clock input at CKREFP/N. The frequency of this reference input is selected by either the CKSL control pin or register bit as follows:

| CKSL pin | CKSL[1:0] bits | Reference Frequency |
|----------|----------------|---------------------|
| Low      | 0 0            | 19.44MHz            |
| Float    | 1 0            | 77.76MHz            |
| High     | 1 1            | 155.52MHz           |

## RECEIVER OPERATION

The receiver accepts an ITU-T G.703 compliant CMI encoded signal at 155.52Mbit/s from the RXP/N inputs. When properly terminated and transformer-coupled to the line, the receiver can handle over 12.7dB of cable loss. The receiver's jitter tolerance exceeds all relevant standards even with 12.7dB worth of cable attenuation and inter-symbol interference (ISI). See Receiver Jitter Tolerance section for more info.

The recovered CMI signal first enters an AGC and an adaptive equalizer designed to overcome inter-symbol interference caused by long cable lengths. The variable gain differential amplifier automatically controls the gain to maintain a constant voltage level output regardless of the input voltage level.

The outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a Delay Locked Loop (DLL), which utilizes a line-rate reference frequency derived from the clock applied to the CKREFP/N pins. After the clock and data have been recovered, the data is decoded to binary by the CMI decoder. The SODP/N pins output the recovered NRZ data at LVPECL levels.

### Receiver Monitor Mode

The SCK\_MON pin or MON register bit puts the receiver in monitor mode and adds approximately 20dB of **flat gain** to the receive signal before equalization. Rx Monitor Mode can handle 20dB of flat loss typical of monitoring points with up to 6dB (typical 225ft) of cable loss. Note that Loss of Signal detection is disabled during Rx Monitor Mode.

### Receive Loss of Signal Detect

The 78P2351R includes a Loss of Signal (LOS) detector. When the peak value of the received signal is less than approximately 19dB below nominal for approximately 110 UI, Receive Loss of Signal is asserted. The Rx LOS signal is cleared when the received signal is greater than approximately 18dB below nominal for 110 UI.

During Rx LOS conditions, the receive clock will remain on the last phase tap of the Rx DLL outputting a stable clock while the receive data outputs are squelched and held at logic '0'.

**Note:** Rx Loss of Signal detection is disabled during Local Loopback and Receive Monitor Modes.

## TRANSMITTER OPERATION

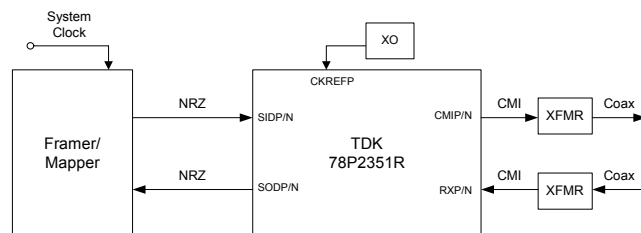
The transmitter section generates an adjustable ITU-T G.703 compliant analog signal for transmission through a wideband transformer onto 75Ω coaxial cable. Differential NRZ data is input to the 78P2351R on the SIDP/N pins at LVPECL levels and passed to a low jitter clock and data recovery circuit. An optional clock decoupling FIFO is provided to decouple the on chip and off chip clocks. The NRZ data is encoded using CMI line coding to ensure an adequate number of transitions.

Each of the transmit timing modes can be configured in HW mode or SW mode as shown in the table below.

| Tx Mode                    | HW Control | SW Control |
|----------------------------|------------|------------|
|                            | CKMODE     | SMOD[1:0]  |
| Reserved                   | Low        | 0 0        |
| Synchronous (FIFO enabled) | Floating   | 1 0        |
| Plesiochronous             | High       | 0 1        |
| Loop-timing                | n/a        | 1 1        |

### Plesiochronous Mode

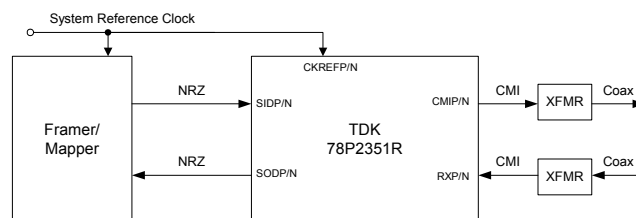
Plesiochronous mode represents a common condition where a synchronous reference clock is not available. In this mode, the 78P2351R will recover the transmit clock from the plesiochronous data and bypass the internal FIFO and re-timing block. This mode is commonly used for mezzanine cards, modules, and any application where the reference clock can't always be synchronous to the transmit source clock/data



**Figure 1: Plesiochronous Mode**

### Synchronous Mode

When the NRZ transmit data is source synchronous with the reference clock applied at CKREFP/N as shown in Figure 2, the 78P2351R can be optionally used in synchronous mode or re-timing mode. In this mode, the 78P2351R will recover the clock from the NRZ data input and re-time the data in an integrated +/- 4-bit FIFO.



**Figure 2: Synchronous**

Since the reference clock and transmit clock/data go through different delay paths, it is inevitable that the phase relationship between the two clocks can vary in a bounded manner due to the fact that the absolute delays in the two paths can vary over time. The transmit FIFO allows long-term clock phase drift between the Tx clock and system reference clock, not exceeding +/- 25.6ns, to be handled without transmit error. If the clock wander exceeds the specified limits, the FIFO will over or under flow, and the FERR register signal will be asserted. This signal can be used to trigger an interrupt. This interrupt event is automatically cleared when a FIFO Reset (FRST) pulse is applied, and the FIFO is re-centered.

### Notes:

- 1) External remote loopbacks (i.e. loopback within framer) are not possible in synchronous operation (FIFO enabled) unless the data is re-justified to be synchronous to the system reference clock or the 78P2351R is configured for loop-timing operation.
- 2) During IC power-up or transmit power-up, the clocks going to the FIFO may not be stable and cause the FIFO to overflow or underflow. As such, the FIFO should be manually reset using FRST anytime the transmitter is powered-up.

### Clock Synthesizer

The transmit clock synthesizer is a low-jitter PLL that generates a 311.04 MHz clock for the CMI encoder. A synthesized 155.52 MHz reference clock is also used in both the receive and transmit sides for clock and data recovery.

### Pulse Amplitude Adjustment

Contact TDK applications for information on user programmable registers with up to 200mV of programmable transmit gain.

### Transmit Backplane Equalizer

An optional fixed LVPECL equalizer is integrated in the transmit path for architectures that use LIUs on active interface cards. The fixed equalizer can compensate for up to 1.5m of trace and can be enabled by the TXOUT1 pin or TXEQ bit as follows:

| TXOUT1 pin | TXEQ bit | Tx Equalizer |
|------------|----------|--------------|
| Low        | 1        | Enabled      |
| Float      | 0        | Disabled     |

### POWER-DOWN FUNCTION

Power-down control is provided to allow the 78P2351R to be shut off. Transmit and receive power-down can be set independently through SW control. Global power-down is achieved by powering down both the transmitter and receiver.

**Note:** the 4-wire serial port interface and configuration registers are not affected by power-down.

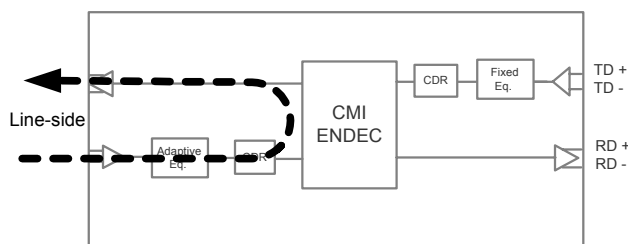
The transmitter can also be powered down using the TXPD control pin. The CMI outputs are tri-stated during transmit power-down for redundancy applications. The TXPD pin is active in both hardware and software modes.

### LOOPBACK MODES

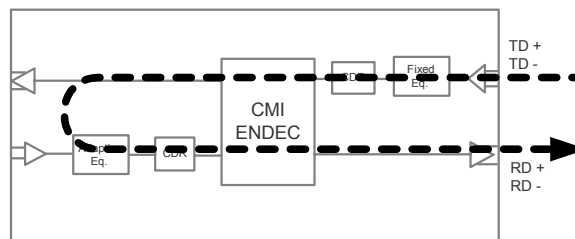
In SW mode, LLBK and RLBK bits in the Signal Control register are provided to activate the local and remote analog loopback modes respectively.

In HW mode, the LPBK pin can be used to activate local and remote analog loopback paths as shown in the table below.

| LPBK pin | Loopback Mode   |
|----------|---|
| Low      | Normal operation  |
| Float    | <u>Remote (analog) Loopback:</u><br>Recovered receive clock and data looped back directly to the transmit driver. The CMI decoder and most of transmit path is bypassed (including the redundant Tx monitor output) |
| High     | <u>Local (analog) Loopback:</u><br>Transmit clock and data looped back to receiver at the analog media interface.   |

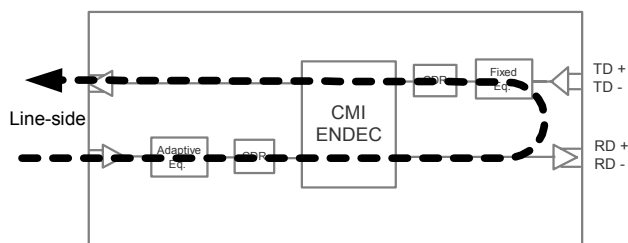


**Figure 3: Remote (analog) Loopback**



**Figure 4: Local (analog) Loopback**

In SW mode only, a Full Remote (digital) Loopback bit FLBK is also available in the Advanced Tx Control register. This loopback exercises the entire Rx and Tx paths of the 78P2351 including the Tx clock recovery unit. As such, the user must enable either Plesiochronous or Loop-timing transmit modes to utilize the Full Remote (digital) Loopback.



**Figure 5: Remote (Digital) Loopback**

## INTERNAL POWER-ON RESET

Power-On Reset (POR) function is provided on chip. Roughly 50  $\mu$ s after Vcc reaches 2.4V at power up, a reset pulse is internally generated. This resets all registers to their default values as well as all state machines within the transceiver to known initial values. The reset signal is also brought out to the PORB pin. The PORB pin is a special function analog pin that allows for the following:

- Override the internal POR signal by driving in an external active low reset signal;
- Use the internally generated POR signal to trigger other resets;
- Add external capacitor to slow down the release of power-on reset (approximately 8 $\mu$ s per nF added).

**NOTE:** Do not pull-up the PORB pin to Vcc or drive this pin high during power-up. This will prevent the internal reset generator from resetting the entire chip and may result in errors.

## SERIAL CONTROL INTERFACE

The serial port controlled register allows a generic controller to interface with the 78P2351R. It is used for mode settings, diagnostics and test, retrieval of status and performance information, and for on-chip fuse trimming during production test. The SPSL pin must be high in order to use the serial port.

The serial interface consists of 4 pins:

- Serial Port Enable (SEN),
- Serial Clock (SCK\_MON),
- Serial Data In (SDI),
- Serial Data Out (SDO).

The SEN pin initiates the read and write operations. It can also be used to select a particular device allowing SCK\_MON, SDI and SDO to be bussed together.

SCK\_MON is the clock input that times the data on SDI and SDO. Data on SDI is latched in on the rising-edge of SCK\_MON, and data on SDO is clocked out using the falling edge of SCK\_MON.

SDI is used to insert mode, address, and register data into the chip. Address and Data information are input least significant bit (LSB) first. The mode and address bit assignment and register table are shown in the following section.

SDO is a tristate capable output. It is used to output register data during a read operation. SDO output is normally high impedance, and is enabled only during the duration when register data is being clocked out. Read data is clocked out least significant bit (LSB) first.

If SDI coming out of the micro-controller chip is also tristate capable, SDI and SDO can be connected together to simplify connections.

The maximum clock frequency for register access is 20MHz.

## REGISTER DESCRIPTION

### REGISTER ADDRESSING

| Address Bits | Bit 7        | Bit 6 | Bit 5 | Bit 4 | Bit 3       | Bit 2 | Bit 1 | Bit 0          |
|--------------|--------------|-------|-------|-------|-------------|-------|-------|----------------|
|              | Port Address |       |       |       | Sub-Address |       |       | Read/<br>Write |
| Assignment   | PA[3]        | PA[2] | PA[1] | PA[0] | SA[2]       | SA[1] | SA[0] | R/W*           |

### REGISTER TABLE

#### a) PA[3:0] = 0 : Global Registers

| Sub Addr | Reg. Name   | Description    | Bit 7     | Bit 6     | Bit 5     | Bit 4          | Bit 3          | Bit 2     | Bit 1     | Bit 0       |
|----------|-------------|----------------|-----------|-----------|-----------|----------------|----------------|-----------|-----------|-------------|
| 0        | MSCR (R/W)  | Master Control | --<br><0> | --<br><0> | --<br><0> | CKSL[1]<br><X> | CKSL[0]<br><X> | --<br><X> | --<br><X> | SRST<br><0> |
| 1        | --<br>(R/W) | Reserved       | --<br><0> | --<br><0> | --<br><1> | --<br><0>      | --<br><0>      | --<br><0> | --<br><1> | --<br><1>   |
| 2        | --<br>(R/W) | Reserved       | --<br><X> | --<br><X> | --<br><X> | --<br><X>      | --<br><X>      | --<br><X> | --<br><X> | --<br><0>   |

#### b) PA[3:0] = 1 : Port-Specific Registers

| Sub Addr | Reg. Name   | Description           | Bit 7          | Bit 6          | Bit 5        | Bit 4          | Bit 3          | Bit 2         | Bit 1         | Bit 0       |
|----------|-------------|-----------------------|----------------|----------------|--------------|----------------|----------------|---------------|---------------|-------------|
| 0        | MDCR (R/W)  | Mode Control          | PDTX<br><0>    | PDRX<br><0>    | --<br><0>    | SMOD[1]<br><X> | SMOD[0]<br><X> | MON<br><0>    | --<br><0>     | --<br><1>   |
| 1        | SGCR (R/W)  | Signal Control        | TCMIINV<br><0> | RCMIINV<br><0> | LOSOR<br><0> | RLBK<br><0>    | LLBK<br><0>    | --<br><0>     | --<br><0>     | FRST<br><0> |
| 2        | ACR1 (R/W)  | Advanced Tx Control 1 | --<br><0>      | --<br><0>      | --<br><0>    | --<br><0>      | --<br><0>      | --<br><0>     | TPK<br><0>    | TXEQ<br><0> |
| 3        | ACR0 (R/W)  | Advanced Tx Control 0 | --<br><1>      | --<br><0>      | --<br><1>    | --<br><0>      | --<br><1>      | BST[1]<br><0> | BST[0]<br><0> | FLBK<br><0> |
| 4        | --<br>(R/W) | Reserved              | --<br><1>      | --<br><X>      | --<br><X>    | --<br><0>      | --<br><0>      | --<br><0>     | --<br><0>     | --<br><0>   |
| 5        | STAT (R/C)  | Status Monitor        | --<br><X>      | --<br><X>      | --<br><X>    | RXLOS<br><X>   | --<br><X>      | --<br><X>     | TXLOS<br><X>  | FERR<br><X> |
| 6-7      | --          | Reserved              | --             | --             | --           | --             | --             | --            | --            | --          |



**REGISTER DESCRIPTION** (continued)

**LEGEND**

| TYPE | DESCRIPTION    | TYPE | DESCRIPTION   |
|------|----------------|------|---------------|
| R/O  | Read only      | R/W  | Read or Write |
| R/C  | Read and Clear |      |               |

**GLOBAL REGISTERS**
**ADDRESS 0-0: MASTER CONTROL REGISTER**

| BIT | NAME          | TYPE | DFLT VALUE | DESCRIPTION   |
|-----|---------------|------|------------|---|
| 7:5 | --            | R/W  | 0X0        | Reserved.   |
| 4:3 | CKSL<br>[1:0] | R/W  | X          | <b>Reference Clock Frequency Select:</b><br>Selects the reference clock frequency input at CKREFP/N pins.<br>11: 155.52 MHz (differential LVPECL input)<br>10: 77.76 MHz (single-ended CMOS input) – <i>Tie CKREFN to ground.</i><br>00: 19.44 MHz (single-ended CMOS input) – <i>Tie CKREFN to ground.</i><br><b>Note:</b> Default values depend on the CKSL pin setting upon reset or power up. |
| 2:1 | --            | R/W  | X0         | Reserved.   |
| 0   | SRST          | R/W  | 0          | <b>Register Soft-Reset:</b><br>When this bit is set, all registers are reset to their default values. This register bit is self-clearing.   |

**ADDRESS 0-1: RESERVED**

| BIT | NAME | TYPE | DFLT VALUE | DESCRIPTION |
|-----|------|------|------------|-------------|
| 7:0 | --   | R/W  | 00100X11   | Reserved.   |

**ADDRESS 0-2: RESERVED**

| BIT | NAME | TYPE | DFLT VALUE | DESCRIPTION |
|-----|------|------|------------|-------------|
| 7:0 | --   | R/W  | XXXXXXXX0  | Reserved.   |

**REGISTER DESCRIPTION** (continued)

**PORT-SPECIFIC REGISTERS**

For PA[3:0] = 1 only. Accessing a register with port address greater than 1 constitutes an invalid command, and the read/write operation will be ignored.

**ADDRESS 1-0: MODE CONTROL REGISTER**

| BIT | NAME    | TYPE | DFLT VALUE | DESCRIPTION   |
|-----|---------|------|------------|---|
| 7   | PDTX    | R/W  | 0          | <b>Transmitter Power-Down:</b><br>0 : Normal Operation<br>1 : Power-Down. CMI Transmit output is tri-stated.  |
| 6   | PDRX    | R/W  | 0          | <b>Receiver Power-Down:</b><br>0 : Normal Operation<br>1 : Power-Down   |
| 5   | --      | R/W  | 0          | Reserved.   |
| 4   | SMOD[1] | R/W  | X          | <b>Serial Mode Interface Selection:</b><br><u>SMOD[1] SMOD[0]</u><br>0      0      Reserved<br>1      0 <u>Synchronous data</u> is passed through the CDR and then through the FIFO.<br>0      1 <u>Plesiochronous data</u> is passed through the CDR to recover a clock, but the FIFO is bypassed because the data is not synchronous with the reference clock.<br>1      1 <u>Loop Timing Mode Enable</u> : The recovered receive clock is used as the reference for the transmit DLL and FIFO.<br><b>Note:</b> Default values depend on the CKMODE pin setting upon reset or power up. |
| 3   | SMOD[0] | R/W  | X          |   |
| 2   | MON     | R/W  | 0          | <b>Receive Monitor Mode Enable:</b><br>0: Normal Operation<br>1: Adds 20dB of flat gain to the receive signal before equalization.  |
| 1:0 | --      | R/W  | 01         | Reserved.   |

**REGISTER DESCRIPTION** (continued)

**ADDRESS 1-1: SIGNAL CONTROL REGISTER**

| BIT  | NAME    | TYPE   | DFLT VALUE | DESCRIPTION  |      |      |  |   |   |                  |   |   |  |   |   |  |
|------|---------|--|------------|--|------|------|--|---|---|------------------|---|---|--|---|---|--|
| 7    | TCMIINV | R/W  | 0          | <b>Transmit CMI Inversion:</b><br>This bit will flip the polarity of the transmit CMI data outputs at CMIP/N. For debug use only.<br>0: Normal<br>1: Invert  |      |      |  |   |   |                  |   |   |  |   |   |  |
| 6    | RCMIINV | R/W  | 0          | <b>Receive CMI Inversion:</b><br>This bit will flip the polarity of the receive CMI data inputs at RXP/N. For debug use only.<br>0: Normal<br>1: Invert  |      |      |  |   |   |                  |   |   |  |   |   |  |
| 5    | LOSOR   | R/W  | 0          | <b>Receive Loss of Signal Override/Disable:</b><br>When set, the LOS signal will always remain low.<br>0: Normal<br>1: Forces LOS output to be low and resets counter  |      |      |  |   |   |                  |   |   |  |   |   |  |
| 4    | RLBK    | R/W  | 0          | <b>Analog Loopback Selection:</b><br><table><thead><tr><th>RLBK</th><th>LLBK</th><th></th></tr></thead><tbody><tr><td>0</td><td>0</td><td>Normal operation</td></tr><tr><td>1</td><td>0</td><td><u>Remote Loopback Enable</u>: Recovered receive data is looped back to the transmit driver for retransmission.</td></tr><tr><td>0</td><td>1</td><td><u>Local Loopback Enable</u>: The transmit data is looped back and used as the input to the receiver.</td></tr></tbody></table> | RLBK | LLBK |  | 0 | 0 | Normal operation | 1 | 0 | <u>Remote Loopback Enable</u> : Recovered receive data is looped back to the transmit driver for retransmission. | 0 | 1 | <u>Local Loopback Enable</u> : The transmit data is looped back and used as the input to the receiver. |
| RLBK | LLBK    |  |            |  |      |      |  |   |   |                  |   |   |  |   |   |  |
| 0    | 0       | Normal operation   |            |  |      |      |  |   |   |                  |   |   |  |   |   |  |
| 1    | 0       | <u>Remote Loopback Enable</u> : Recovered receive data is looped back to the transmit driver for retransmission. |            |  |      |      |  |   |   |                  |   |   |  |   |   |  |
| 0    | 1       | <u>Local Loopback Enable</u> : The transmit data is looped back and used as the input to the receiver.           |            |  |      |      |  |   |   |                  |   |   |  |   |   |  |
| 3    | LLBK    | R/W  | 0          |  |      |      |  |   |   |                  |   |   |  |   |   |  |
| 2:1  | --      | R/W  | 00         | Reserved.  |      |      |  |   |   |                  |   |   |  |   |   |  |
| 0    | FRST    | R/W  | 0          | <b>FIFO Reset:</b><br>0: Normal operation<br>1: Reset FIFO pointers to default locations.<br>This reset should be initiated anytime the transmitter or IC powers up to ensure the FIFO is centered after internal VCO clocks and external transmit clocks are stable.<br><u>NOTE:</u> FIFO reset not required for Plesiochronous Mode  |      |      |  |   |   |                  |   |   |  |   |   |  |

**ADDRESS 1-2: ADVANCED TRANSMIT CONTROL REGISTER 1**

| BITS | NAME | TYPE | DFLT VALUE  | DESCRIPTION   |
|------|------|------|-------------|---|
| 7:1  | --   | R/W  | 000000<br>0 | Reserved.   |
| 0    | TXEQ | R/W  | 0           | <b>Transmit Fixed Equalizer Enable:</b><br>When enabled, compensates for between 0.75m and 1.5m of FR4 trace to the LVPECL data inputs SIDP/N<br>0: Normal Operation<br>1: Enable equalizer |

**REGISTER DESCRIPTION** (continued)

**ADDRESS 1-3: ADVANCED TRANSMIT CONTROL REGISTER 0**

| BIT | NAME     | TYPE | DFLT VALUE | DESCRIPTION   |
|-----|----------|------|------------|---|
| 7:3 | --       | R/W  | 10101      | Reserved.   |
| 2:1 | BST[1:0] | R/W  | 00         | <b>Transmit Driver Amplitude Boost:</b><br>Adds 5% or 10% of boost to the CMI output.<br>00 : Normal amplitude<br>01 : 5% boost<br>10 : Reserved<br>11 : 10% boost  |
| 0   | FLBK     | R/W  | 0          | <b>Full Remote (digital) Loopback Enable:</b><br>When enabled the recovered receive data is decoded and looped back to the transmit clock recovery unit exercising the entire receive and transmit paths.<br><b>NOTE:</b> Must be used in conjunction with Plesiochronous Mode or Loop-Timing Mode. |

**ADDRESS 1-4: RESERVED**

| BIT | NAME | TYPE | DFLT VALUE | DESCRIPTION |
|-----|------|------|------------|-------------|
| 7:0 | --   | R/W  | 1XX00000   | Reserved.   |

**ADDRESS 1-5: STATUS MONITOR REGISTER**

| BIT | NAME  | TYPE | DFLT VALUE | DESCRIPTION   |
|-----|-------|------|------------|---|
| 7:5 | --    | R/C  | XXX        | Reserved.   |
| 4   | RXLOS | R/C  | X          | <b>Receive Loss of Signal Indication:</b><br>0: Normal operation<br>1: Loss of signal condition detected at CMI inputs  |
| 3:2 | --    | R/C  | X          | Reserved.   |
| 1   | TXLOS | R/C  | X          | <b>Transmit Loss of Signal Indication:</b><br>0: Valid transmit input signal detected at SIDP/N<br>1: No valid signal detected at SIDP/N  |
| 0   | FERR  | R/C  | X          | <b>Transmit FIFO Error Indication:</b><br>This bit is set whenever the internal FERR signal is asserted, indicating that the FIFO is operating at its depth limit. It is reset to 0 when the FRST bit is asserted.<br>0: Normal operation<br>1: Transmit FIFO phase error |

**ADDRESS 1-6: TRANSMIT GAIN REGISTER**

| BIT | NAME | TYPE | DFLT<br>VALUE | DESCRIPTION   |
|-----|------|------|---------------|---|
| 7:0 | RSVD | R/O  | 0             | Reserved for pulse amplitude programmability. Contact Teridian applications support for more information. |

**ADDRESS 1-7: RESERVED**

| BIT | NAME | TYPE | DFLT<br>VALUE | DESCRIPTION        |
|-----|------|------|---------------|--------------------|
| 7:0 | RSVD | R/O  | 0             | Reserved for test. |

## PIN DESCRIPTION

### LEGEND

| TYPE | DESCRIPTION                     | TYPE | DESCRIPTION                           |
|------|---------------------------------|------|---------------------------------------|
| A    | Analog Pin                      | PO   | LVPECL-Compatible Differential Output |
| CIT  | 3-State CMOS Digital Input      | OD   | Open-drain Output                     |
| CI   | CMOS Digital Input              | PI   | LVPECL-Compatible Differential Input  |
| CID  | CMOS Digital Input w/ Pull-down | S    | Supply                                |
| CIS  | CMOS Schmitt Trigger Input      | G    | Ground                                |
| COZ  | CMOS Tristate Digital Output    |      |                                       |

### TRANSMITTER PINS

| NAME         | PIN      | TYPE | DESCRIPTION  |
|--------------|----------|------|--|
| SIDP<br>SIDN | 4<br>5   | PI   | <b>Transmit Serial Data Input:</b><br>Differential NRZ data input. See <i>Transmitter Operation</i> section for more info on different timing modes.   |
| CMIP<br>CMIN | 53<br>54 | A    | <b>Transmit Serial CMI Data Output:</b><br>A CMI encoded data signal conforming to the relevant ITU-T G.703 pulse templates when properly terminated and transformer coupled to 75ohm cable.<br><b>Notes:</b> 1) Pins are tri-stated during transmit power-down. 2) Pins are active, but undefined during reset. |

### RECEIVER PINS

| NAME         | PIN      | TYPE | DESCRIPTION   |
|--------------|----------|------|---|
| SODP<br>SODN | 13<br>14 | PO   | <b>Receive Serial NRZ Data Output:</b><br>Recovered serial data decoded into NRZ format and output at LVPECL levels.<br><b>Notes:</b> 1) Outputs are squelched during LOS and held low. 2) Pins are active, but undefined during reset. |
| RXP<br>RXN   | 50<br>51 | A    | <b>Receive Serial CMI Input:</b><br>Receive inputs that should be differentially terminated and transformer coupled to the coaxial cable.   |

### REFERENCE AND STATUS PINS

| NAME             | PIN      | TYPE      | DESCRIPTION  |
|------------------|----------|-----------|--|
| CKREFP<br>CKREFN | 45<br>44 | PI/<br>CI | <b>Reference Clock Input:</b> (Required)<br>A reference clock input used for clock/data recovery and generation. Can be a differential 155.52MHz differential LVPECL Input (Type PI) at CKREFP/N or a single-ended 19.44MHz or 77.78MHz CMOS Input (Type CI) at CKREFP (tie CKREFN to ground when unused). |
| LOS              | 33       | OD        | <b>Loss of Signal</b> (active-high):<br>Standards compatible loss of signal indicator.   |
| PORB             | 36       | A         | <b>Power-On Reset</b> (active low):<br>See Power-On Reset description on use of this pin. Do not pull-up to Vcc.   |

**PIN DESCRIPTION** (continued)

**CONTROL PINS**

| NAME   | PIN | TYPE | DESCRIPTION   |
|--------|-----|------|---|
| LPBK   | 10  | CIT  | <b>Loopback Selection:</b><br><u>Low:</u> Normal operation<br><u>Float:</u> Remote Loopback Enable: Recovered receive data and clock are looped back to the transmitter for retransmission.<br><u>High:</u> Local Loopback Enable: The transmit data is looped back and used as the input to the receiver.                      |
| CKMODE | 9   | CIT  | <b>Clock Mode Selection:</b><br><u>Low:</u> Reserved<br><u>Float:</u> Reference clock is <u>synchronous</u> to transmit data. Clock is recovered with a CDR and data is passed through a FIFO<br><u>High:</u> Reference clock is <u>plesiochronous</u> to transmit data. Clock is recovered with a CDR and the FIFO is bypassed |
| TXOUT1 | 56  | CIT  | <b>Advanced Tx Control 1:</b><br><u>Low:</u> Enables fixed LVPECL equalizer at the transmit inputs SIDP/N (for FR4 trace lengths up to 1.5m).<br><u>Float:</u> Normal operation<br><u>High:</u> Normal operation  |
| TXOUT0 | 1   | CIT  | <b>Advanced Tx Control 0:</b><br><u>Low:</u> Nominal amplitude<br><u>Float:</u> 5% amplitude boost<br><u>High:</u> 10% amplitude boost  |
| TXPD   | 8   | CID  | <b>Transmitter Power Down:</b><br>When high, powers down and tri-states the transmit driver.  |
| SPSL   | 32  | CID  | <b>Serial Port Selection:</b><br>When high, chip is software controlled through the 4-wire serial port.   |
| CKSL   | 34  | CIT  | <b>Reference Clock Frequency Selection:</b><br>Selects the reference frequency that is supplied at the CKREFP/N pins. Its level is read in at power-up or on the rising edge of a reset signal at the PORB pin.<br><u>Low:</u> 19.44MHz<br><u>Float:</u> 77.76MHz<br><u>High:</u> 155.52MHz                                     |

**PIN DESCRIPTION** (continued)

**SERIAL-PORT PINS**

| NAME    | PIN | TYPE | DESCRIPTION   |
|---------|-----|------|---|
| SEN     | 41  | CIU  | [SPSL=1] <b>Serial-Port Enable:</b><br>High during read and write operations. Low disables the serial port. While SEN is low, SDO remains in high impedance state, and SDI and SCK activities are ignored.<br>[SPSL=0] <b>Reserved. Must be tied high</b> |
| SCK_MON | 42  | CIS  | [SPSL=1] <b>Serial Clock:</b><br>Controls the timing of SDI and SDO.<br>[SPSL=0] <b>Receive Monitor Mode Enable:</b><br>When high, adds 20dB of flat gain to the incoming signal before equalization.   |
| SDI     | 40  | CI   | [SPSL=1] <b>Serial Data Input:</b><br>Inputs mode and address information. Also inputs register data during a Write operation. Both address and data are input least significant bit first.<br>[SPSL=0] <b>Reserved. Must be tied low</b>                 |
| SDO     | 39  | COZ  | [SPSL=1] <b>Serial Data Output:</b><br>Outputs register information during a Read operation. Data is output least significant bit first<br>[SPSL=0] <b>Must be tied low</b>   |

**POWER AND GROUND PINS**

It is recommended that all supply pins be connected to a single power supply plane and all ground pins be connected to a single ground plane.

| NAME | PIN                                     | TYPE | DESCRIPTION               |
|------|---|------|---------------------------|
| VCC  | 2, 6, 11, 31, 38,<br>43, 48, 52         | S    | <b>Power Supply (Vdd)</b> |
| GND  | 3, 7, 12, 30, 35,<br>37, 46, 47, 49, 55 | G    | <b>Ground</b>             |



## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation beyond these limits may permanently damage the device.

| PARAMETER                    | RATING                |
|------------------------------|-----------------------|
| Supply Voltage (Vdd)         | -0.5 to 4.0 VDC       |
| Storage Temperature          | -65 to 150 °C         |
| Junction Temperature         | -40 to 150 °C         |
| Pin Voltage (CMIP, CMIN)     | Vdd + 1.5 VDC         |
| Pin Voltage (all other pins) | -0.3 to (Vdd+0.6) VDC |
| Pin Current                  | ±100 mA               |

### RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges.

| PARAMETER                     | RATING           |
|-------------------------------|------------------|
| DC Voltage Supply (Vdd)       | 3.15 to 3.45 VDC |
| Ambient Operating Temperature | -40 to 85°C      |
| Junction Temperature          | -40 to 125°C     |

### DC CHARACTERISTICS:

| PARAMETER  | SYMBOL | CONDITIONS                       | MIN | NOM | MAX | UNIT |
|--|--------|----------------------------------|-----|-----|-----|------|
| Supply Current<br>(including transmitter current<br>through transformer) | Idd    | Max cable length                 |     | 160 | 180 | mA   |
| Receive-only Supply Current  | Iddr   | Transmitter disabled<br>(PDTX=1) |     | 92  | 106 | mA   |
| Power down Current   | Iddq   | PDTX=1, PDRX=1                   |     | 7   | 10  | mA   |

**ELECTRICAL SPECIFICATIONS** (continued)

**ANALOG PINS CHARACTERISTICS:**

The following table is provided for informative purpose only. Not tested in production.

| PARAMETER                                   | SYMBOL | CONDITIONS       | MIN | NOM | MAX | UNIT       |
|---|--------|------------------|-----|-----|-----|------------|
| RXP and RXN<br>Common-Mode Bias Voltage     | Vblin  | Ground Reference | 1.9 |     | 2.6 | V          |
| RXP and RXN Differential<br>Input Impedance | Rilin  |                  |     | 20  |     | k $\Omega$ |
| Analog Input/Output<br>Capacitance          | Cin    |                  |     | 8   |     | pF         |
| PORB Input Impedance                        | --     |                  |     | 5   |     | k $\Omega$ |

**DIGITAL I/O CHARACTERISTICS:**

Pins of type CI, CID:

| PARAMETER            | SYMBOL   | CONDITIONS    | MIN | NOM | MAX | UNIT       |
|----------------------|----------|---------------|-----|-----|-----|------------|
| Input Voltage Low    | Vil      |               |     |     | 0.8 | V          |
| Input Voltage High   | Vih      |               | 2.0 |     |     | V          |
| Input Current        | Iil, Iih |               | -1  | 0   | 1   | $\mu$ A    |
| Pull-down Resistance | Rpd      | Type CID only | 40  | 58  | 120 | k $\Omega$ |
| Input Capacitance    | Cin      |               |     | 8   |     | pF         |

Pins of type CIT:

| PARAMETER  | SYMBOL | CONDITIONS | MIN     | NOM | MAX | UNIT       |
|--|--------|------------|---------|-----|-----|------------|
| Input Voltage Low                                      | Vtil   |            |         |     | 0.4 | V          |
| Input Voltage High                                     | Vtth   |            | Vcc-0.6 |     |     | V          |
| Minimum impedance to be<br>considered as "float" state | Rtiz   |            | 30      |     |     | k $\Omega$ |

Pins of type CIS:

| PARAMETER             | SYMBOL   | CONDITIONS | MIN | NOM | MAX | UNIT    |
|-----------------------|----------|------------|-----|-----|-----|---------|
| Low-to-High Threshold | Vt+      |            | 1.3 |     | 1.7 | V       |
| High-to-Low Threshold | Vt-      |            | 0.8 |     | 1.2 | V       |
| Input Current         | Iil, Iih |            | -1  |     | 1   | $\mu$ A |
| Input Capacitance     | Cin      |            |     | 8   |     | pF      |

Pins of type COZ:

| PARAMETER                           | SYMBOL | CONDITIONS        | MIN | NOM | MAX | UNIT     |
|-------------------------------------|--------|-------------------|-----|-----|-----|----------|
| Output Voltage Low                  | Vol    | Iol = 8mA         |     |     | 0.4 | V        |
| Output Voltage High                 | Voh    | Ioh = -8mA        | 2.4 |     |     | V        |
| Output Transition Time              | Tt     | CL = 20pF, 10-90% |     |     | 2   | ns       |
| Effective Source Impedance          | Rscr   |                   |     | 30  |     | $\Omega$ |
| Tri-state Output Leakage<br>Current | Iz     |                   | -1  |     | 1   | $\mu$ A  |

**ELECTRICAL SPECIFICATIONS** (continued)

**DIGITAL I/O CHARACTERISTICS:** (continued)

Pins of type PO:

| PARAMETER                  | SYMBOL           | CONDITIONS                 | MIN   | NOM  | MAX  | UNIT |
|----------------------------|------------------|----------------------------|-------|------|------|------|
| Signal Swing               | V <sub>pk</sub>  |                            | 0.5   | 0.8  | 1.1  | V    |
| Common Mode Level          | V <sub>cm</sub>  | V <sub>dd</sub> referenced | -1.55 | -1.2 | -1.1 | V    |
| Effective Source Impedance | R <sub>eff</sub> |                            |       | 20   |      | Ω    |
| Rise Time                  | T <sub>r</sub>   | 10-90%                     |       | 0.8  | 1.2  | ns   |
| Fall Time                  | T <sub>f</sub>   | 10-90%                     |       | 0.8  | 1.2  | ns   |

Pins of type PI:

| PARAMETER         | SYMBOL            | CONDITIONS                 | MIN  | NOM  | MAX  | UNIT |
|-------------------|-------------------|----------------------------|------|------|------|------|
| Signal Swing      | V <sub>pk</sub> i |                            | 0.3  |      |      | V    |
| Common Mode Level | V <sub>cm</sub>   | V <sub>dd</sub> referenced | -1.6 | -1.2 | -0.8 | V    |

Pins of type OD

| PARAMETER                 | SYMBOL          | CONDITIONS            | MIN | NOM | MAX | UNIT |
|---------------------------|-----------------|-----------------------|-----|-----|-----|------|
| Output Voltage Low        | V <sub>ol</sub> | I <sub>ol</sub> = 8mA |     |     | 0.4 | V    |
| Pull-down Leakage Current | I <sub>pd</sub> | Logic high output     |     |     | 1   | nA   |
| Pull-up Resistor          | R <sub>pu</sub> |                       | 4.7 |     | 10  | kΩ   |

**REFERENCE CLOCK CHARACTERISTICS:**

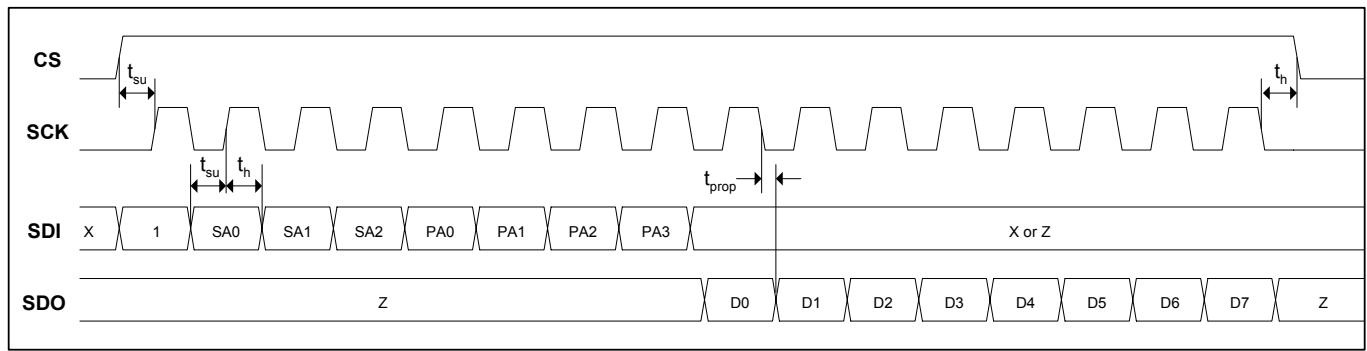
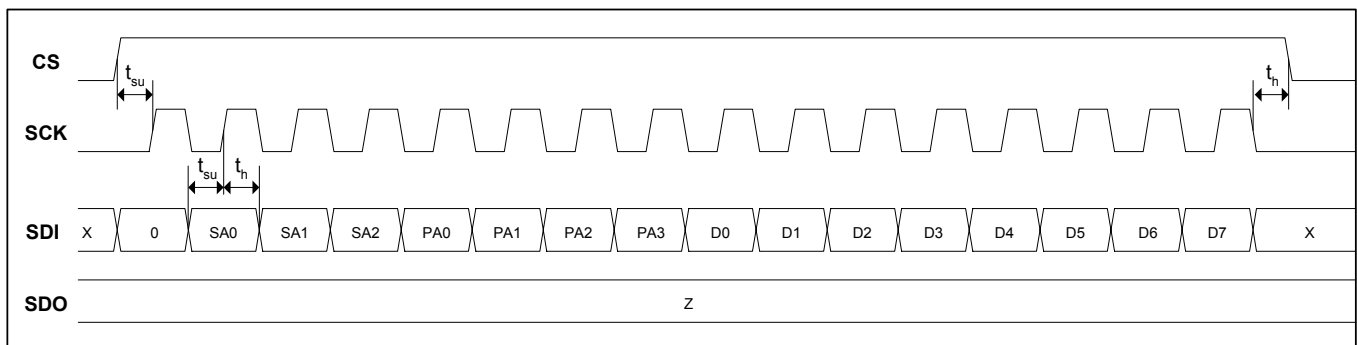
| PARAMETER                 | SYMBOL | CONDITIONS                                       | MIN | NOM | MAX | UNIT |
|---------------------------|--------|--|-----|-----|-----|------|
| CKREF Duty Cycle          | --     |  | 40  |     | 60  | %    |
| CKREF Frequency Stability | --     | Synchronous mode                                 | -20 |     | +20 | ppm  |
|                           |        | Plesiochronous or Loop-timing mode. (see Note 1) | -75 |     | +75 |      |

Note 1: In Plesiochronous mode, the transmit data source (i.e. framer) must still be of +/-20ppm quality in order to meet SONET/SDH bit rate requirements.

**ELECTRICAL SPECIFICATIONS** (continued)

**SERIAL-PORT TIMING CHARACTERISTICS:**

| PARAMETER                    | SYMBOL     | CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------|------------|-----|-----|-----|------|
| SDI to SCK setup time        | $t_{su}$   |            | 4   |     |     | ns   |
| SDI to SCK hold time         | $t_h$      |            | 4   |     |     | ns   |
| SCK to SDO propagation delay | $t_{prop}$ |            |     |     | 10  | ns   |
| SCK Frequency                | SCK        |            |     |     | 20  | MHz  |


**Figure 6: Read Operation**

**Figure 7: Write Operation**

## ELECTRICAL SPECIFICATIONS (continued)

### TRANSMITTER SPECIFICATIONS FOR CMI INTERFACE

Bit Rate: 155.52Mbps/s  $\pm$  20ppm

Code: Coded Mark Inversion (CMI)

Relevant Specification: ITU-T G.703, Telcordia GR-253, ANSI T1.102

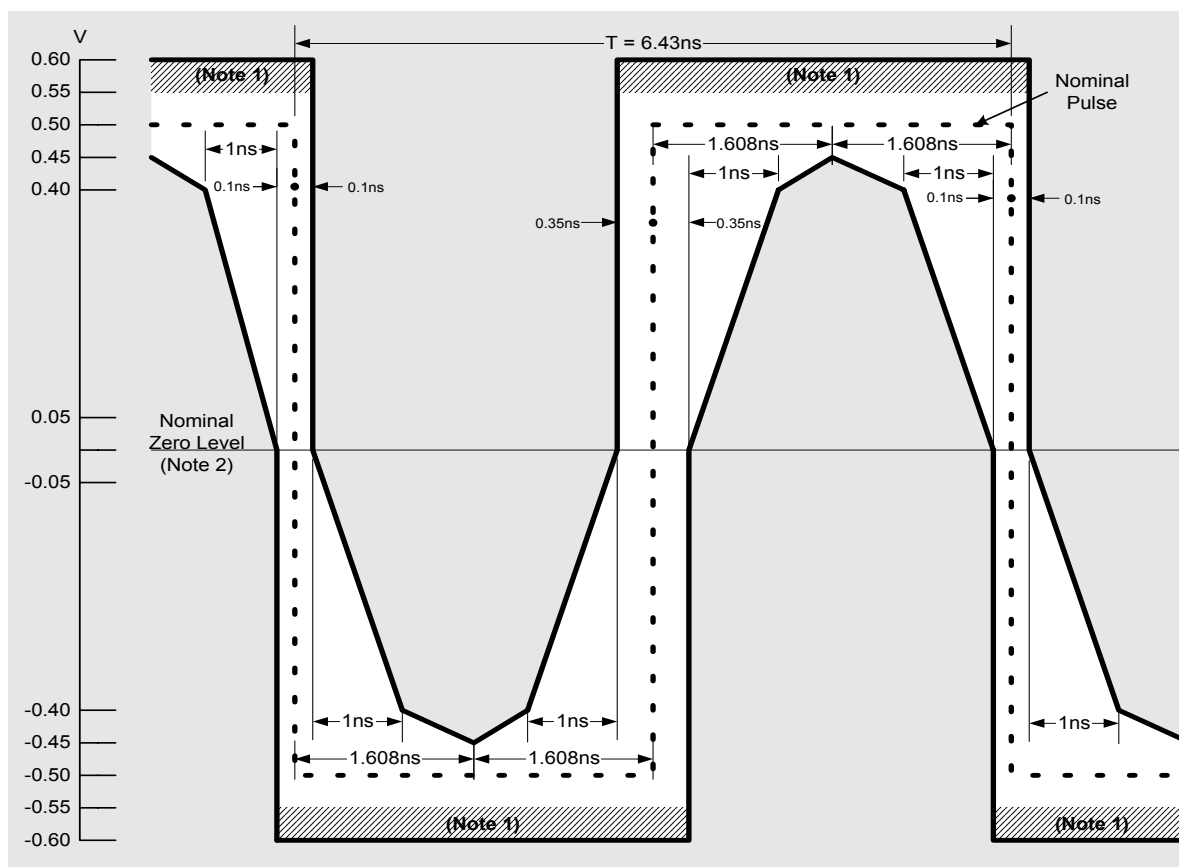
With the coaxial output port driving a 75 $\Omega$  load, the output pulses conform to the templates in Figures 8 and 9. These specifications are tested during production test. Consult application note for reference schematic, layout guidelines, and recommended transformers.

| PARAMETER   | CONDITION                                   | MIN   | NOM  | MAX  | UNIT |
|---|---|-------|------|------|------|
| Peak-to-peak Output Voltage<br>(Fuse-trimmed to nominal target at final test) | Template, steady state                      | 0.9   | 1.04 | 1.1  | V    |
| Rise/ Fall Time   | 10-90%                                      |       |      | 2    | ns   |
| Transition Timing Tolerance   | Negative Transitions                        | -0.1  |      | 0.1  | ns   |
|   | Positive Transitions at Interval Boundaries | -0.5  |      | 0.5  |      |
|   | Positive Transitions at mid-interval        | -0.35 |      | 0.35 |      |

The following specifications are not tested during production test. They are included for information only.

Note that the return loss depends on the board layout and the particular transformer used.

| PARAMETER        | CONDITION            | MIN | NOM    | MAX | UNIT             |
|------------------|----------------------|-----|--------|-----|------------------|
| Output Impedance | Driver is open drain |     | 1<br>8 |     | M $\Omega$<br>pF |
| Return Loss      | 7MHz to 240MHz       | 15  |        |     | dB               |

**ELECTRICAL SPECIFICATIONS** (continued)


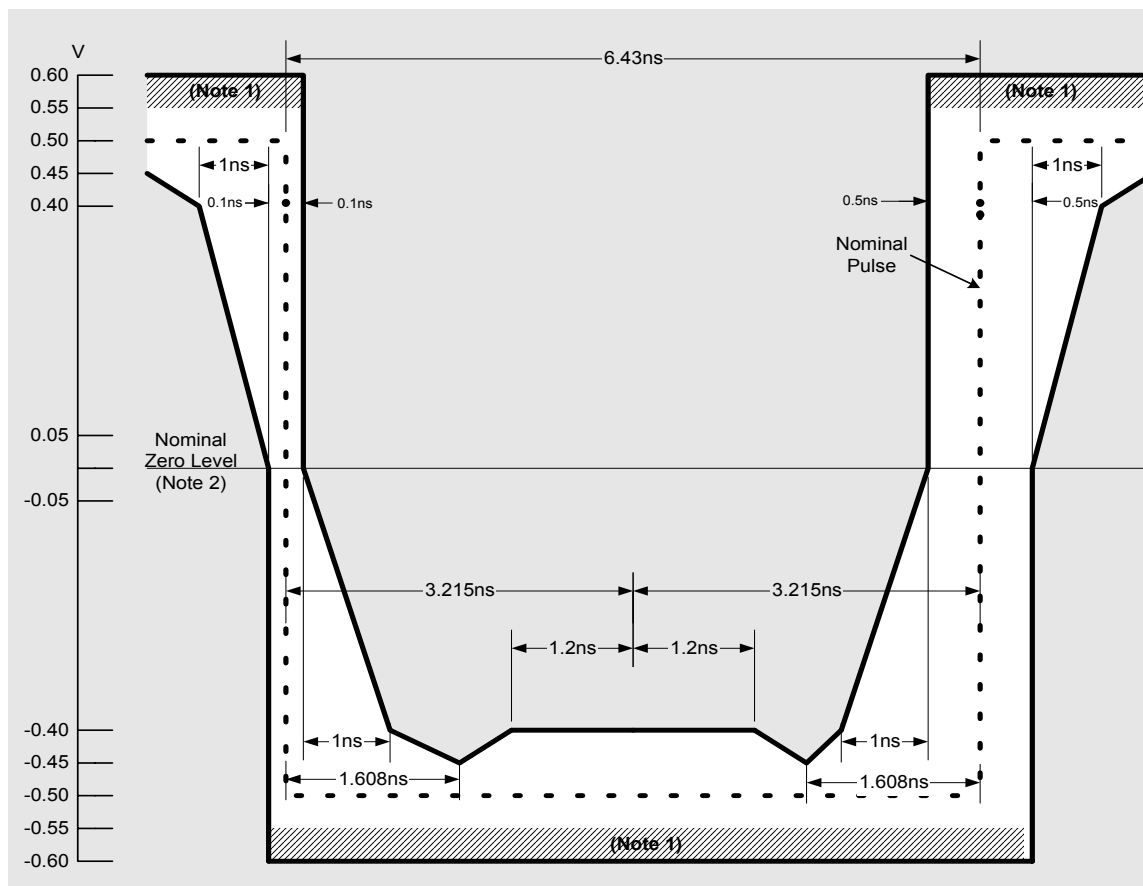
Note 1 – The maximum “steady state” amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the shaded area bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V.

Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01  $\mu$ F, to the input of the oscilloscope used for measurements. The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed  $\pm 0.05$ V. This may be checked by removing the input signal again and verifying that the trace lies with  $\pm 0.05$ V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident. The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal. When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between  $-0.4$ V and  $0.4$ V, and should not exceed 2ns.

**Figure 8 – Mask of a Pulse corresponding to a binary Zero.**

**ELECTRICAL SPECIFICATIONS** (continued)


Note 1 – The maximum “steady state” amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the shaded area bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V.

Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01  $\mu$ F, to the input of the oscilloscope used for measurements. The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed  $\pm 0.05$ V. This may be checked by removing the input signal again and verifying that the trace lies with  $\pm 0.05$ V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident. The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal. When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between  $-0.4$ V and  $0.4$ V, and should not exceed 2ns.

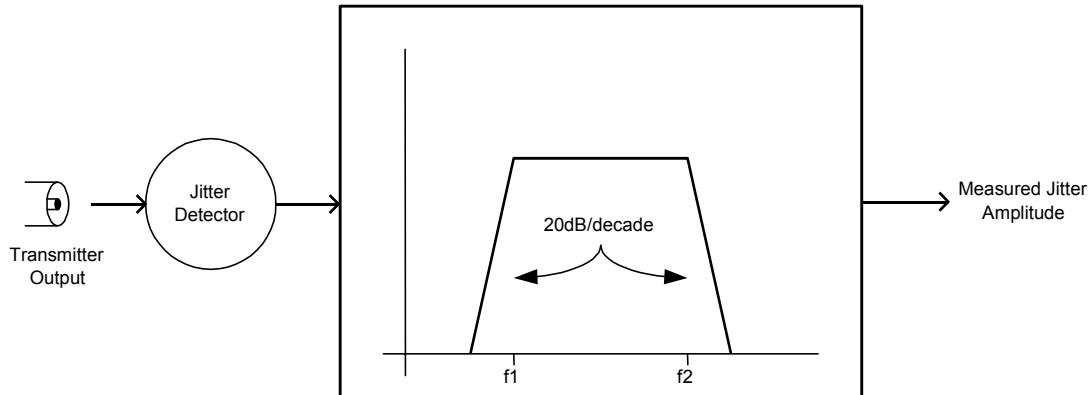
Note 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are  $\pm 0.1$ ns and  $\pm 0.5$ ns respectively.

**Figure 9 – Mask of a Pulse corresponding to a binary One**

## ELECTRICAL SPECIFICATIONS (continued)

### TRANSMITTER OUTPUT JITTER

The transmit jitter specification ensures compliance with ITU-T G.813, G.823, G.825 and G.958; ANSI T1.102-1993 and T1.105.03-1994; and GR-253-CORE for all supported rates. Transmit output jitter is not tested during production test.



| PARAMETER                 | CONDITION   | MIN | NOM | MAX   | UNIT |
|---------------------------|---|-----|-----|-------|------|
| Transmitter Output Jitter | 200 Hz to 3.5 MHz, measured with respect to CKREF for 60s |     |     | 0.075 | UIpp |



## ELECTRICAL SPECIFICATIONS (continued)

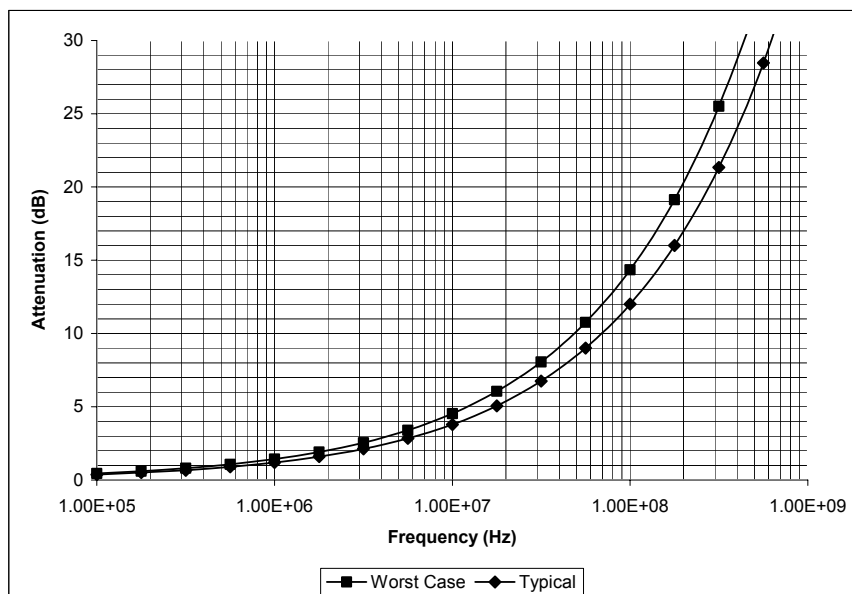
### RECEIVER SPECIFICATIONS FOR CMI INTERFACE (Transformer-coupled)

Consult application notes for reference schematic, layout guidelines, and recommended transformers.

| PARAMETER                                      | CONDITION                                       | MIN | TYP | MAX | UNIT |
|--|---|-----|-----|-----|------|
| Peak Differential Input Amplitude, RXP and RXN | MON=0. 12.7dB of cable loss                     | 70  |     | 550 | mVpk |
| Peak Differential Input Amplitude, RXP and RXN | MON=1. 20dB flat loss with 6dB cable loss (max) | 25  |     | 80  | mVpk |
| Flat-loss Tolerance                            | MON=0. All valid cable lengths.                 | -2  |     | 4   | dB   |
| Latency  |   |     | 5   | 10  | UI   |
| PLL Lock Time                                  |   |     | 1   | 10  | μs   |
| Return Loss                                    | 7MHz to 240MHz                                  | 15  |     |     | dB   |

The input signal is assumed compliant with ITU-T G.703 and can be attenuated by the dispersive loss of a cable. The minimum cable loss is 0dB and the maximum is -12.7dB at 78MHz.

The "Worst Case" line corresponds to the ITU-T G.703 recommendation. The "Typical" line corresponds to a typical installation referred to in ANSI T1.102-1993. The receiver is tested using the cable model. It is a lumped element approximation of the "Worst Case" line.



**Figure 10: Typical and worst-case Cable attenuation**

## ELECTRICAL SPECIFICATIONS (continued)

### RECEIVER JITTER TOLERANCE

The 78P2351R exceeds all relevant jitter tolerance specifications shown in Figure 11. STM-1e (electrical) jitter tolerance specifications are in ITU-T G.825. Receive jitter tolerance is not tested during production test.

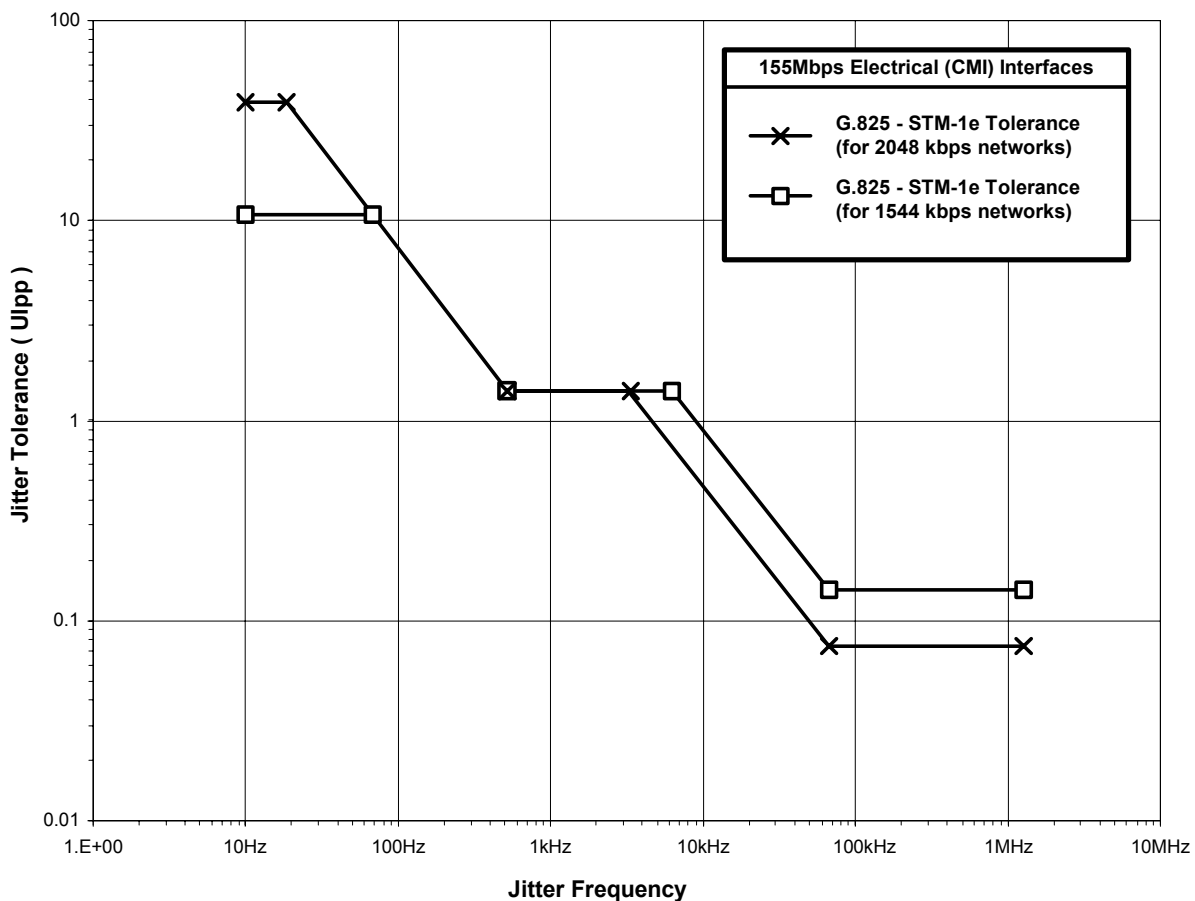


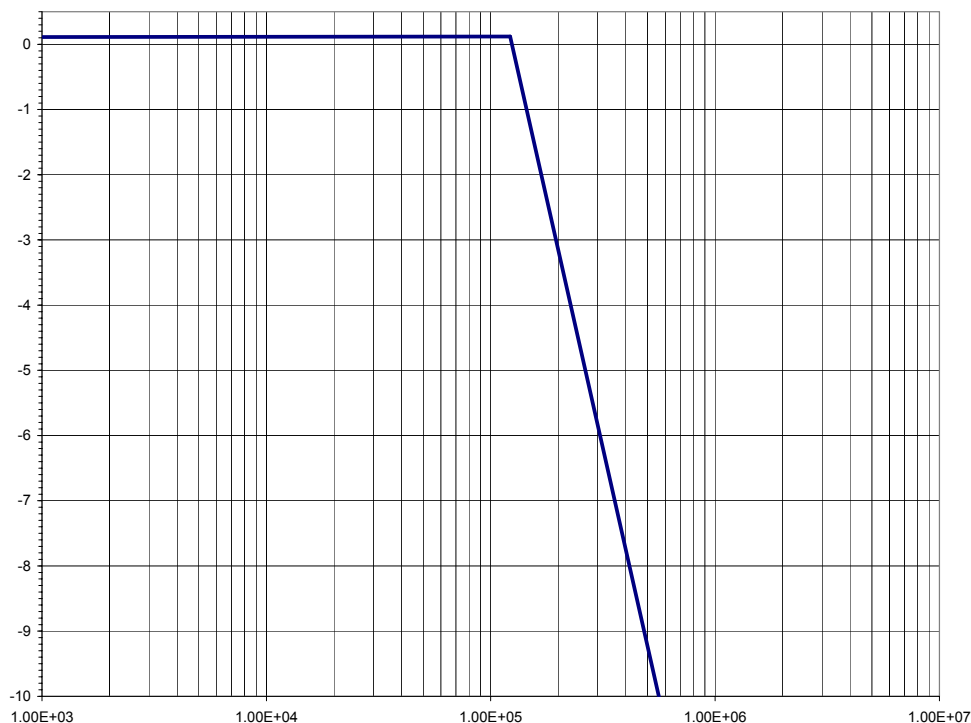
Figure 11: Jitter Tolerance - electrical (CMI) interfaces

| PARAMETER               | CONDITION       | MIN  | NOM      | MAX | UNIT |
|-------------------------|-----------------|------|----------|-----|------|
| STM-1e Jitter Tolerance | 10Hz to 19.3Hz  | 38.9 |          |     | UIpp |
|                         | 19.3Hz to 500Hz |      | 750 f-1  |     | μs   |
|                         | 500Hz to 6.5kHz | 1.5  |          |     | UIpp |
|                         | 6.5kHz to 65kHz |      | 9800 f-1 |     | μs   |
|                         | 65kHz to 1.3MHz | 0.15 |          |     | UIpp |

## ELECTRICAL SPECIFICATIONS (continued)

### RECEIVER JITTER TRANSFER FUNCTION

The receiver clock recovery loop filter characteristics such that the receiver has the following transfer function. The corner frequency of the Rx DLL is approximately 120 kHz. Receiver jitter transfer function is not tested during production test.



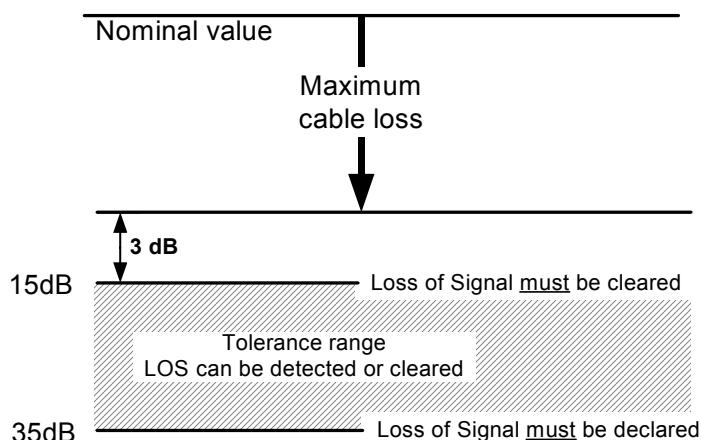
**Figure 12: Jitter Transfer**

| PARAMETER                         | CONDITION     | MIN | NOM | MAX | UNIT          |
|-----------------------------------|---------------|-----|-----|-----|---------------|
| Receiver Jitter transfer function | below 120 kHz |     |     | 0.1 | dB            |
| Jitter transfer function roll-off |               |     | 20  |     | dB per decade |

## ELECTRICAL SPECIFICATIONS (continued)

### LOSS OF SIGNAL CONDITION

| PARAMETER     | CONDITION | MIN | TYP | MAX | UNIT |
|---------------|-----------|-----|-----|-----|------|
| LOS threshold |           | -35 | -19 | -15 | dB   |
| LOS timing    |           | 10  | 110 | 255 | UI   |



## APPLICATION INFORMATION

### EXTERNAL COMPONENTS:

| COMPONENT                        | PIN(S)       | VALUE | UNITS    | TOLERANCE |
|----------------------------------|--------------|-------|----------|-----------|
| Receiver Termination Resistor    | RXP<br>RXN   | 75    | $\Omega$ | 1%        |
| Transmitter Termination Resistor | CMIP<br>CMIN | 75    | $\Omega$ | 1%        |

### TRANSFORMER SPECIFICATIONS:

| COMPONENT                                       | VALUE | UNITS | TOLERANCE |
|---|-------|-------|-----------|
| Turns Ratio for the Receiver                    |       | 1:1   |           |
| Turns Ratio for the Transmitter (center-tapped) |       | 1:1CT |           |

Suggested Manufacturers: Halo, MiniCircuits, Tamura, Belfuse

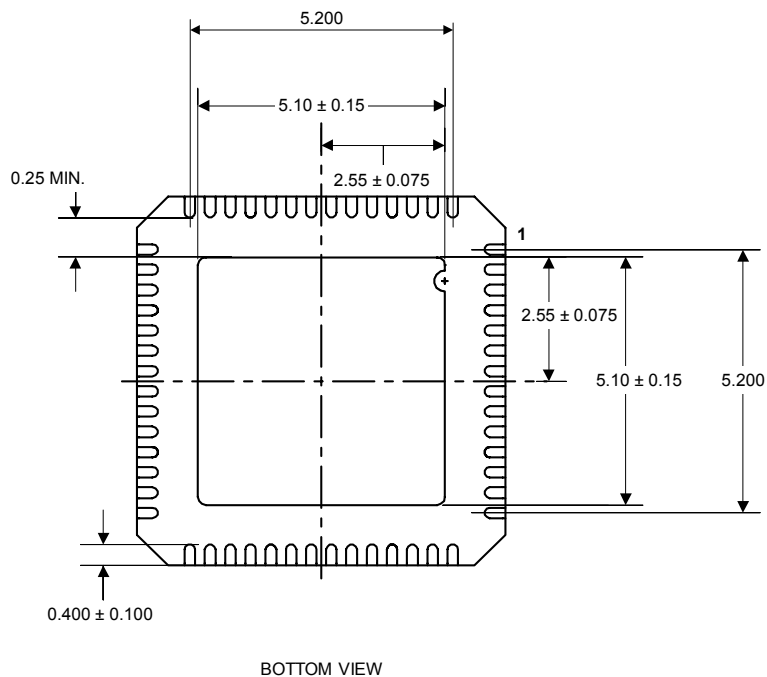
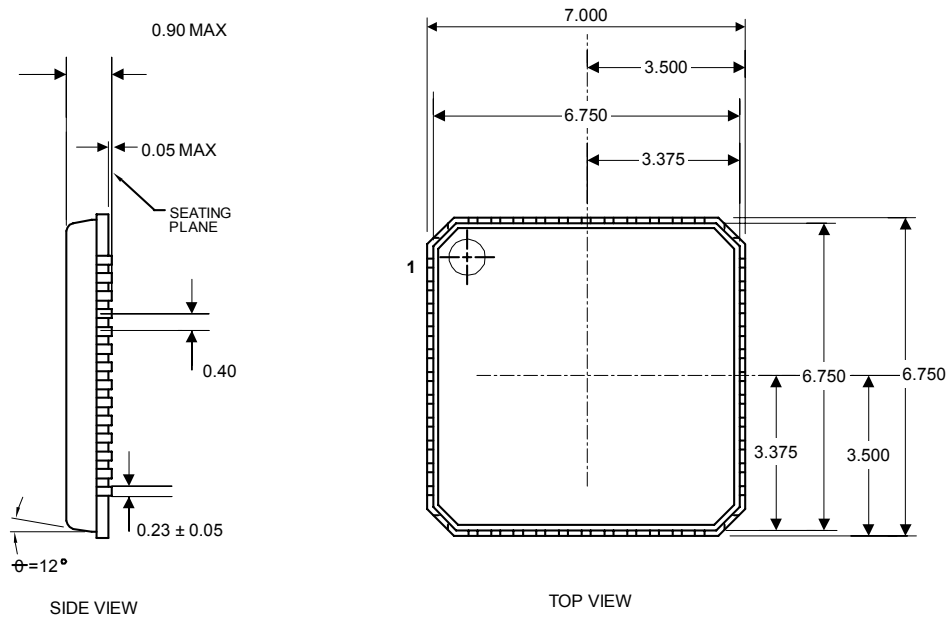
### THERMAL INFORMATION:

| PACKAGE                   | CONDITIONS   | $\Theta_{JA}$ (°C/W) | $\Theta_{JC}$ (°C/W) |
|---------------------------|--|----------------------|----------------------|
| Standard 56-pin JEDEC QFN | No forced air;<br>4-layer JEDEC test board                                   | 46.8                 | 16.6                 |
|                           | No forced air;<br>4-layer JEDEC test board<br>Die attach pad soldered to PCB | 23.5                 | 15.6                 |

## SCHEMATICS

For reference schematics, layout guidelines, suggested transformer part numbers, etc. please check Teridian Semiconductor's website or contact your local sales representative for the latest application note(s) and/or evaluation boards.

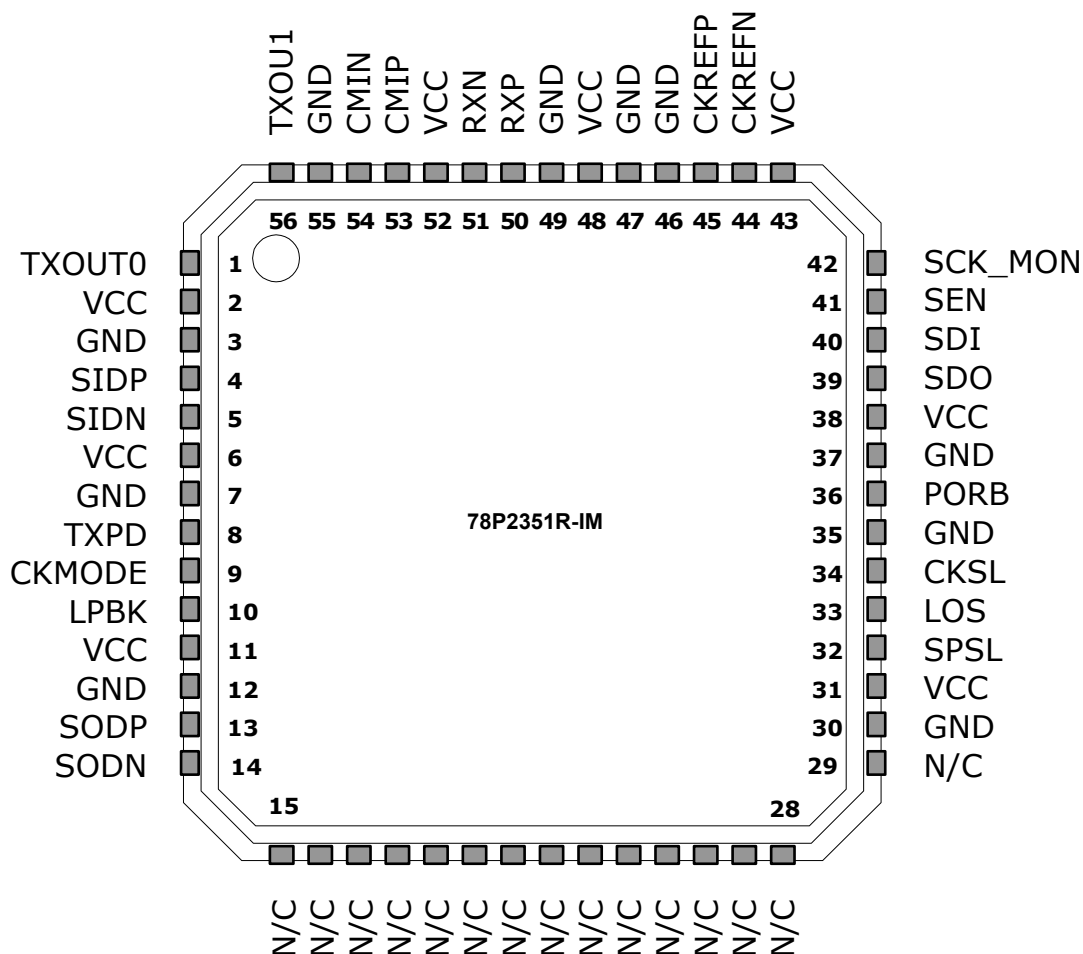
## MECHANICAL SPECIFICATIONS



**56-pin Quad Flat No-lead package (QFN)**  
(All dimensions in mm)

## PACKAGE INFORMATION

(Top View)



## ORDERING INFORMATION

| PART DESCRIPTION         | ORDER NUMBER | PACKAGE MARK                 |
|--------------------------|--------------|------------------------------|
| 56-pin QFN; Revision A06 | 78P2351R-IM  | 78P2351R-IM<br>xxxxxxxxxxP6  |
| Tape & Reel option       | append 'R'   | n/a                          |
| Lead-free option         | append 'F'   | xxxxxxx-xxx<br>xxxxxxxxxxP6F |

| Revision History |  |
|------------------|--|
| --               | <b>Contact Teridian for revision history of earlier releases</b>   |
| v2-0             | <b>August 15, 2005: Final Datasheet Release</b> <ul style="list-style-type: none"> <li>Updated Ordering Numbers to reflect production silicon revision A06</li> <li>Improved/modified Functional Descriptions</li> <li>Improved/modified Register Descriptions               <ul style="list-style-type: none"> <li>Added FLBK bit</li> <li>Removed Rx LOL bit</li> </ul> </li> <li>Improved/modified Pin Descriptions</li> <li>Updated Electrical Specification min/max limits for:               <ul style="list-style-type: none"> <li>DC Characteristics,</li> <li>CID, CIU, CIT, and PO pin types</li> <li>CMI Loss of Signal Conditions</li> </ul> </li> <li>Changed name and logo from TDK to Teridian</li> </ul> |
| v2-1             | <b>August 15, 2006:</b> <ul style="list-style-type: none"> <li>Updated Ordering Numbers to remove silicon revision A06</li> <li>Updated Package Mark from C6 to P6</li> </ul>  |

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Teridian Semiconductor Corp., 6440 Oak Canyon Rd., Irvine, CA 92618  
 TEL (714) 508-8800, FAX (714) 508-8877, <http://www.teridian.com>

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