TEXAS INSTRUMENTS

CDC7005 Evaluation Module Manual

High Performance Analog/CDC

User's Guide

2004

Clock Drivers

SCAU005B

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Preface

Read This First

About This Manual

This manual explains how to use the CDC7005 evaluation module and to provide the guidelines to build the customer's own systems. The manual includes schematics, layout, bill of materials, and a software description.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1—Introduction
- ❏ Chapter 2—Quick Start
- ❏ Chapter 3—EVM Hardware
- ❏ Chapter 4—Serial Peripheral Interface (SPI) Software
- ❏ Chapter 5—Schematics, Board Layout, and Parts List

Related Documentation From Texas Instruments

- ❏ CDC7005 Data Sheet, SCAS685, Texas Instruments

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If You Need Assistance. . .

If you need assitance with this device, please email
clocks_apps@list.ti.com

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Tables

Chapter 1

Introduction

The CDC7005 is a high-performance, low phase noise and low skew clock synchronizer that synchronizes an on-board voltage controlled crystal oscillator (VCXO) frequency to an external reference clock. The device operates up to 800 MHz. The PLL loop bandwidth and damping factor can be adjusted to meet different system requirements by selecting the external VCXO, loop filter components, frequency for PFD, and charge pump current. Each of the five differential LVPECL outputs can be programmed by a serial peripheral interface (SPI). The SPI allows individual control of the frequency and enable/disable state of each output. As the system requires external components like a loop filter and VCXO, this EVM provides an excellent way to evaluate and modify the performance and parameters of the clock system in conjunction with the specific customer application. Loop bandwidth can be selected as low as 10 Hz or less, allowing this device to clean the system's clock jitter. The CDC7005 can be used as a simple 1:5 LVPECL buffer with output dividing options.

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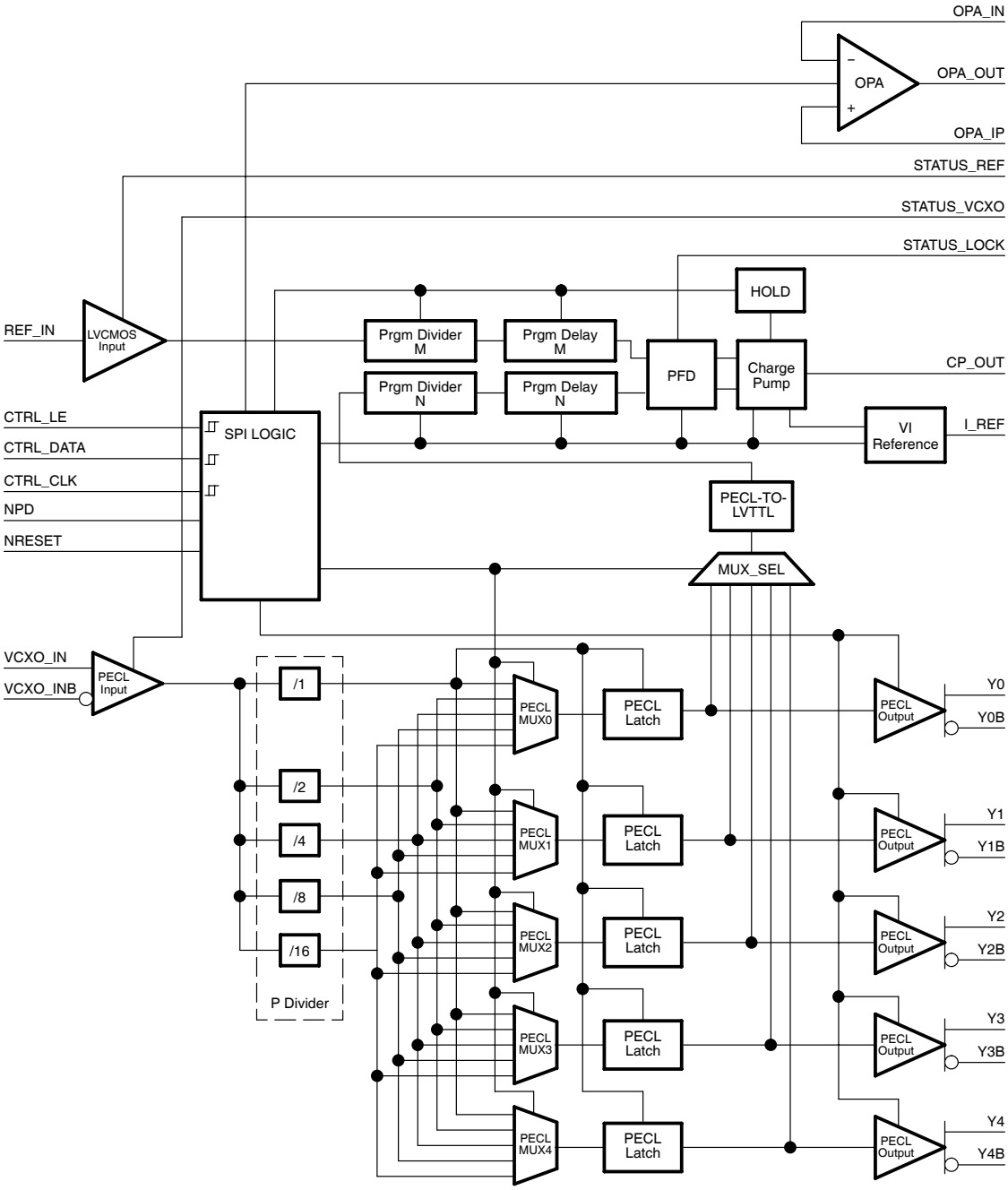
1.1 CDC7005 Functional Block Diagram



Chapter 2

Quick Start

In order to setup the EVM quickly and to take some measurements at default settings, the following actions are required:

- ❑ Supply 3.3 V to P1, LED D4 will be on.
- ❑ Apply a single-ended reference clock to the reference clock input (REF_IN). For default setting, the reference clock must be 1/8th of VCXO frequency (if VCXO frequency is 245.76 MHz, then the reference clock must be 30.72 MHz for locking).
- ❑ Connect Y0/Y0B (or Y1/Y1B) to oscilloscope in order to check output signal. Ensure the oscilloscope has 50 Ω to ground termination.

After power up, D1 is on if there is a valid reference clock and D2 is on if there is a valid VCXO clock for the CDC7005. If the reference clock and VCXO clocks are phase locked, D3 is on.

Chapter 3

EVM Hardware

This chapter discusses the EVM hardware.

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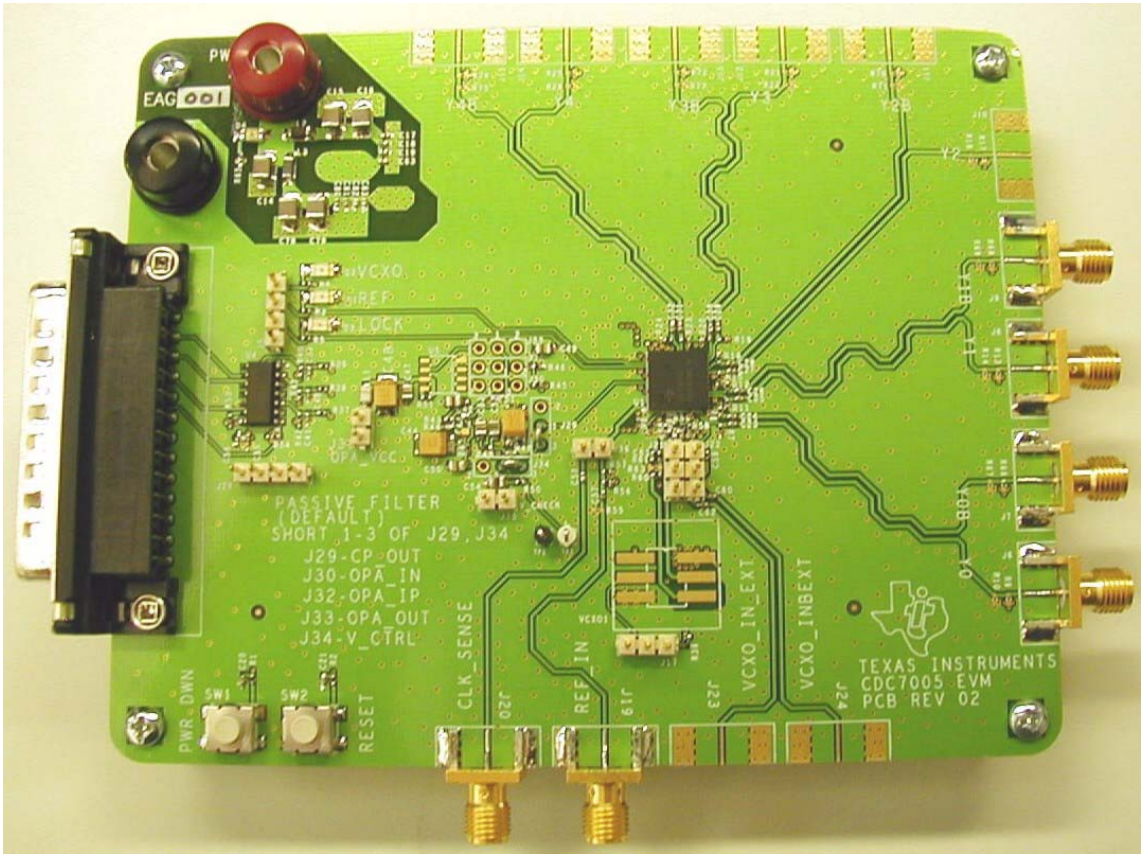
3.1 Board View and Connector Location

Figure 3–1. Board View



3.2 Connector Description

Table 3–1. Connectors, Switches, and Indicators

Reference	Description
P1	Power supply 3.3 V
P2	GND
J5	Status outputs (STATUS_LOCK, STATUS_VCXO, STATUS_REF)
J6, J7	Y0/Y0B PECL differential output
J8, J9	Y1/Y1B PECL differential output
J10, J11	Y2/Y2B PECL differential output
J12, J13	Y3/Y3B PECL differential output
J14, J15	Y4/Y4B PECL differential output
J17	VCXO enable
J36	Reference clock input sense enable (on or off)
J19	Reference clock input
J20	Reference clock input sense
J21, J22	VCXO_IN/VCXO_INB input selector/VCXO output selector
J23, J24	External VCXO_IN/VCXO_INB input/VCXO output sense
J27	External programming interface by parallel port
J28	External programming interface by universal pins
J29, J34	Filter type selector
J30	Non-inverted OPA input selector (external or internal OPA)
J31	Power supply for external OPA (on or off)
J32	Inverted OPA input selector (external or internal OPA)
J33	OPA output selector (internal or external OPA)
J35	VCXO control voltage sense
SW1	Power-down key
SW2	Reset key
D1	STATUS_REF indicator
D2	STATUS_VCXO indicator
D3	STATUS_LOCK indicator

3.3 Hardware Configuration

This section describes the board configuration using on-board jumpers and solder bridges.

Note:

Default settings are in italics.

3.3.1 Power Supply (P1, P2)

- ❑ Supply 3.3 V ±10% on P1 and P2 using a stabilized external power supply.
  - ■ **WARNING: Never supply more than 3.6 V on P1.**

3.3.2 Onboard Switches and Indicators (P1, P2, D1–D4)

- ❑ Push SW1 to enter the power-down mode of the CDC7005 device. Then all current sources are switched off, all outputs are switched into 3-state, and all dividers (M, N, and P) are reset to default.
- ❑ Push SW2 to enter the reset mode of the device. Then the dividers (M, N, and P) are reset to default.
- ❑ The three status outputs of the CDC7005 are fed to LED indicators and to pin header J5. An D1 on condition indicates a valid reference input clock signal, D2 is on if the VCXO input clock is valid, and D3 turns on if PLL has been locked.
- ❑ D4 indicates power supply

Default setting: *I_REF is connected to ground through a 12-kΩ resistor*. For default operation, the device uses an internal resistor.

Note:

In case of low input impedance of the VCXO control voltage input, there is a possibility D3 may not turn on to indicate locking.

3.3.3 Programming Interfaces (J27, J28)

The SPI of the device is used for writing to the control register of the device. It consists of three control lines CTRL_CLK, CTRL_DATA, and CTRL_LE. There are four 30-bit wide RAM registers, which can be addressed by the two LSBs of a transferred word. Every transmitted word must have 32 bits, starting with MSB. After supplying power or activating the power-down mode, the registers are loaded with the device default values internally (see the CDC7005 data sheet, SCAS685). However, if specific register settings are required for any applications, there are two ways to program the device externally:

- ❑ Connect the parallel port cable to the PC and EVM parallel port. This needs control S/W (see Chapter 5).
- ❑ Connecting an external pattern generator to J28. Connect pin 18 of J27 to the ground.

3.3.4 Loop Filter (J29–J35)

The loop filter is one of the key elements determining the loop bandwidth of the PLL. The loop filter converts the charge pump current into the control voltage for the voltage controlled oscillator. The phase difference between the input clocks of the phase frequency detector determines the width of the charge pump output current pulses. These high frequency pulses are transformed into a voltage to control the oscillator.

Basically, three types of loop filters are implemented on the EVM.

- ❏ Passive loop filter
- ❏ Active loop filter using an operational amplifier (OPA) implemented on the CDC7005.
- ❏ Active loop filter using an external low-noise OPA.

Filter types can be selected by soldering the bridges J29–J30 and J32–J34, see Table 3–2. Control voltage of the VCXO can be measured at J35. If an external OPA is used, it needs to be switched on by connecting J31. For example, passive filter operation is provided when pads 1 and 3 of J29 are solder bridged and pads 1 and 3 of J34 are solder bridged.

Default setting: Passive Loop Filter

Note:

Using an active loop filter requires changing of the charge pump direction via SPI programming.

Table 3–2. Filter Configurations

Bridge	Passive Filter	Active With An Internal OPA	Active With An External OPA
J29	1–3	1–2	1–2
J30	Don't care	1–3	1–2
J31	Open	Open	Closed
J32	Don't care	1–2	1–3
J33	Don't care	1–2	1–3
J34	1–3	1–2	1–2

3.3.5 High-Speed Outputs and Inputs (J6–J15 and J19–J20)

The CDC7005 drives five differential LVPECL outputs. All PECL outputs are ac-coupled and terminated with 150 Ω to GND. This is in contrast to typical LVPECL termination, which requires V_{CC} – 2 V as termination voltage. The reason is to simplify the power supply scheme. The device output's trace impedance is 50 Ω and traces are matched in length. All outputs have options for pull-up and pull-down resistors.

The reference input clock signal has to be applied to J19. The reference input clock signal can be sensed on J20. In this case, close the bridge J36 (the oscilloscope's 50 Ω may be used to terminate the 50-Ω trace). The reference input clock sense line is matched to the LVPECL outputs line to avoid any additional delay offset. The input is ac-coupled (C57) and properly biased with 100-Ω pull-up and 100-Ω pull-down resistors.

3.3.6 VCXO Inputs and Outputs (J23–J28)

The CDC7005 requires an external VCXO in order to complete the PLL loop. The VCXO adjusts the frequency and phase depending on the control voltage level coming from loop filter and provide the input clock to the LVPECL block.

The circuitry lets the user:

- Measure the on-board VCXO output from outside on J23 and J24 (close 1–3 of J21 and 1–3 of J22).
- Feed the LVPECL clock from an external source into the VCXO_IN/ VCXO_INB inputs of the CDC7005. If the CDC7005 is intended to be used as a programmable clock buffer without PLL capabilities, then close 2–3 of J21 and J22. In case of using an external oscillator (or VCXO), close 2–3 of J21 and J22. The VCXO output clock has to be applied on J23 and J24 and VCXO control voltage can be taken on TP1.

Default settings: J17 is open, 1–2 of J21 and J22 are connected.

Note:

This EVM offers universal foot print for VCXO, so it allows the addition of several VCXO's.

Chapter 4

Serial Peripheral Interface (SPI) Software

This chapter discusses the serial peripheral interface software.

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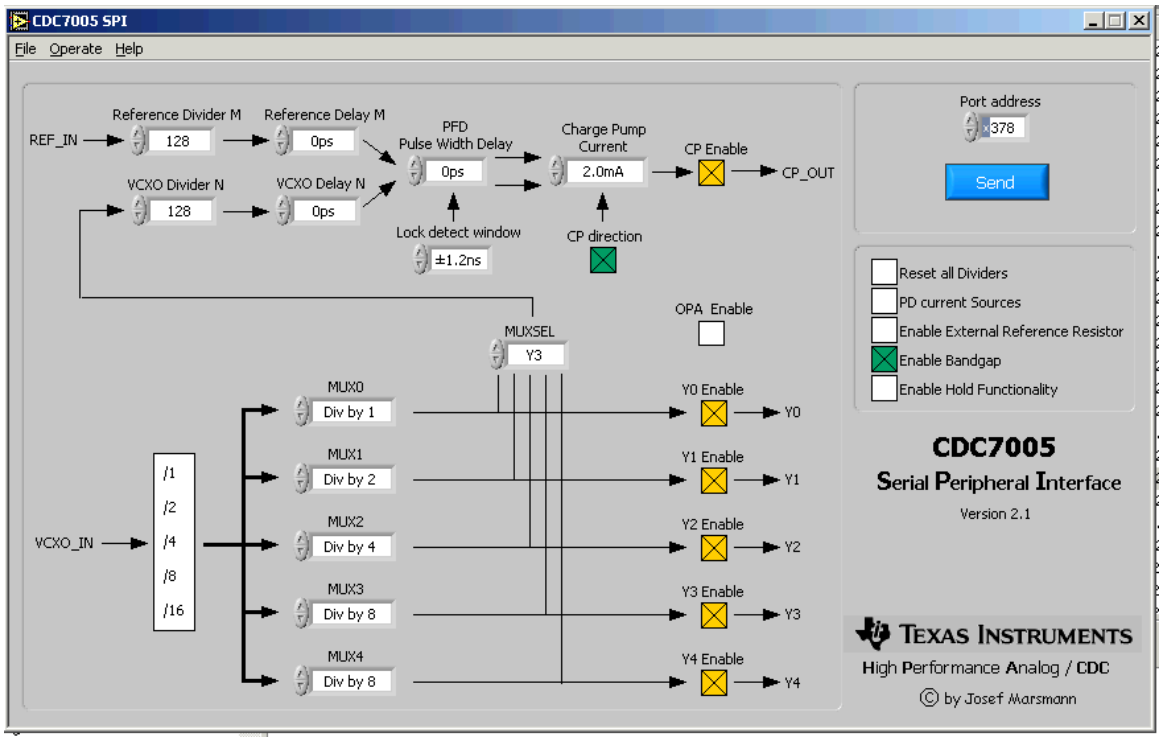
4.1 Functional Description

Programming software is required for programming the internal control register of the CDC7005 in the EVM. The software runs under Windows98, NT, and 2000. A quick installation is required prior to use. See Section 4.2 *Software Installation*.

There are several cases where programming is mandatory:

- Using an active loop filter
- Reference clock and VCXO clock do not have a ratio of 1:8.
- Changing of divider ratio or disabling of certain LVPECL output
- Changing of phase offset, (delay M/N)
- Changing of charge pump output current
- Widening the lock detect window

Figure 4–1. Screen View



4.2 Software Installation

Use the following steps to install the SPI control software.

1) Run program setup.exe in folder Software\Programming Software
2) Run program setup.exe in folder Software\Parallel Port Access
3) Reboot the computer
4) Run the software from Start –> Programs –> CDC7005 SPI –> CDC7005 SPI EVM

Chapter 5

Application Level Circuit Diagram

This chapter discusses the application level circuit diagram.

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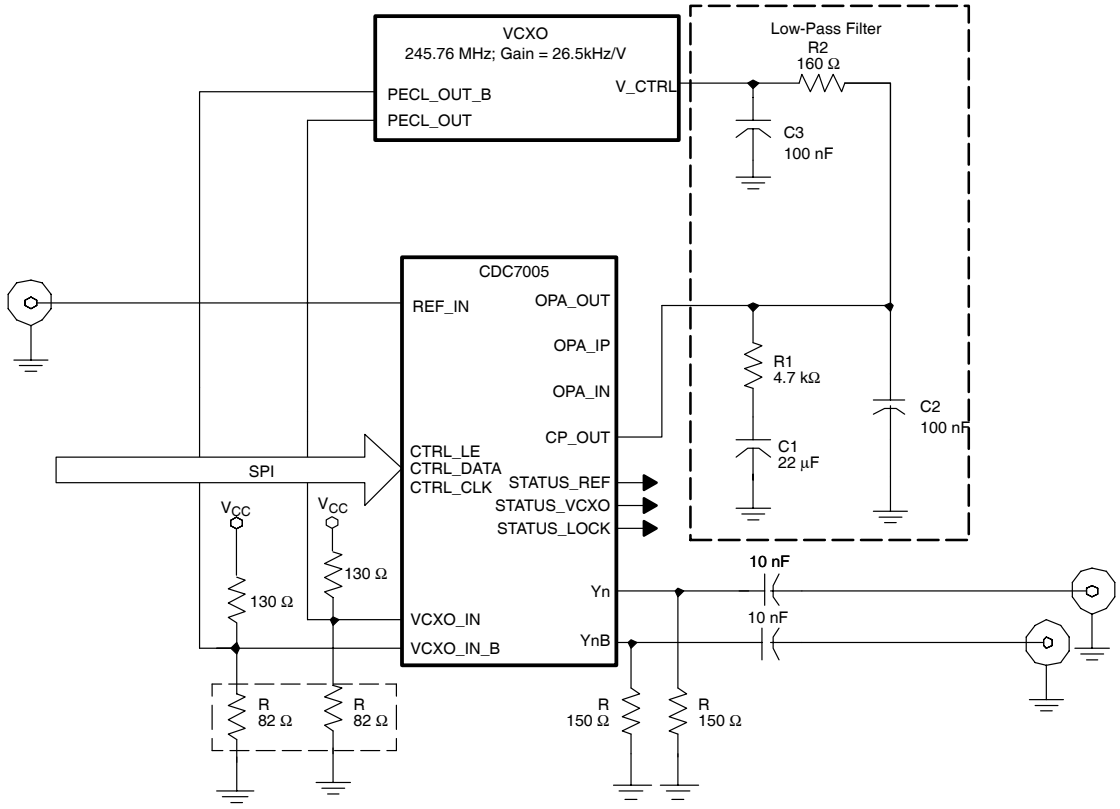
5.1 Application Level Circuit Diagram

In the following applications sections all three loop filter configurations are discussed.

5.1.1 Passive Loop Filter

The passive loop filter is a second order filter (two poles, one zero). The zero is required for the overall loop stability. R1, C1, and C2 generate the dominant pole of the system. A second pole is introduced by R2 and C3.

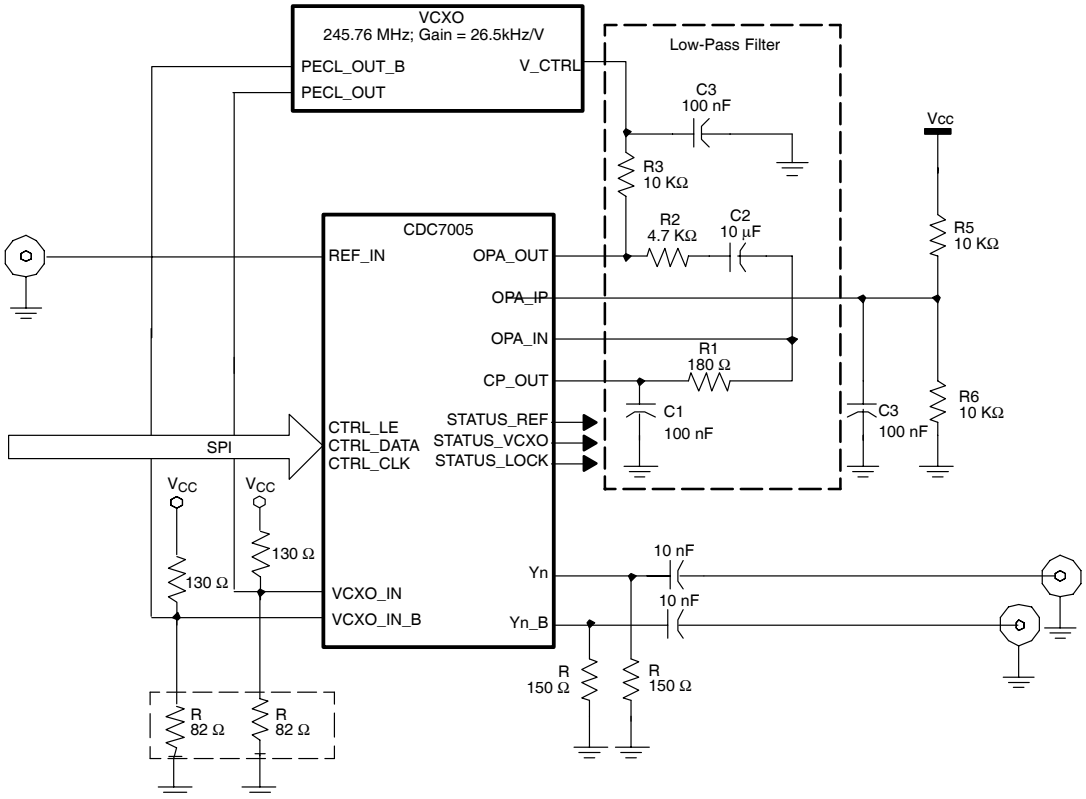
Figure 5–1. CDC7005 With a Passive Loop Filter Configuration



5.1.2 Active Loop Filter—Internal Operational Amplifier

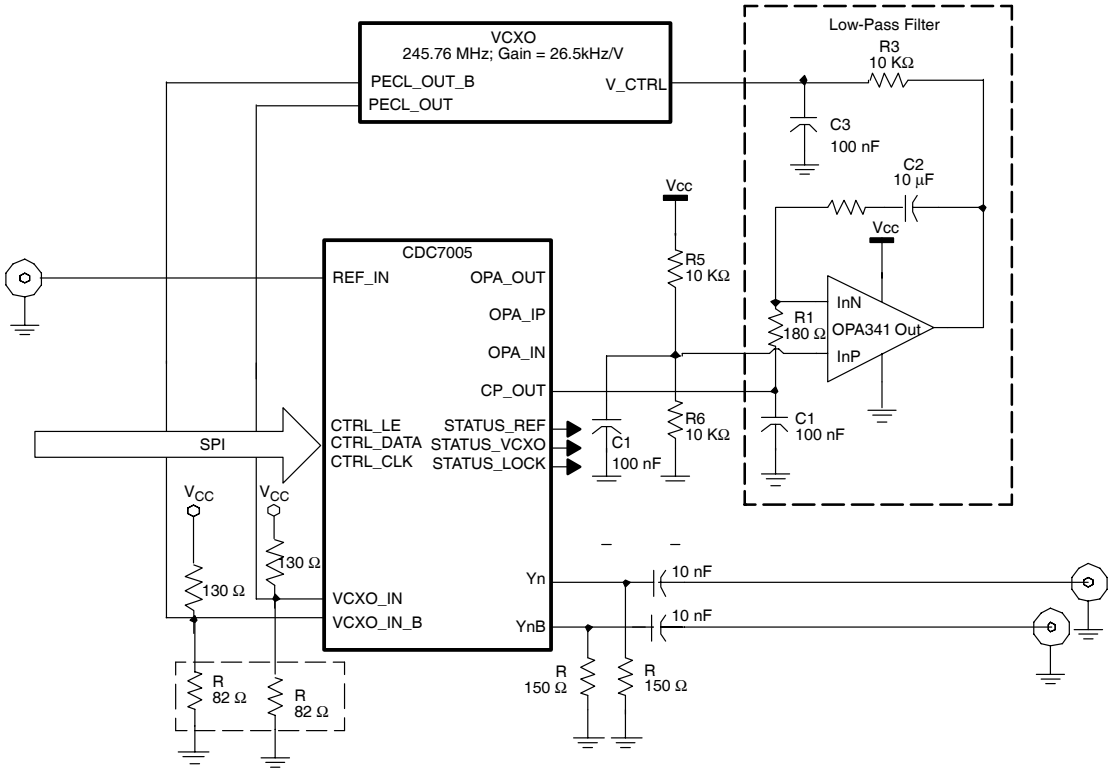
The active loop filter requires zero for loop stability, which is generated by R2 and C2 components. The first pole is introduced by R3 and C3 and the second pole is introduced by R1 and C1.

Figure 5–2. CDC7005 With an Active Loop Filter Using a CDC7005 Integrated OPA



5.1.3 Active Loop Filter—External Operational Amplifier

Figure 5–3. CDC7005 With an Active Loop Filter Using OPA341



Chapter 6

Parts List, Board Layout, and Schematic

This chapter contains the parts list, board layout, and schematic for the CDC7005 EVM.

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6.1 Parts List

Item	Qty	Reference Designator	Part	Part Number	Note
1	3	C14, C15, C78	22 μF, 16 V 20% tantalum TE SMD	Panasonic ECS−T1CC226R	
2	4	C16, C64, C65, C79	10 μF, 16 V TANT TEH SER SMD	Panasonic ECS−H1CC106R	
3	4	C17, C80, C35, C55	0.1 μF, 16 V ceramic Y5V 0402	Yageo 04022F104Z7B20D	
4	2	C81, C18	0.033 uF, 10% 16 V X5R 0402 ceramic	AVX 0402YD333KAT2A	
5	22	C19, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C57, C58, C60, C62, C63, C66, C67, C68, C69, C82, C83	0.01 μF, 25 V ceramic X7R 0402	Panasonic ECJ−0EB1E103K	
6	2	C21, C20	0.01 μF, 50 V ceramic Y5V 0402	Panasonic ECJ−0EF1H103Z	
7	6	C34, C56, C74, C75, C76, C77	100 pF, 25 V ceramic X7R 0402	Panasonic ECJ−0EB1E101K	
9	3	C39, C40, C41	Ceramic 10 pF, 25 V C0G 0402	Panasonic ECD−G0E100C	
10	7	C42, C47, C49, C50, C52, C53, C54	0.1 μF, 16 V film 0805 20%	Panasonic ECP−U1C104MA5	Must be film cap
11	1	C43	NU	Panasonic ECP−U1C104MA5	
12	2	C44, C48	10 μF, 25 V 10% X5R 1210 ceramic	Murata GRM32DR61E106KA12L	
13	1	C51	22 μF, 10 V 10% X7R 1210 ceramic	Murata GRM32ER71A226KE20L	
14	4	C59, R60, R61, C61	0 Ω	Panasonic ERJ−2GE0R00X	
15	4	C70, C71, C72, C73	0.022 μF 10% 16 V X7R 0402	AVX 0402YC223KAT2A	
16	3	D1, D2, D3	LED, amber	Lite−On LTST−C150AKT	
17	1	D4	LED, green	Lite−On LTST−C150KGKT	
18	2	J5, J28	HDR4	Header 4 pos, 0.100 ctr	
19	6	J6, J7, J8, J9, J19, J20	SMA CONN	Johnson Comp 142−0701−841	
20	8	J10, J11, J12, J13, J14, J15, J23, J24	NU SMA CONN		
21	3	J17, J21, J22	HDR3	Header 3 pos, 0.100 ctr	
22	1	J27	CONN 25-pin male DSUB	SPC Technology DB−25P−PCB	

23	5	J29, J30, J32, J33, J34	NU HDR	Not used (header 3 pos, 0.100 ctr)	J29, J34 pin 1–3 shorted
23a	2	MP4	Jumper wire, 00.1" long	3M/ESD 923345–01–C	To short pin 1 and 3 of J29, J34
Item	**Qty**	**Reference Designator**	**Part**	**Part Number**	**Note**
24	3	J31, J35, J36	HDR2	Header 2 pos, 0.1 ctr	
25	1	L1	Inductor chip 20.2NH 20% SMT	J W Miller Magnetics PM0805–2N2M	
26	2	L3, L2	75 Ω at 100 MHz	Murata BLM31PG500SN1L	
27	1	P1	PWR_IN banana jack	Pomona Model 3267	
28	1	P2	GND banana jack	Pomona Model 3267	
29	9	R1, R2, R36, R45, R46, R47, R51, R53, R54	100 kΩ 1/16W 1% 0402 SMD	Panasonic ERJ–2RKF1002X	
30	3	R3, R4, R5	750 Ω 1/16W 5% 0402 SMD	Panasonic ERJ–2GEJ751X	
31	1	R6	12 kΩ 1/16W 5% 0402 SMD	Panasonic ERJ–2GEJ123X	
32	10	R7, R8, R11, R12, R15, R16, R19, R20, R23, R24	150 Ω 1/16W 1% 0402 SMD	Panasonic ERJ–2RKF1500X	
33	20	R9, R10, R13, R14, R17, R18, R21, R22, R25, R26, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75	NU RES	Panasonic ERJ–2RKF1000X	
34	5	R37, R38, R39, R56, R57	100 Ω 1/16W 1% 0402 SMD	Panasonic ERJ–2RKF1000X	
35	4	R40, R41, R42, R50	100 kΩ 1/16W 1% 0402 SMD	Panasonic ERJ–2RKF1003X	
36	1	R43	180 Ω 1/16W 5% 0402 SMD	Panasonic ERJ–2GEJ181X	
37	2	R48, R44	40.7 kΩ 1/16W 5% 0402 SMD	Panasonic ERJ–2GEJ472X	
38	1	R49	160 Ω 1/16W 5% 0402 SMD	Panasonic ERJ–2GEJ161X	
39	1	R55	NU	Panasonic ERJ–2GEJ510X	
40	2	R62, R58	130 Ω 1/16W 5% 0402 SMD	Panasonic ERJ–2GEJ131X	
41	2	R59, R64	82 Ω 1/16W 5% 0402 SMD	Panasonic ERJ–2GEJ820X	
42	1	R63	NU	NU	
43	1	R65	10.5 kΩ 1/16W 1% 0402 SMD	Panasonic ERJ–2RKF1501X	
44	2	SW2, SW1	SW pushbutton	KT11P3JM	
45	1	TP2	T point PC BLK	Keystone Elec 5011	

45a	1	TP1	T point PC WHT	Keystone Elec 5012
46	1	U1	CDC7005ZVA	Texas Instruments CDC7005ZVAT

Item	Qty	Reference Designator	Part	Part Number	Note
47	1	U4	SN74LV125	Texas Instruments SN74LV125AD	
48	1	U5	OPA341	Texas Instruments OPA341UA	
49	1	VCXO1	VCXO_6	Toyocom VCXO	
50	4	MP3	Stand off		Legs for PCB
51	4	MP2	Screw		Legs for PCB

6.2 Board Layout

Figure 6–1. Component View and Silkscreen

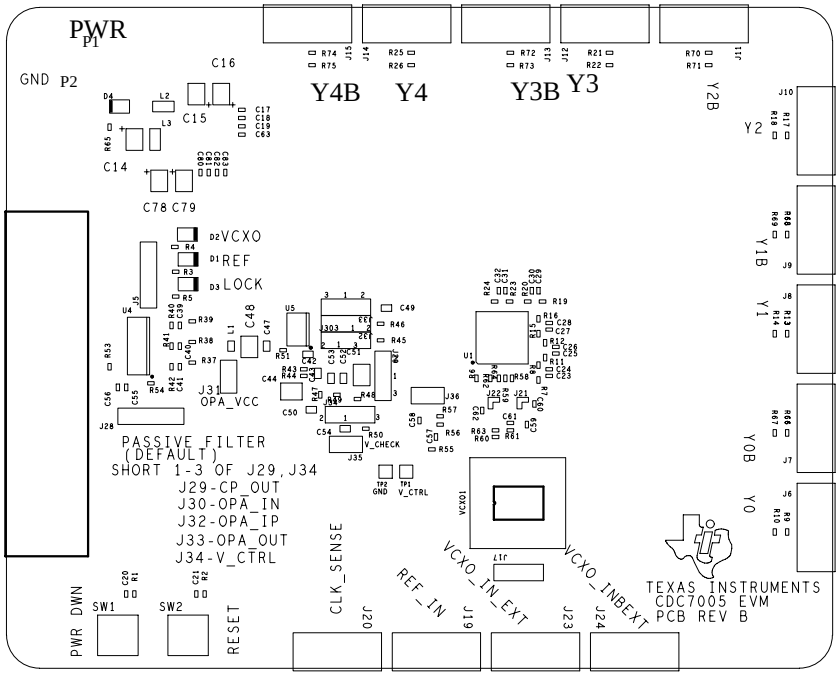


Figure 6–2. Top Layer View

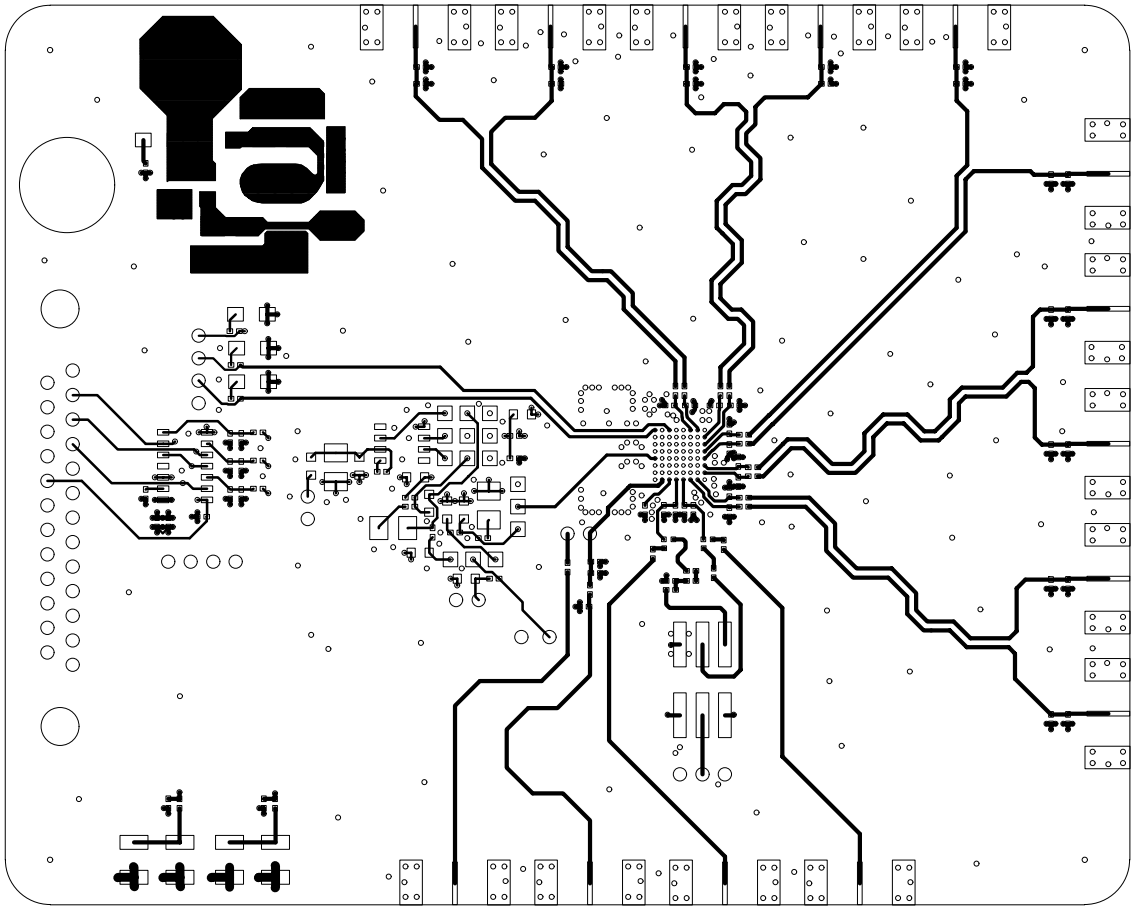


Figure 6–3. Bottom Layer View

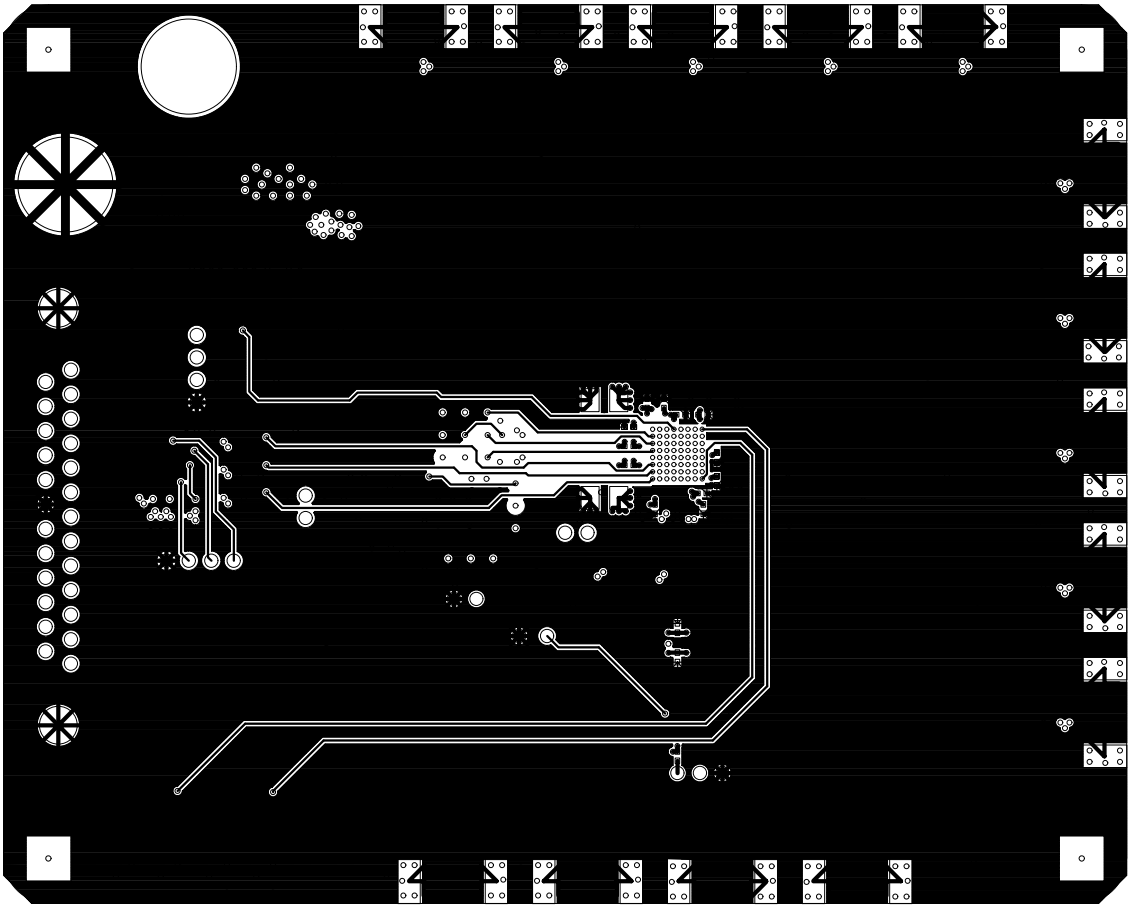


Figure 6–4. Ground Plane View

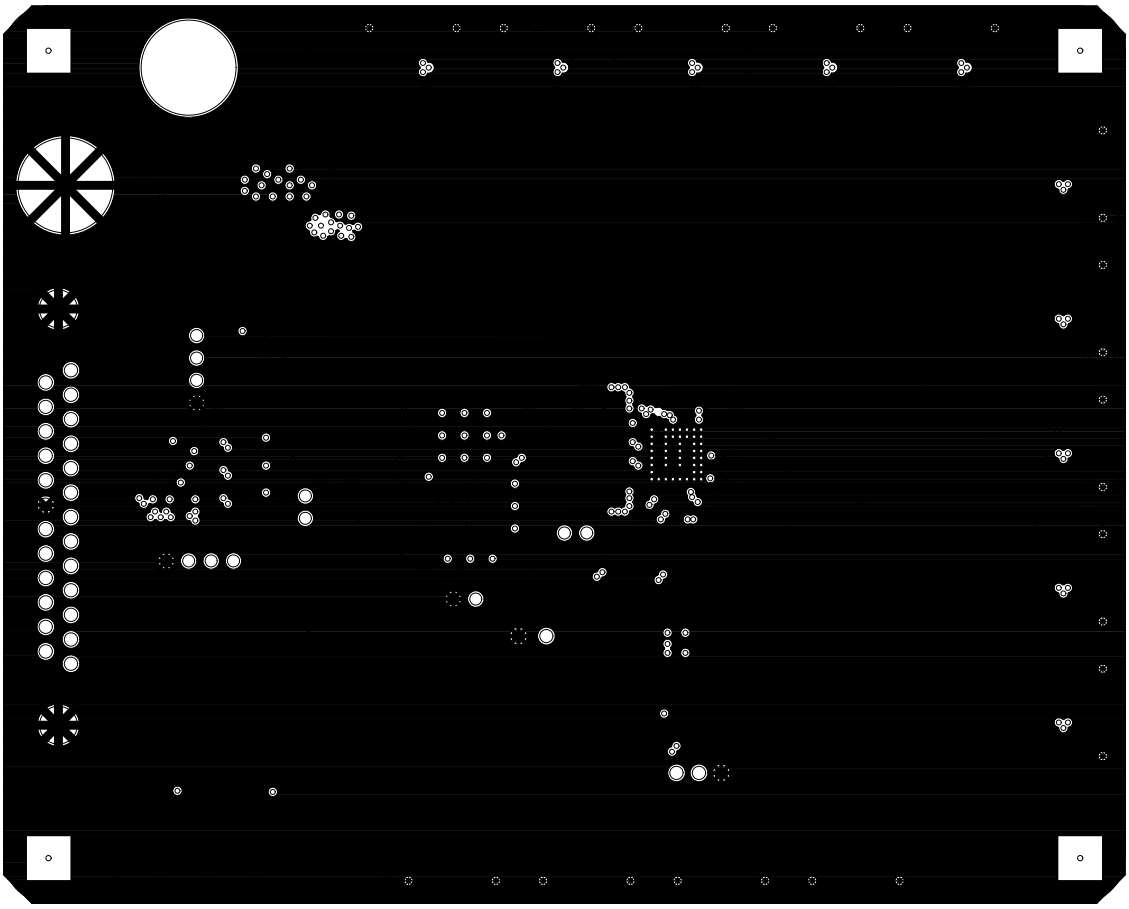
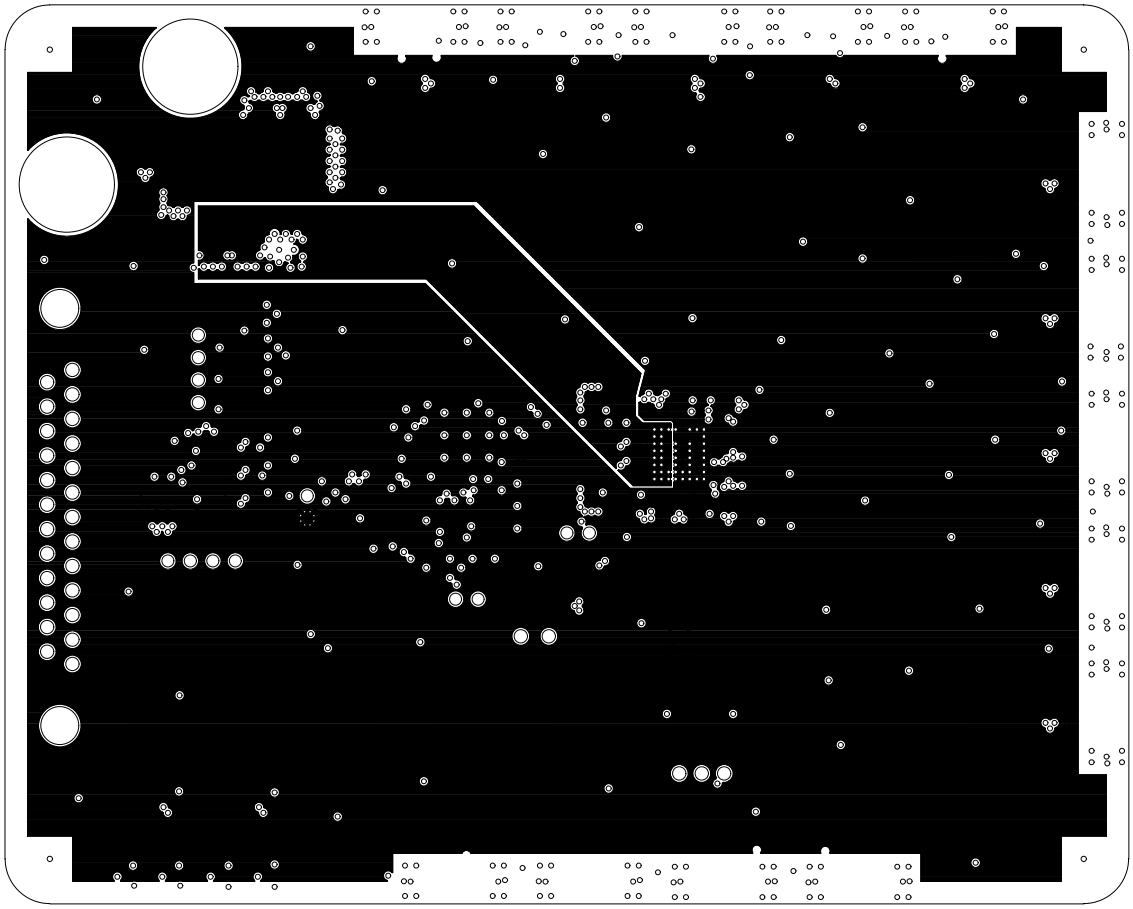
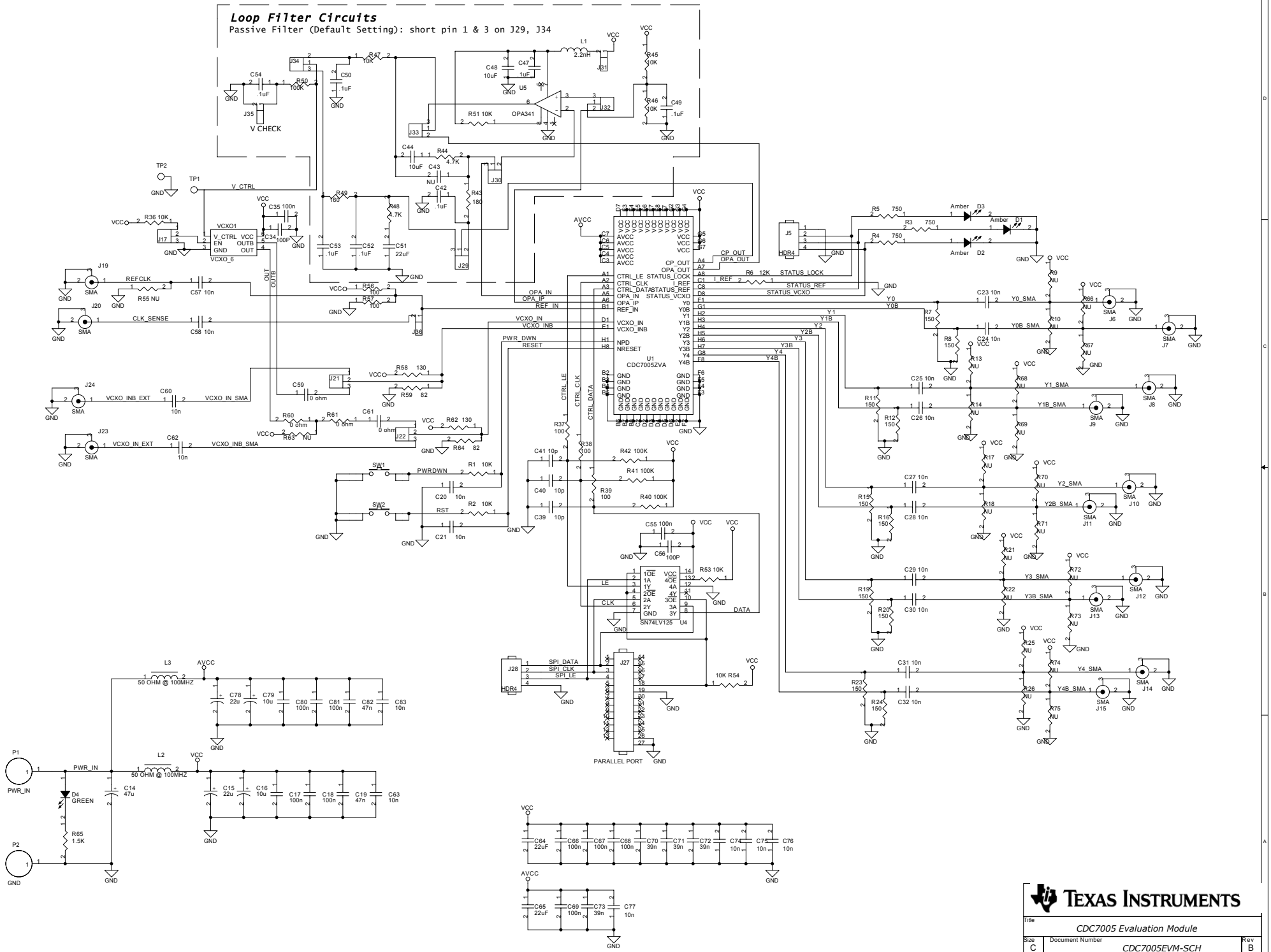


Figure 6–5. Power Layer View



6.3 Schematic

The following page contains the schematic for the CDC7005.


Loop Filter Circuits
Passive Filter (Default Setting): short pin 1 & 3 on J29, J34
V CHECK
V_CTRL
VCXO_6
REFCLK
CLK_SENSE
VCXO_INB_EXT
VCXO_IN_SMA
VCXO_IN_EXT
VCXO_INB_SMA
PWRDWN
RST
CDC7005ZVA
SN74LV125
PARALLEL PORT
SPI_DATA
SPI_CLK
SPI_LE
DATA
PWR_IN
50 OHM @ 100MHZ
GREEN
Amber
STATUS_LOCK
STATUS_REF
STATUS_VCXO
Y0_SMA
Y0B_SMA
Y1_SMA
Y1B_SMA
Y2_SMA
Y2B_SMA
Y3_SMA
Y3B_SMA
Y4_SMA
Y4B_SMA
TEXAS INSTRUMENTS
CDC7005 Evaluation Module
CDC7005EVM-SCH
Friday, September 10, 2004